XC4000XL Power Calculation

Almost all power consumption in Xilinx FPGAs is dynamic, the result of charging and discharging internal and external capacitance. The small exception is the static power used for internal housekeeping operations, for leakage current, and for driving external resistive loads.

The total dynamic power in XC4000XL devices is the sum of three major ingredients:

- Clock distribution power.
- Output power.
- Power used for internal logic and driving the interconnections.

The balance between these depends on the design implementation, but often the three ingredients have roughly equal magnitude.

Global Clock Distribution Power

All XC4000 Series devices use a clock distribution network that achieves short clock delay, negligible clock skew, and the lowest possible power consumption. Each global clock signal is routed to the center of the chip and then drives a horizontal "backbone." Each column of CLBs has several vertical clock distribution "Longlines," each serving the upper or lower half of a column. These Longlines are only driven when the flip-flop placement requires it, and flip-flop clock inputs are only connected to a clock line when needed. Clock power is thus minimized.

The total power for each global clock input has three ingredients:

- **A** - the power to drive the backbone.
- **B** - the discretionary power to drive each vertical half-Longline.
- **C** - the power to clock each individual flip-flop.

A and B are device-size dependent, while C is constant. Table 1 lists the values for A, B, and C , expressed in µW/MHz, with a nominal 3.3 V power supply. The power consumption varies with the square of the supply voltage, but is almost independent of temperature and of the device speed grade.

To calculate total clock power, you must know N (the number of flip-flops driven by the clock) and you must estimate V (the number of vertical half-length Longlines used for distributing the clock). A reasonable estimate is that V is the square root of N.

The total power consumed by one global clock is thus: $P = f \cdot (A + B \cdot \sqrt{N} + C \cdot N)$

For example, a 60 MHz clock driving 300 flip-flops in an XC4036XL consumes:

$60 \cdot (300 + 17 \cdot 50 + 300 \cdot 8)\mu W =$

$60 \cdot (300 + 850 + 2400)\mu W = 213\ mW$

Output Power Due to Charging Capacitive Loads

The following estimates assume an internal 10 pF pin capacitance.

- One output driving a 10 pF external load:
  0.2 mW/MHz =
  0.1 mW per million transitions per second
- One output driving a 50 pF load:
  0.6 mW/MHz =
  0.3 mW per million transitions per second.

Note*: Clock frequency can be a misleading way to measure logic activity; counting all transitions avoids this ambiguity.*

Logic and Interconnect Power

- One internal flip-flop driving nothing but its neighboring CLB:
  0.08 mW per million transitions per second.
- One internal flip-flop driving nine loads (very high fan-out):
  0.16 mW per million transitions per second.

Conclusion

This information allows you to estimate device power consumption. The fundamental difficulty is finding the toggle frequency of internal nodes, which requires you to know the statistical behavior of all system inputs to the chip, not just the clock rate. Some estimates assume that 12.5% of the internal flip-flops toggle at the clock rate. However, this is a gross oversimplification, based on the behavior of 16-bit counters. In real designs, the average activity can be significantly lower or higher than 12.5%. ◆

Table 1 -
Clock Power Consumption in µW/MHz

Device	Back-bone	per Vertical	per Flip-Flop
XC4005XL	120	19	8
XC4010XL	170	28	8
XC4013XL	200	33	8
XC4020XL	230	39	8
XC4028XL	270	44	8
XC4036XL	300	50	8
XC4044XL	330	56	8
XC4052XL	370	61	8
XC4062XL	400	67	8
XC4085XL	470	78	8