FPGAs, Power and Packages

By BRADLY FAWCETT ◆ Editor

As programmable logic suppliers accelerate their use of advanced deep-submicron process technologies, the performance and density capabilities of FPGAs continues to increase dramatically. System designers can now take advantage of programmable logic devices exceeding 100,000 logic gates and supporting system clock rates approaching 100 MHz.

In general, the CMOS technology used to produce FPGAs is a low-power technology. However, given the density and performance levels of leading-edge FPGA devices, power consumption issues can no longer be ignored during high-density FPGA design. In the past, the availability of architectural resources (such as logic blocks and interconnect routing) and the inherent delays of the various logic elements and routing switches were almost always the limiting factors in determining device utilization levels and system speed. Now, power consumption can be the limiting factor. In other words, a designer might not be able to use all the available logic blocks and run the design as fast as possible without risking reliability problems due to overheating the devices.

As well as affecting the maximum possible density and performance, the power characteristics of FPGA devices directly affect packaging (and, therefore, component costs) and device reliability. Junction temperatures within a device are a function of power consumption and the thermal resistance of the package (θ_{JA}). Overall device reliability decreases exponentially as junction temperature increases. In general, junction temperatures need to stay below 125° C for plastic packages and 150° C for ceramic packages.

Several factors determine the power consumption within an FPGA, including the supply voltage, the architecture of the device, system performance (switching frequency), and device utilization (the number of interconnects and logic elements used and the percentage of these that switch at a given time).

As with most CMOS devices, the operating power consumption of an FPGA is almost exclusively dynamic, and varies with the square of the supply voltage. Thus, using FPGAs based on the 3.3V power standard, as opposed to the 5V standard, greatly reduces device power requirements. For a given circuit and clock speed, just reducing the supply voltage from 5V to 3.3V decreases operating power consumption by 56%. (The move to lower supply voltages is largely driven by the fact that the ever-shrinking transistors within a submicron device cannot withstand high voltages; however, even if this was not the case, the industry would be driven to lower supply voltages due to device power dissipation issues alone.)

Low-Power Architectures

The architectures of Xilinx high-density FPGAs — specifically the XC4000E, XC4000EX, and XC4000XL families — have been designed to minimize power consumption. For example, the patented segmented-interconnect architecture minimizes the lengths of metal traces, thereby preventing unnecessary interconnect capacitance from slowing device operation and causing extra power dissipation. The extra buffering that was added to the long lines and quad lines when adapting the original XC4000 architecture to create the new XC4000EX and XC4000XL series devices further minimizes interconnect capacitances. As a result, these devices can be fully utilized and operated with high system clock frequencies, even when using plastic packages.

> *"...power consumption issues can no longer be ignored during high-density FPGA design."*

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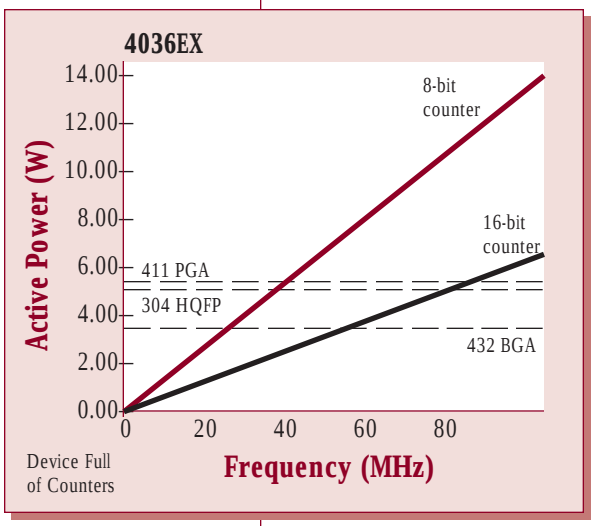
For example, the figure shows the power consumption of an XC4036EX device (a 5V FPGA) when the entire device is filled with 8-bit and 16-bit counters. (In an 8-bit counter, 25% of the flip-flops toggle each clock period, while in a 16-bit counter 12.5% of the flip-flops toggle; thus, the power consumption with the 8-bit counter benchmark is about twice that of the 16-bit counter.) The horizontal lines on the graph correspond to the maximum power dissipation recommended for various package types (without heat sinks or fans). Thus, it is safe to operate the full XC4036EX device in a low-cost HQFP plastic package at speeds up to 70 MHz without requiring heat sinks or fans.

In contrast, some other vendors' high-density FPGAs have interconnect structures based on a multiplicity of long metal traces. The high-speed switching of these long traces, with their inherently larger capacitance, results in considerably higher power consumption. As a result, while the data sheets offered by these vendors boast of high densities and performance rates, these rates can only be reliably sustained by using expensive ceramic packages (and even then often require the further expense of heat sinks and fans). For example, one competitor's device, with a density roughly equivalent to the XC4036EX, was benchmarked using the same methodology as described above. Due to power dissipation limits, it can be run only at speeds below 18 MHz in plastic packages, and at speeds below 35 MHz in ceramic packages; at any higher performance level, heat sinks and fans will be needed.



Thus, users of high-density FPGAs must be careful not to fall victim to "bait and switch" tactics, wherein a designer is enticed to select a high-density FPGA based on performance claims and the price of plastic-packaged parts, only to later discover that power consumption considerations dictate the use of a more expensive package and/or slower speed operation.

Estimating/Minimizing Consumption

Unfortunately, power consumption within an FPGA is design-dependent and can be difficult to calculate prior to implementing the design. Charts provided in Xilinx data sheets provide dynamic power consumption values for typical design elements (for example, the power consumption of one XC4000E CLB flip-flop driving its neighbor and nine lines of interconnect is 0.2mW per million transitions per second); these can be used to derive useful power consumption estimates, but require the designer to estimate the average percentage of nodes in the FPGA design that switch with each clock transition. In any event, it is highly-recommended that users of high-density FPGAs always measure device power consumption (usually by measuring the total I_{CC} current at actual system frequency) upon completion of a design to insure that the right package and cooling methods are being employed.

Some design techniques can be employed to minimize FPGA power consumption/heat (*see* XBRF014). As mentioned earlier, users of high-density, high-performance devices should strongly consider the use of FPGAs based on the 3.3V supply voltage standard, such as the XC4000XL series. Most power dissipation is produced by external capacitive loads on output buffers, so those loads should be minimized and outputs should be switched as infrequently as possible. Similarly, use clock enables to switch off inactive portions of circuits, preventing internal nodes from toggling unnecessarily. Use the place and route tools to maximize the performance of the design, even if the resulting performance far exceeds requirements. Circuits that are able to run faster can do so because of lower routing capacitance; consequently, they dissipate less power at any given clock frequency. ◆