Getting to the Core

By BRADLY FAWCETT ◆ Editor

Continuing improvements to both fabrication processes and device architectures have led to dramatic increases in FPGA capacity and performance, as evidenced by the new XC4000EX family devices. Taking advantage of these increasing capabilities can pose formidable challenges to the user — challenges that cannot always be met by traditional gate-level design techniques, or even HDLs and synthesis-based design. For many users, reusable intellectual property in the form of design "cores" are becoming a key tool in meeting the twin challenges of increasing design complexity and shorter development cycles.

Simply put, cores are complex, pre-designed and reusable functional blocks, typically hundreds to thousands of gates in size, that can be included as part of a larger FPGA design. Cores can be developed internally (for example, re-used portions of previous-generation designs) or purchased as intellectual property from the FPGA vendor or a third-party provider.

The main benefit of cores is the decreased development time and effort associated with using a pre-designed, proven function. Designers can focus their efforts on the proprietary portions of their designs, rather than "re-inventing" a standard function.

Xilinx is committed to the development of a broad selection of cores optimized for use in Xilinx devices. We are fulfilling that commitment in two ways — through the internal development of our own core products, called LogiCORE™ modules, and by partnering with leading third-party core developers through the Xilinx AllianceCORE™ program. The goal is to allow Xilinx FPGA users to act as system integrators, easily combining proven functional blocks with the proprietary logic of the particular application.

To date, the Xilinx LogiCORE PCI Interface has been the most-successful core-based product in the programmable logic industry. With its combination of logic complexity and strict performance requirements, the PCI interface also is one of the most-challenging designs ever to be placed in an FPGA core. We are now using the considerable experience that we gained in developing, selling, and servicing the PCI interface to improve future LogiCORE products and shape our relationships with third-party core developers.

Two of the most-important lessons that we learned are (1) cores should be fully-optimized for the target FPGA architecture, and (2) cores must be delivered to the user as part of a complete product solution.

Some third-party ASIC core vendors are seeking to expand their potential market by re-targeting their "generic" HDL code to various FPGAs. However, with such an HDL-based core, there is little guarantee that the physical implementation will be optimal for the target FPGA architecture. The utilization levels and performance will vary dependent on the efficiency of the synthesis tools and how the core is combined with adjacent logic. The time and effort spent in overcoming these problems can quickly eliminate the time-to-market advantage that initially motivated the use of a core.

In contrast, cores optimized for the target FPGA can use all the available features of the architecture, such as dedicated arithmetic carry logic, internal three-state buffers, and on-chip memory, to achieve optimal logic utilization. Placement and timing constraints, used in conjunction with re-entrant, timing-driven 'place and route' tools, result in predictable and optimized performance levels.

However, there is much more to delivering a core-based solution than just supplying the

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core's design netlist. Potential users should also consider three other main factors that lead to a "complete" solution: silicon, software, and service.

Core-based designs are most appropriate for high-density FPGAs with a rich feature set. FPGA device features such as flexible clocking, numerous and flexible output enables, on-chip memory capability, and on-chip three-state bussing are critical to the implementation of system-level solutions. Broad product families, such as the Xilinx XC4000 series, allow the choice of the most-appropriate device for a given application.

The FPGA development environment must support the appropriate design entry, synthesis, implementation, and verification tools needed for the particular core design. The methodology and tools used to pre-define the implementation of critical paths, such as placement and timing constraint files or guide designs, should be well-understood. Where appropriate, simulation models and test benches should be part of the package supplied to the user, thereby facilitating the verification of the completed design. System software and prototyping equipment also may be required to ease the rapid integration of a core into a complete design.

To ensure the productivity gains that motivated the use of a core, extensive documentation and application support must be available. Of course, the degree of support required for core integration is often proportional to the complexity and flexibility of the core.

Recognizing these needs, the LogiCORE and AllianceCORE programs are emphasizing quality over quantity. For example, we are taking an active role in working with our AllianceCORE partners in the process of "productizing" their cores. A core must meet a minimum set of criteria before it can receive the AllianceCORE label, in terms of "sensibility," format, and completeness.

First, the core must "make sense" — it must provide value over an ASIC or standard product version of the same function, and be cost-effective when implemented in a Xilinx device.

We are not interested in promoting generic, synthesizable functions as AllianceCORE products. The core must be optimized for the target Xilinx FPGA architecture and be delivered as a parametizable "black box" that allows needed customization in critical areas. Timing-critical cores designed to adhere to an industry standard (such as PCI and USB bus interfaces) must be supplied with the appropriate constraints files in order to guarantee functionality and compliance.

The core must be packaged as part of a complete product, including adequate documentation, the availability of technical support, and, where appropriate, additional elements such as test benches, simulation models, and prototyping equipment.

Xilinx recently announced the availability of the first AllianceCORE products, USB modules from CAE/Inventra, and PCMCIA modules from Mobile Media Research *(see page 17)*. It is notable that their offerings include important system integration tools such as simulation models and prototyping boards. The chart on page 17 lists the partners that are currently developing products under the AllianceCORE program; expect future additions and deletions to this list as we discover which providers can meet our stringent quality criteria.

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Of course, this emphasis on complete, optimized solutions and our high level of involvement will limit the number of partners that we can work with at a given time and, subsequently, the number of available AllianceCORE products. Again, the intention is to provide our users with complete solutions that preserve the value of using Xilinx programmable logic devices, as opposed to just filling pages in a catalog of products by promoting the use of generic cores developed for other technologies. ◆