XCELL

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THE QUARTERLY JOURNAL FOR XILINX PROGRAMMABLE LOGIC USERS

XILINX®

The Programmable Logic Company℠

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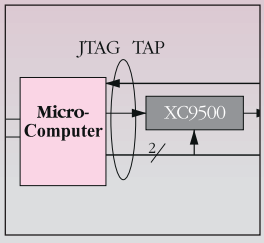

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FROM THE FAWCETT

PLD Capacity & 'Gate Counting'

By BRADLY FAWCETT ◆ Editor

Every user of programmable logic at some point faces the question, "How large a device will I require to fit my design?"

One of the most difficult problems facing those of us who make, market and sell programmable logic devices is establishing meaningful capacity metrics for our devices. We would like to supply potential users with metrics that provide an accurate indication of the amount of logic that can be implemented within a given CPLD or FPGA device, and, at the same time, reflect the relative capacity of our devices compared to other manufacturers' competing products. Unfortunately, these two goals are often at odds with one another. In fact, a look at the density claims that I see in some PLD advertisements these days reminds me of the old saying that there are three types of falsehoods - lies, damned lies and statistics.

Of course, what is a problem for us is also a problem for potential programmable logic users, who must sift through the competing claims of the various vendors and try to select the most cost-effective solution for their application.

At the root of the problem is the multiplicity of available programmable logic architectures. Since each family of devices tends to have a unique architecture for its logic resources, direct comparisons, such as merely counting the number of available logic blocks or macrocells, are not always sufficient. (However, in some instances, direct comparisons of available resources probably could be used a bit more often than I think they are).

Most vendors, including Xilinx, describe device capacities in terms of "gate counts" — the number of 2-input NAND gates that would be required to implement the same function. This metric has the advantage of being familiar to ASIC designers and, in theory, allows the comparison of programmable logic device capacities to those of traditional, mask-programmed gate arrays.

But FPGA and CPLD devices do not consist of arrays of 2-input NAND gates; they have structures such as look-up tables, multiplexers and flip-flops for implementing logic functions. Thus, "counting gates" is far from an exact science; different vendors apply varying methodologies to determine gate counts.

All too often, gate counting becomes a game of "one-upmanship" among competing vendors. In fact, it seems to me that some marketeers decide what gate capacity they want to claim, and then design their metrics to reach that number. For example, in ancient times (that is, a couple of years ago), one of our competitors was bringing a large FPGA to market with a claimed capacity of 22,000 gates; the device had even been named to reflect that claim. Then Xilinx announced and started sampling the "25,000 gate" XC4025. Suddenly, the competing device somehow "grew" an additional 4,000 gates and was renamed and brought to market as a "26,000 gate" FPGA.

With the advent of FPGAs like the XC4000 Series that offer on-chip memory as well as logic resources, the issue is further complicated by the use of "memory gates" in addition to "logic gates". Each bit of memory counts as four gates. This factor can quickly inflate gate counts. For example, a single 4-input look-up table (LUT)

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GUEST EDITORIAL

One Size Does Not Fit All:

Development System Products & Strategies

by KENN PERRY ◆ *Director of Software Marketing*

One design tool configuration cannot meet the needs of all programmable logic designers. Overall, today's designers are looking for top-down, language-driven design support that enables system-level integration within their programmable logic design methodologies. However, user requirements and expectations vary considerably, dependent on their design methodologies, cost considerations and time-to-market pressures.

Xilinx is addressing the needs of the low-, mid- and high-density classes of designers with three XACT*step*™ software solutions: the Foundation Series™, Alliance Series™ and System Level Integration (SLI)™ options. Thus, Xilinx users can choose between a complete, tightly integrated design system supporting industry-leading HDLs, schematic capture and simulation (the Foundation Series), or the integration of Xilinx implementation tools into their chosen EDA environment, leveraging defacto industry standards (the Alliance Series). Additionally, comprehensive system-level design is supported by SLI options, such as LogiCore™ modules, that enable users to achieve high density and performance while greatly reducing time-to-market. These products are available today.

> *"Xilinx is addressing the needs of the low-, mid- and high-density classes of designers."*

Foundation Series

Designers of low-density FPGAs and CPLDs, the largest group of users, typically are cost-sensitive and prefer easy-to-use, push-button, integrated software solutions that support both schematic and language-based entry methods. Intolerant of delays, defects or risks, these users desire a complete, "shrink-wrapped" solution. The Foundation Series solutions provide the technological "foundation" upon which support for higher-density Xilinx devices can be built.

Xilinx is the first programmable logic vendor to offer a low-cost, shrink-wrapped solution that integrates schematic entry, HDL synthesis and gate-level simulation for both CPLDs and FPGAs. The goal of the Foundation Series solution is to provide an environment where the user can open the box, install the software, get up-to-speed quickly and complete designs successfully without assistance — although support is readily available if needed. From a single environment, users have access to HDL synthesis (VHDL and ABEL initially), schematic entry, gate simulation and core implementation tools, making PLD development simple and easy without compromising design flexibility or performance. The Xilinx continuum of software functionality and device technology enables users to expand their Foundation Series system capabilities with the changing demands of their design requirements.

Alliance Series and the Alliance Program

The mainstream segment of programmable logic, encompassing mid-range density users (10K to 15K gates), is the fastest growing segment in the programmable logic market. With decreasing market windows and increasing technology demands, main-

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Continued from the previous page

stream designers have critical business issues to solve. To remain competitive in today's marketplace, they have developed their own design methodologies employing tools and technology provided by EDA vendors. They prefer to leverage their previous investments and experiences by using the appropriate combination of tools from their EDA and programmable logic suppliers. Therefore, it is critical that their programmable logic design solutions are tightly-integrated with their established methodologies and support industry standards. The Alliance Series, based on the industry's most powerful set of third-party EDA integration solutions and partnerships, provides the benefits of an "open system". Alliance Series products support industry standard design interfaces, such as EDIF, VHDL, Verilog and LPM, and allow designers to create and verify designs in their chosen third-party EDA environment.

"The upcoming upgrade to the XACTstep software platform incorporates our next-generation core software."

Through the Xilinx Alliance Program, integrated design solutions for the design of Xilinx devices are available from a broad array of third-party EDA suppliers. The Alliance Program is structured to assure that Xilinx users have access to the widest variety of high-quality third-party tools, certified to work with Xilinx products. Currently, the Xilinx Alliance Program includes more than 100 partners, representing over 160 products, who have been selected for their contribution to Xilinx development and their responsiveness to customer needs. The Alliance Program supports these partners with technical information and assistance on an ongoing basis and, in turn, the partners provide Xilinx with input regarding product interfaces and directions.

System Level Integration (SLI)

High-density users, typically the early adopters, require leading-edge technology to help solve their very large, complex and performance-driven design problems. These users focus on advanced functionality and need the newest, most advanced technologies. As programmable logic devices increase in density, designing at the gate level is no longer a realistic approach.

SLI tools go far beyond just delivering support for higher-gate-count designs. Xilinx SLI options facilitate the design of system-level functions in high-density, high-performance programmable logic devices. Intended as "add-ons" to the Alliance and Foundation Series products, current SLI tools include the LogiCore modules. LogiCore modules are fully-verified, drop-in system level modules, such as target and initiator PCI bus interfaces. These tools can dramatically shorten design cycles and facilitate complex, system-level integration within programmable logic devices.

Next Generation Core Software Platform

The upcoming upgrade to the XACT*step* software platform incorporates our next-generation core software environment, leveraging the industry-leading technologies from the merger between Xilinx and NeoCAD. This new core technology includes timing-driven optimization, mapping, FPGA placement and routing and CPLD fitting algorithms; it will be the software platform for all existing and future Xilinx IC product development and support. This new release will still incorporate many aspects of the popular XACT*step* version 6 software environment, providing users with an easy migration path and protecting previous tool and training investments.

In summary, upcoming releases of the XACT*step* product series are being developed to include the latest technological advancements, including enhanced SLI product offerings, value-added EDA technologies and additional Xilinx device support.. These advancements will deliver increased ease-of-use benefits for rapid design implementation flows, enhanced integration and high-quality results. In addition, Xilinx integrated educational tools will round out the technologies being delivered.

Future programmable logic design solutions from Xilinx will place more emphasis on making users of programmable logic better overall system designers, as well as ensuring rapid design implementation into Xilinx silicon. ◆

Continued from page 2

can account for anywhere from one to nine "gates" when used to implement a logic function, depending on the type of function that is implemented. However, when that same look-up table is used as 16 bits of ROM or RAM memory, it now is implementing 16 x 4 = 64 "equivalent gates." Thus, FPGA gate counts rapidly inflate when the capacity metric assumes a significant amount of on-chip memory usage; it's important to know what assumptions about memory usage apply to a claimed gate density in these devices.

For example, the device names in the XC4000E and XC4000EX families are based on our "maximum logic gates" metric — a measure of logic capacity only that assumes no memory usage. However, a major competitor has named its competing family based on a metric they call "typical gates" that includes both types of gates, and further assumes up to 35% on-chip memory utilization. Superficially, based on the device names alone, it appears that their devices are much larger than ours. However, even a cursory examination of device resources reveals a quite different story. For example, their "20,000-gate" device includes 1,152 4-input look-up tables, 1,344 registers and a maximum memory capacity of 12K bits. In contrast, the Xilinx "13,000-gate" XC4013E includes 1,152 4-input lookup tables, an additional 576 3-input lookup tables, 1,536 registers, and a maximum memory capacity of 18K bits.

This is not to say that Xilinx has not, at times, been guilty of "gate-inflation.". However, we have been more consistent over the years than most of our competitors. We recently reviewed and slightly revised our methodology for assigning gate counts for XC4000 Series and XC5200 family FPGAs. The results of that effort can be seen in the product specifications included in our latest data book. Xilinx application note #059, "Gate Count Capacity Metrics for FPGAs," explains our capacity metrics and the methodology used to obtain them; the application note can be viewed at our WebLINX web site (www.xilinx.com).

Besides being subject to statistical manipulation, gate counts used as capacity metrics suffer from another severe drawback – they usually take only logic block and on-chip memory resources into account. Modern FPGAs include a host of other important features. For example, architectural features in the XC4000 Series that are not reflected in our capacity metrics include wide-edge decoders, dedicated arithmetic carry logic, registers and logic in the I/O blocks, global buffers and clock distribution networks, and internal three-state buffers. These important features can considerably boost the capacity and system integration capabilities of these devices.

"Take the time to examine and compare all the internal resources of the various devices being considered for a design."

Experienced CPLD and FPGA users realize that there can be considerable variation in the logic capacity of a given device dependent on factors such as how well the application's logic functions match the target device's architecture, the efficiency of the development tools, and the knowledge and skill of the designer. So, my advice is to apply a healthy dose of skepticism to CPLD and FPGA manufacturers' gate count metrics (yes, even ours). Examine the assumptions behind the "gate counting methodology." Better yet, take the time to examine and compare all the internal resources of the various devices being considered for a design. Fortunately, with a little experience, most designers can get a good intuitive feel for the logic capacity of the devices that they use. ◆

Swiss Engineers Use FPGAs to Link

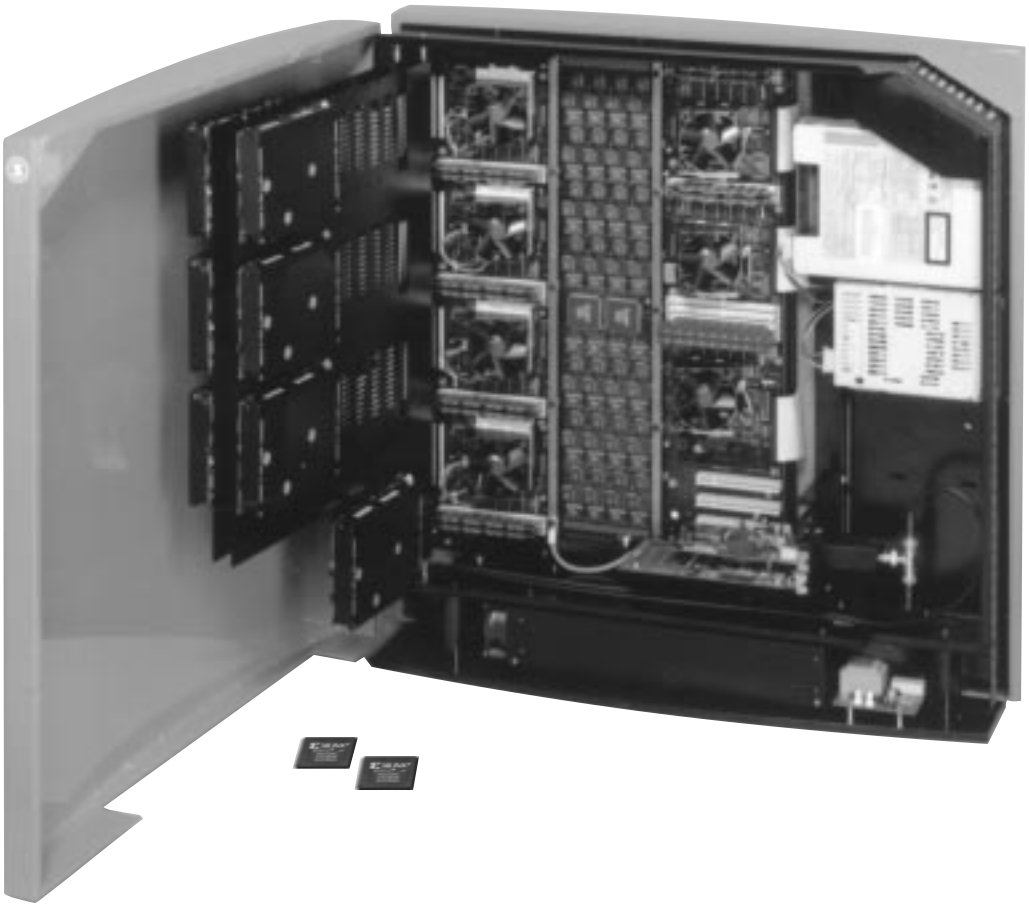
Designers at Supercomputing Systems AG (Zürich, Switzerland) took a novel approach in designing the GigaBooster parallel computer system — combining multiple processing elements built from standard components with a fast, low-latency communication scheme implemented in hardware. To implement the critical communications control logic, they chose the world's leading FPGA family — the XC4000 Series.

> *"To implement the critical communications control logic, they chose the world's leading FPGA family — the XC4000 Series."*

Based on the "alpha7," a prototype system designed at the electronics laboratory of the ETH (the Swiss Federal Institute of Technology), the GigaBooster is a parallel computer containing seven individual processing elements (PEs) on a single board. Each PE is constructed from a DECchip 21066 Alpha processor, one Mbyte of cache memory, up to 128 Mbytes of DRAM memory (256 Mbytes in the "root" PE), a SCSI controller, and two special registers that control clock, reset, interrupts and similar functions. Each PE is accompanied by two banks of FIFO buffers dedicated to interprocessor communication and connected to a common 72-bit bus. All the special registers and FIFO buffers are controlled by a central communications controller realized within three XC4013 FPGAs. All the PEs run the Digital UNIX operating system, providing access to over 3000 applications.

A new communications protocol called Intelligent Communication was developed to provide fast communications and communication control, enabling the system to take full advantage of the processing power in each PE. This protocol, implemented directly in hardware using the FPGAs, allows fast, low-latency data exchange among the processors, and a programming model with simple and efficient code. The in-system programmable nature of the XC4013 FPGAs was key to the development of this protocol; during development, various approaches were tested and compared simply by reconfiguring the FPGA devices.

In the original alpha7 system design, the communications controller was squeezed into just two XC4013 devices.



Supercomputing Processors

Supercomputing Systems

In the GigaBooster system, the controller was redesigned into three XC4013 FPGAs to allow room for expansion. One FPGA holds several small state machines, an abundance of control registers, and other glue and interface logic; this design uses about half of the available logic blocks, but all of the I/O pins. The other two FPGAs implement the logic directly involved in the gathering and redistribution of data from the processing elements, including a 42-bit counter and a large register/comparator file for each PE. The first of these FPGAs is more than 90% utilized, and connects to five of the processing elements.

About 40% of the second FPGA contains the identical logic for the remaining two PEs. Additional logic is dedicated to monitoring the communications behavior of applications running on the system, and the remainder of this FPGA can be used to support a module slot for an additional processing element or an interface to an optical high-speed network. The XC4000 architecture's built-in carry logic was critical to attaining acceptable performance from the large counters and comparators in this implementation. The design runs at 20 MHz.

The FPGA designs were developed on a Sun workstation using Viewlogic's Powerview tools and the XACT® development system. This combination "forms a very comfortable development environment," according to Hansruedi Vonder Müehll, the design engineer at the Swiss Federal Institute of Technology who was responsible for the original design of the communications controller. Some floorplanning was required, and both functional and timing simulation were used to debug and verify system operation.

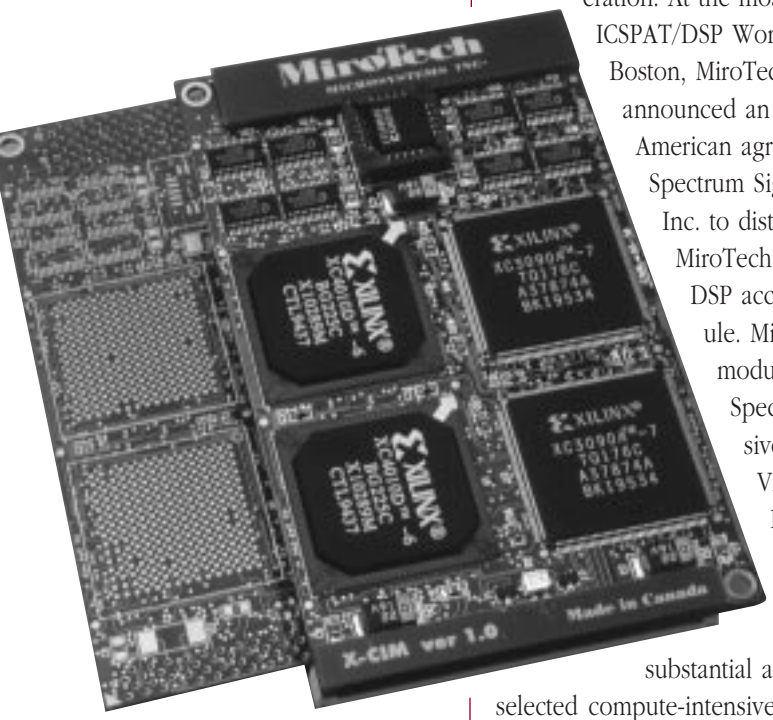
The FPGA's readback capability also was exploited during system debug, and is now used to "dump" the state of the communications controller in the event of a communication failure. Using readback, the values of internal counters, registers, and state machines can be extracted and analyzed.

In summary, the use of reconfigurable XC4013 FPGAs was key to the implementation of interprocessor communication protocols directly in hardware, as opposed to the more-traditional software approaches. The resulting high-performance communications management allows the system to tap the full processing power of each of its Alpha processors, delivering 1.6 Gigaflops of peak performance in an affordable and compact system. ◆

"The use of reconfigurable XC4013 FPGAs was key to the implementation of interprocessor communication protocols direclty in the hardware."

MiroTech Microsystems:
Real-Time Reconfigurability for DSP Acceleration

MiroTech
The Acceleration Company



Our congratulations to the development team at MiroTech Microsystems Inc. (Montreal, Canada). MiroTech Microsystems has released a commercial product that uses reconfigurable computing to advance the state-of-the-art for DSP acceleration. At the most recent ICSPAT/DSP World Exposition in Boston, MiroTech Microsystems announced an exclusive North American agreement with Spectrum Signal Processing Inc. to distribute MiroTech's FPGA-based DSP acceleration module. MiroTech's X-CIM module complements Spectrum's extensive PCI, VXI and VME C4x-based DSP product line. Together these products provide substantial acceleration for selected compute-intensive, high-performance applications.

X-CIM is an FPGA-based reconfigurable computer in a TIM form factor that is fully-compliant with Texas Instruments' TMS320C40 DSP processor. The module features 80 Mbytes/s communication port bandwidth, 30 ms on-the-fly reconfigurability, and hardware-implemented parallel processing. It's a sophisticated, highly portable architecture based on Xilinx reconfigurable FPGAs and banks of high-speed RAM.

As the tendency towards more complex DSP systems continues to grow, designers are constantly seeking new ways to reach higher performance and to unravel bottlenecks while reducing development costs. "What is unique with our X-CIM is its implementation in an IEEE standard and off-the-shelf product packaging," noted MiroTech President and CEO Pierre Popovic. "The X-CIM module can deliver acceleration up to 100 times that of a general-purpose DSP processor for highly repetitive 'inner loops' within algorithms."

The marriage of the X-CIM module with Spectrum's products allows the design of very compute-intensive systems while staying within Spectrum's C40 environment and DSP development tools. X-CIM modules are supported by a comprehensive suite of software tools referred to as COREKIT. With these tools, developers can transparently accelerate a wide range of DSP functions in applications such as radar, sonar, voice and image processing.

For more information on the X-CIM product line, contact MiroTech Microsystems Inc. at 514-956-0060 or at MiroTech@montreal.com. ◆

The **Xilinx Reconfigurable Computing Developer's Program** is promoting the commercial use of FPGAs in reconfigurable computing applications. These systems add significant value by dynamically changing FPGA designs, in real-time, while the system is operating. Applications that can exploit the benefits of the RC concept include graphics and image processing, audio processing, and data communications.

For more information on the Xilinx Developer's Program and our reconfigurable computing efforts, please see our web site at www.xilinx.com, or call John Watson at 408-879-6584.

Xilinx Joins Virtual Socket Interface Alliance

Last September, a group of more than 35 leading electronics firms announced the formation of the Virtual Socket Interface (VSI) alliance. This open alliance is dedicated to promoting the growth of the system level integration (SLI) chip industry by developing the technical standards required to enable the "mix and match" of system level modules (SLMs). Xilinx has entered the VSI alliance, and is actively participating in standardization efforts affecting programmable logic technologies. Our participation augments our current programs for the development of a diverse set of high-quality SLMs, called LogiCore™ modules, for the various Xilinx FPGA and CPLD families.

The goal is to establish a set of open SLM design interface and productization standards. Through use of the developed standards, design engineers will be able to use SLMs from several sources in the design of highly-integrated programmable logic devices. For example, a designer could construct a system combining SLMs supplied by Xilinx (such as the LogiCore PCI master/slave), SLMs from third-party providers (such as the members of the Xilinx LogiCore Alliance), and reusable modules from his/her previous designs.

SLMs from all sources will be designed to common standards, much like physical components that are mixed-and-matched today on a printed circuit board. These VSI-compliant SLMs can be viewed as "virtual components" that, through common interface standards, fit quickly into "virtual sockets." In order to rapidly provide a solution, the design data standards will be based on open formats commonly supported by all EDA vendors.

High-quality SLMs are a key component for high-performance and high-density programmable logic design. The use of pre-defined and pre-verified SLMs can dramatically reduce system development cost and time, resulting in faster time-to-market and a greater competitive advantage.

For further information about the VSI Alliance, see their web site at www.ipnet.org. For additional information about the LogiCore products and LogiCore Alliance Program, see the WebLINX web site at www.xilinx.com/products/logicore/logicore.htm. ◆

New AppLINX CD-ROM Shipped

An updated AppLINX CD-ROM has been shipped to all registered Xilinx users. The CD contains a complete collection of Xilinx applications and product information. Access to the AppLINX CD is another benefit of maintenance support for the Xilinx development system.

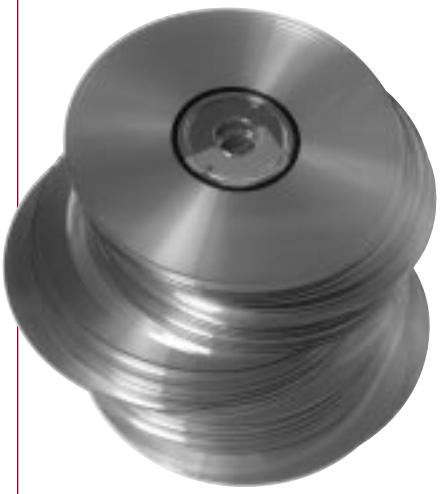
The AppLINX CD-ROM includes:

- Updated September 1996 data book
- All Xilinx application notes and their corresponding design files
- Development system documentation
- The last six issues of the *XCell* journal
- Adobe Acrobat® Reader™ with full content-searching capabilities
- Presentation notes for the Xilinx 1996 Fall Seminar

The AppLINX CD merges the best aspects of the Xilinx WebLINX web site and the Xilinx FTP site. Users with access to an HTML browser can navigate the files quickly and easily off-line, while links are available to find the latest information on-line.

The AppLINX CD will be updated on a regular basis. Make sure you visit the Xilinx WebLINX web site at www.xilinx.com for the latest information.

Regarding the fall seminar, contact your local Xilinx sales office to inquire about a presentation to your company. ◆



New Product Literature

Learn about the newest Xilinx products and services through our extensive library of product literature. The most recent pieces are listed below. To order or to obtain a complete list of all available literature, please contact your local Xilinx sales representative. ◆

TITLE	DESCRIPTION	NUMBER
Corporate		
Product Overview Brochure	Features & Benefits	0010130-05
Software Solutions Brochure	Features & Benefits	0010304

UPCOMING EVENTS

Look for Xilinx technical papers and/or product exhibits at these upcoming industry forums. For further information about any of these conferences, please contact Kathleen Pizzo (Tel: 408-879-5377 FAX: 408-879-4676). ◆

Design SuperCon
Jan. 21–23
Santa Clara, California

ACM/SIGDA 5th International Symposium on FPGAs
Feb. 9–11
Monterey, California

International Integrated Circuits Conference
March 13–14
Beijing, China

International Integrated Circuits Conference
March 17–18
Shanghai, China

European Design and Test Conference
March 17–20
Paris, France

Intellectual Property in Electronics Seminar
March 17–18
Santa Clara, California

Semiconductor Solutions
March 18–20
Birmingham,
United Kingdom

FINANCIAL RESULTS

A Difficult Quarter

For the first time, Xilinx Inc. quarterly sales revenues declined from both the prior quarter and the year ago period. Revenues for the September-ending quarter were $130.6 million, a decrease of 13.1% from the immediately preceding quarter and 7.5% from the same quarter one year ago.

"The September quarter was a difficult quarter for the overall programmable logic industry and Xilinx in particular," stated CEO Wim Roelandts. "We believe this revenue shortfall can be attributed to several factors, including increased pressure from selected customers to reduce their own inventory, a seasonably weaker summer quarter in Europe, and new customer programs that have not ramped up as quickly as initially forecasted."

Roelandts continued, "However, we are encouraged by the nearly 1,400 new software seats that we sold this quarter, 70% of which are versions of our new, shrink-wrapped, low-cost Foundation™ software," Roelandts added. "We are also optimistic that our new XC9500 and XC4000EX families will provide meaningful contributions to revenues before our fiscal year end."

Xilinx Inc. stock is traded on NASDAQ under the symbol XLNX. ◆

WebLINX and *Smart*Search Agents Keep You Up-to-Date

WebLINX (www.xilinx.com) has become a popular stopping place on the information superhighway. Based on recent traffic reports, more than 5,000 people visit the Xilinx World Wide Web site each week. Some of the most popular areas of our web include *Smart*Search, Product Information pages, Application Notes and the Data Book page.

We're constantly adding new information to WebLINX. In fact, over the last few months we have added many new application notes and application briefs to the site, as listed here.

If you are interested in keeping up-to-date with new technical information being posted to WebLINX, then *Smart*Search Agents are for you. A *Smart*Search Agent will automatically notify you via e-mail when a document of interest to you is posted to any of the 50 or so sites that we index. For example, you can create a *Smart*Search Agent that will alert you regarding any new application notes posted to the Xilinx site by following these steps:

1. Using your browser, go to www.xilinx.com
2. Click on the "Register Now for Agents!" hyperlink near the bottom of the page.
3. Click on the "register" hyperlink
4. Fill out the registration questionnaire.
5. After you have successfully registered for Agents, go to *Smart*Search by clicking on the *Smart*Search logo or text at the bottom of the page.
6. Click on the "Xilinx Only" link.
7. Leave the text box blank but select the "application notes" check box.
8. Click on the Start Search button. On the results page, in the upper right corner is a text box with the label "Agent Name:"
9. Type "Xilinx Application Notes" into the agent name box and click on the Create Agent button.

That's it! This will create an agent that will notify you whenever Xilinx posts a new application note to the site. Remember that you can create an agent for anything you can search for, and they are not limited to the Xilinx site. ◆

The following XAPP application notes and XBRF application briefs have recently been added to WebLINX. You can find these by first going to the application notes page and selecting XAPP application notes or application briefs.

- XAPP051 Synchronous/Asynchronous FIFOs
- XAPP052 Efficient Shift Registers, LFSR Counters, etc.
- XAPP053 Implementing FIFOs in XC4000 Series RAM
- XAPP054 Constant Coefficient Multipliers for the XC4000E
- XAPP055 Block Adaptive Filter
- XAPP056 System Design with New XC4000EX I/O Features
- XAPP057 Using Select-RAM Memory in XC4000 Series FPGAs
- XAPP058 XC9500 In-System Programming Using an 8051 Microcontroller
- XAPP059 Gate Count Capacity Metrics for FPGAs
- XAPP060 Design Migration from XC4000 to XC5200
- XAPP062 Design Migration from XC4000 to XC4000E
- XAPP063 Interfacing XC6200 to Microprocessors (MC68020 Example)
- XAPP064 Interfacing XC6200 to Microprocessors (TMS320C50 Example)
- XAPP065 XC4000 Series Edge-Triggered and Dual-Port RAM Capability

In addition, the following application notes have been updated:

- XAPP013 Using the Dedicated Carry Logic in XC4000E
- XAPP018 Estimating the Performance of XC4000E Adders and Counters

Xilinx Application Briefs are technical papers describing the advantages of Xilinx products, especially versus alternative solutions:

- XBRF001 XC4000E Select-RAM: Flexibility with Speed
- XBRF002 XC4000E Low Power Consumption: At High Speed
- XBRF003 XC4000E Select-RAM: Maximum Configurability
- XBRF005 XC4000EX Routing: A Comparison with XC4000E and ORCA
- XBRF006 PLL Design Techniques and Usage in FPGA Design
- XBRF007 XC4000-Series FPGAs: The Best Choice for Delivering Logic Cores
- XBRF009 XC9500 Pin Locking Capability and Benchmarks

One-Day VHDL Seminar Now Available

Xilinx is sponsoring a series of one-day introductory VHDL seminars conducted by qualified instructors from Esperan Inc. Esperan specializes in technical training and has educated thousands of VHDL users since 1992. This one-day course, a must for new users, emphasizes the basics of the VHDL language.

A full day of lecture and hands-on labs, the seminar uses the VHDL tool offered by Xilinx in the Foundation Series™. The tuition fee is $99. Feedback from participants has been extremely positive; extra seminars have been added to the schedule to meet demand.

VHDL SEMINAR ATTENDEES LEARN:

- The benefits of using VHDL design to reduce time-to-market
- VHDL's general structure and syntax
- How to write good VHDL code that will synthesize efficiently
- How to effectively target CPLD and FPGA architectures
- How to implement state machines, combinatorial logic and arithmetic functions in VHDL

Each attendee receives an evaluation kit of the Xilinx software. This provides ample opportunity to practice the skills and knowledge obtained at the seminar. The kit includes the Foundation Series software, an integrated tool set of schematic entry, VHDL synthesis, functional and timing simulation and design implementation tools – everything needed to create an entire design.

Xilinx, its distributors and representatives, together with Esperan, are sponsoring these seminars. Contact your local Xilinx representative to inquire about VHDL training seminars in your area.

In related news, electronics distributors Hamilton Hallmark, Marshall and Insight are in the process of creating VHDL workshops as well. In each case, Xilinx FPGA devices and the Foundation Series tools have been selected for use in the lab exercises. ◆

First Hands-On Workshop on Reconfigurable Computing

The Xilinx University Program (XUP) has had an active training schedule with nine recent workshops in four countries. XUP workshops are designed to train university instructors on the basics of using programmable logic for undergraduate courses, graduate courses and research.

In addition to the standard workshops, and in response to a growing interest in dynamically-reconfigurable logic, a unique, leading-edge workshop was held at Cornell University (Ithaca, NY).

The Cornell workshop was the first to examine both the hardware and software issues associated with dynamically-reconfigurable computing, including hands-on laboratory exercises. Participating lecturers included representatives from Xilinx, the Virginia Institute of Technology, ETZ Zurich, Cornell University, and Imperial College (UK). Mr. Nick Treddinick, an IEEE fellow, presented the keynote address.

Xilinx is committed to addressing the needs of the reconfigurable logic market, and the Xilinx University Program is committed to further academic support of this exciting area of study. Proceedings from the workshop are available to XUP participants, and further information about this workshop and future XUP workshops can be obtained on the web at www.xilinx.com/programs/univ.htm. ◆

Updated Training Courses Available

The basic Xilinx technical training courses have been updated to reflect all the features of the latest development software. XACT*step*™ version 6.0.1 software is fully incorporated into the schematic-based design course. The course examines a complete design scenario for the Foundation Series software user. The updated synthesis-based design course provides VHDL/Verilog designers with an intimate working knowledge of the XACT*step* v5.2.1/6.0.1 synthesis software. Both of these courses are available worldwide.

The current schedule of schematic- and synthesis-based courses, as well as course registration information, can be found at the WebLINX web site (www.xilinx.com). ◆

New XC9500 ISP Products in Volume Production

Four new XC9500 ISP (In-System Programmable) CPLD devices are now in volume production. The XC9536, XC9572, XC95108 and XC95216 CPLDs are ready for designers looking for the best, most-flexible ISP solution. These 36-, 72-, 108- and 216-macrocell devices, respectively, feature fast, guaranteed performance, the industry's best pin-locking architecture, a true JTAG-compliant interface, and advanced flash memory technology with up to 10,000 program/erase cycles. The resulting benefits include reduced overall costs, faster time-to-market and the flexibility needed to make design changes anytime during the product life cycle.

Please contact your local Xilinx sales representative for further technical information, price and availability information, or requests for samples of these new ISP CPLD products. ◆

Feature	XC9536	XC9572	XC95108	XC95216
Macrocells	36	72	108	216
Usable Gates	800	1600	2400	4800
t_{PD} *(ns)*	5/7.5/10/15	7.5/10/15	7.5/10/15	10/15/20
Registers	36	72	108	216
Pin-locking	✓	✓	✓	✓
JTAG (1149.1)	✓	✓	✓	✓
Max. User I/Os	34	72	108	166
Packages	PC44/VQ44	PC84 PQ100/TQ100	PC84 PQ100/TQ100 PQ160	PQ160 HQ208

Five Million and Counting

XC4000 device #5,000,000 shipped in September. The recipient, Acuson Corporation, a manufacturer of medical electronics systems, was featured at a commemoration ceremony.

Since its introduction in the early 1990s, the XC4000 family has quickly grown to become the world's most successful FPGA product line. The addition of XC4000E devices (and now the XC4000EX versions) to the product family have accelerated XC4000 unit shipments since mid-1994, when the family reached the million-unit milestone.

"As medical technology continues to advance at a phenomenal rate, the success of Acuson more and more depends on our ability to design and deliver the best products possible in the shortest amount of time," stated Robert Gallagher, Acuson president. "The XC4000 has greatly contributed to our technological vision and has helped us provide cost-effective solutions for the needs of our dynamic marketplace. We are delighted to share in the XC4000's success." ◆

XC4000EX Family Enters Production

The world's most popular FPGA series just got bigger! Xilinx began shipments of production-qualifed XC4036EX devices in November. The XC4036EX offers 36,000 maximum logic gates and a typical gate range (logic and memory) of 22,000 to 65,000 gates. Planned devices in the XC4000EX family will range from 28,000 to 128,000 logic gates.

The XC4000EX FPGAs contain all the advanced features of the popular XC4000 and XC4000E architectures. However, several significant enhancements to the architecture address the routing, clock distribution, and I/O needs of higher density devices *(See* XCell *#20, page 21).*

Development system software for the XC4000EX family will start shipping in late December. The initial software offering will support Synopsys, Mentor Graphics and Viewlogic EDA environments, as well as workstations from Sun (both SunOS and Solaris) and HP. Please contact your local Xilinx sales representative for the latest availability status. ◆

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Product Obsolescence Policy

During its first 12 years, Xilinx has continued to maintain every component product line it successfully introduced. We take pride in that. However, as processes migrate to smaller geometries with lower costs, and architectures continue to improve, the economics of overlapping products dictates that some product life cycles should end.

We are aware that IC users are very wary of product obsolescence. All too often, products are discontinued as a result of business decisions that do not adequately include the customers' perspective. To ensure that we get it right the first time we discontinue a product, Xilinx has taken a different approach and solicited customer input to assist in designing our product obsolescence program.

Our goal is to provide users with ample notification of product discontinuances and ensure adequate supplies of affected products for as long as possible. The program includes "customer advisory" notices as a preview of future product changes and discontinuances, generous last-time-buy periods to allow ample planning and/or redesign time, and relationships with end-of-life suppliers that ensure product availability beyond the Xilinx last-time-buy and last-time-ship periods.

Xilinx Product Discontinuance Policy — The Xilinx Product Discontinuance Policy addresses two situations—where a replacement device exists (PDN1) and where a replacement **does not** exist (PDN2).

PDN1 — When a form, fit, function replacement exists, the last-time-buy (LTB) period is one year and last-time-ship is 90 days after the LTB period. The one-year period should provide ample time for users to determine if they prefer to exercise a last-time buy or requalify with the replacement device.

PDN2 — When no form fit or function replacement exists, the last-time-buy is two years to allow users the time necessary to completely redesign the board or perform a detailed analysis of LTB requirements.

End-of-Life Supplier — At the end of PDN1 or PDN2, all remaining inventory will be shipped to an end-of-life supplier. The supplier will be able to deliver Xilinx discontinued products to those users that choose not to exercise the last-time-buy option, or have an unexpected need.

In summary, Xilinx has attempted to take a user-sensitive approach to product obsolescence. Early notification, extended last-time-buy periods and the use of end-of-life suppliers give the user a variety of options to explore and ease any problems resulting from a product discontinuance.

Your comments and suggestions regarding this policy are welcome. Please send all comments to Daniel Chan, Xilinx Marketing, at daniel.chan@xilinx.com. ◆

Xilinx Obsolecesnce Policy

	Form, Fit and Function Alternative	Obsolete Ordering Code	Notify to Last Time Buy (LTB)	Last Time Buy (LTB) to Last Time Ship (LTS)	Example
PCN* (Product Change Notice)	Yes	No	Product changes after 90 days†		XC4000 process migration
PDN 1 (Product Discontinuance Notification)	Yes	Yes	1 year	90 days	XC4000A/H discontinuation
PDN 2	No	Yes	2 years	90 days	

**Specification control document (SCD) available to stay with old product for one year.*
†90 days from latter of qualification data or evaluation sample availability.

Xilinx To Discontinue Older XC4000A/H FPGA Devices

Xilinx has announced that it will stop production of two families of field programmable gate arrays devices in 1997 — the XC4000A and the XC4000H families (older variations of the XC4000 Series of products). The XC4000E, XC4000EX and XC4000D families will not be affected.

Users of these devices can replace them with newer Xilinx XC4000E and XC5200 FPGA family products; these newer devices provide footprint-compatible solutions with substantial cost and performance advantages over the older devices.

This marks the first obsolescence of mature Xilinx FPGA devices, and it begins the implementation of one of the industry's most customer-friendly product discontinuation policies. Last-time orders to buy the XC4000A and XC4000H devices will be accepted until September 30, 1997. Last-time shipments will be made until March 31, 1998. ◆

New CPLD Software Updates

New device support and enhancements have been added to the Xilinx XC9500 CPLD software. Both the core fitter and EZTag™ download software have been enhanced to support XC9500 CPLD family designs.

The latest updates feature:

1. JEDEC programming file generation for the newest member of the XC9500 family, the XC9572-7.
2. Refined fitter optimization algorithms for improved fitting efficiency
3. Netlist reader improvements to accept Exemplar™ generated netlists
4. ISP algorithm enhancements
5. Faster download time from a PC

The names of the enhanced fitter and EZTag files:

Platform	Fitter File	EZTag File
PC	FITTERPC.ZIP	EZTAG_PC.ZIP
Sun	FITTERSN.TAR.Z	EZTAG_SN.TAR.Z
HP	FITTERHP.TAR.Z	EZTAG_HP.TAR.Z

The PC files are accessible from the Xilinx BBS and FTP sites:

BBS: Software Help ➡ CPLD Software

FTP: ftp://ftp.xilinx.com/pub/swhelp/cpld

Since the UNIX versions of these files are compressed for the convenience of our workstation users, they are available only on the FTP site. A detailed description of each file is contained in CPLD.LST, also located at these sites. Download these files NOW to take advantage of the industry's best software for the industry's best pin-locking CPLD. ◆

HW-130 Device Programmer Update

We work closely with third-party programmer manufacturers to support our products with standard programmer solutions. Our own HW-130 programmer for Xilinx SPROMs and CPLDs supports system development and low-volume programming requirements.

Updated HW-130 interface software is now available for both PC and workstation platforms (DOS, Windows 3.1, Windows 95, Windows NT, Sun OS, Solaris, HP9000/700 and IBM RS6000 environments). Users can download the files from the bulletin board system, or request the upgrade by contacting a local Xilinx sales representative. The upgrade is free-of-charge to current HW-130 owners.

Programming support for the XC9500 family is available now on the HW-130 for the XC9536 and the XC95108 CPLD devices. The XC9500 family also is supported by BP Microelectronics' and Data I/O's latest updates, available from their bulletin board systems. Several other programmer manufacturers have scheduled XC9500 family support in late 1996 and early 1997. The XC9500 family has been added to the charts located near the back of this newsletter that list programmers supporting Xilinx products. ◆

VITAL Model Support for XC9500 CPLDs

VITAL model support for the XC9500 CPLD family is now available from Topdown Design Solutions. These models allow the designer to generate timing-accurate, gate-level VHDL from Xilinx XNF files. VBAK/VITAL models are designed to work with the Model Technology V-System simulator. These models are designed, implemented, sold and supported by Topdown Systems.

For additional information, contact Topdown Systems by telephone at 800-438-8435 or by electronic mail at info@topdown.com. Topdown Systems' web site is located at www.topdown.com. ◆

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Implementing Median Filters in XC4000E FPGAs

by JOHN L. SMITH,
Univision Technologies Inc.,
Billerica, MA

The median filter is a popular image processing technique for removing salt and pepper ("shot") noise from images. With this technique, the eight direct neighbors and center point of a sliding 3-by-3 array are examined. The median value of the nine elements replaces the original center pixel. The median of the 3-by-3 array is the fifth element in the sorted list of nine elements; thus, the algorithm requires a high-speed sort of the nine pixel values.

The graph of **Figure 1** shows the minimum exchange network required to produce a median from nine input pixels by performing a partial sort. Each node is a two element sort, with the lower input exiting the node on the left, the higher input leaving on the right. The triangular groups of nodes perform a full sort on three elements.

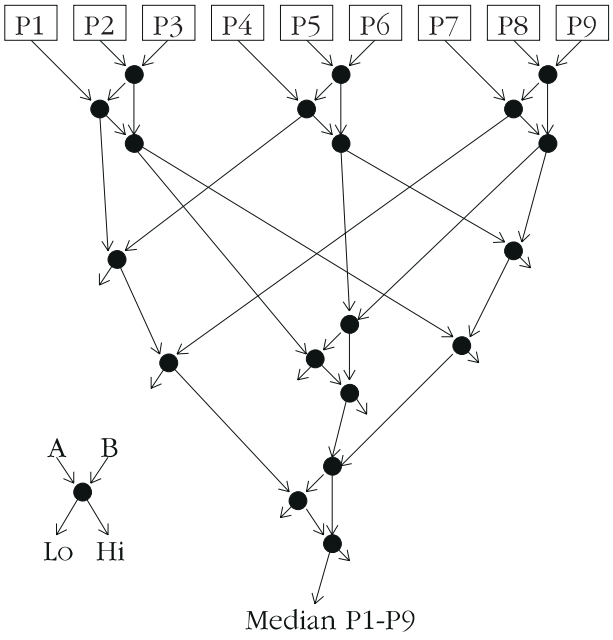

Figure 1: Minimum exchange network required to produce a median from nine input pixels by performing a partial sort

The high-speed carry logic of the XC4000E FPGA is used to implement an efficient compare/swap function. The carry logic in each CLB is set up for an A-B subtract function, while the function generators are used to implement a 2:1 multiplexer. The multiplexer is controlled by the carry out of the subtraction (**Figure 2**). Nodes where both outputs are used may be implemented in nine CLBs (eight for the mux, 1/2 for carry chain initialization, and 1/2 for carry out test); nodes where one output is discarded require only five CLBs.

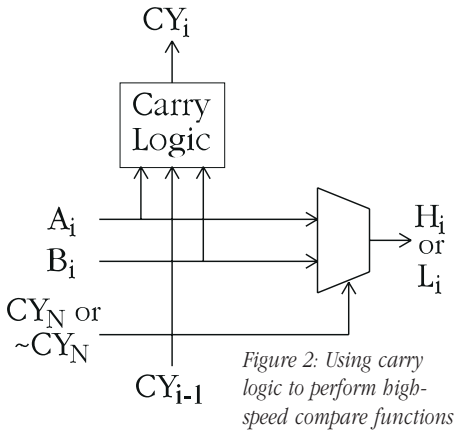

Figure 2: Using carry logic to perform high-speed compare functions

When the circuit is implemented, pipelining can be used so that only three pixels are clocked in at once, eliminating two of the three full sort node groups at the top of the graph (**Figure 3**). In a system with eight-bit pixels, total CLB usage for this real-time median sort circuit is 85 CLBs. ◆

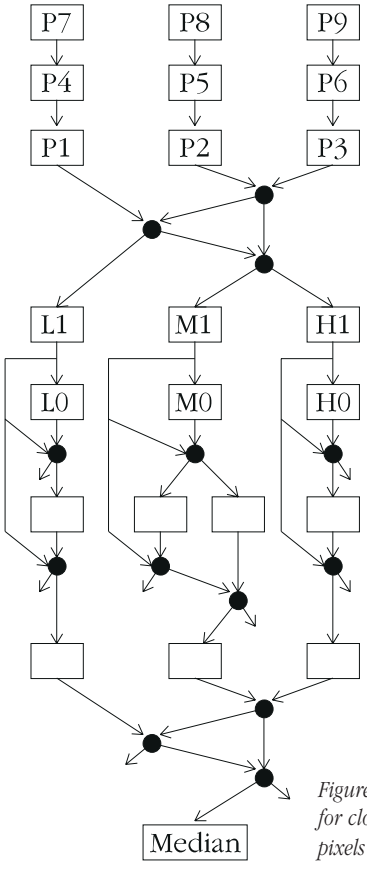

Figure 3: Pipeline for clocking in three pixels at a time

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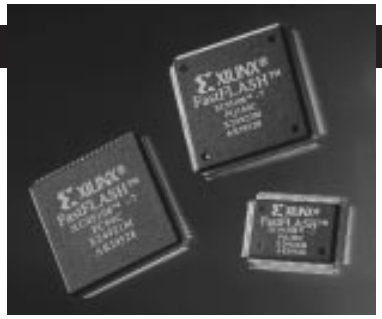


XC9500 ISP on the HP3070 Tester

With in-system-programming (ISP), programmable logic devices such as XC9500 CPLDs can be programmed and reprogrammed even though they are soldered on a system board. ISP devices can facilitate prototype development, streamline manufacturing flows and enable remote system updates.

The XC9500 family implements ISP functionality using the IEEE 1149.1 (JTAG) Test Access Port (TAP), and without requiring externally applied "supervoltages." Thus, automatic test equipment (ATE) that supports the JTAG TAP can be used to program XC9500 CPLDs.

HP3070 Configuration and Fixturing

One such ATE platform, the Hewlett Packard HP3070 Board Test System, can perform ISP as an integrated part of the manufacturing test process. The Xilinx EZTag™ software, the Xilinx-supplied vector translation tool (gen_hp) and an HP3070 ATE system equipped with a Control-Plus card are required in order to integrate XC9500 device programming into the system test flow.

Using EZTag to Generate an SVF file

First, run EZTag to generate a Serial Vector Format (SVF) file from the JEDEC programming file of the target design. The SVF file is in an ASCII format and describes TAP operations. The file encodes the entire programming algorithm for the selected device in the system as a series of TAP instructions. If a readback/verify operation is required after the program step, a separate SVF file with the verification vectors specified should be generated.

Generating an HP 3070 ISP Program

Use the SVF file(s) as input to the "gen_hp" tool. This tool takes the SVF file(s) and creates a complete HP3070 test program.

This tool runs on the HP workstation that acts as the controller for the HP 3070. The "gen_hp" program translates the SVF files to the appropriate number of digital Vector Control Language (VCL) files. VCL is the HP3070 stimulus description language.

After generating the VCL file, "gen_hp" invokes the HP 3070 "dcomp" compiler to generate the ".o" object file from each VCL file. The object file is the executable ATE used to perform ISP on a XC9500 device on the HP3070.

The "gen_hp" program also creates a testplan file that drives the test program on the HP 3070. This testplan file can then be incorporated into an existing testplan file to have the in-system programming function executed at the appropriately chosen point in the ATE test flow.

This software and methodology will also work on the following HP testers: the HP3072, HP3073, HP3074, HP3075, HP3079CT, HP3172, HP3173 and HP3175 systems.

Availability

The gen_hp software and accompanying documentation is available via the Xilinx WebLINX™ (www.xilinx.com) web site, FTP site (/pub/swhelp/cpld) and BBS (Sofware Help ➡ CPLD). The SVF to VCL translation tool is currently supported on HP700, SunOS 4.X, Windows NT and Windows 95 platforms. ◆

Procedure used to create an SVF file:

1. Create the design using XABEL-CPLD or any compatible third-party design entry tool.
2. Fit the design and save it to a JEDEC output file.
3. Invoke the EZTag software from the XACT® command line with the SVF option specified.
4. Generate an SVF file to "program," "erase" or "verify" the selected part in the boundary-scan chain.

Downloading CPLDs with an Embedded Processor

With its FastFLASH™ technology supporting up to 10,000 program/erase cycles, Xilinx XC9500 CPLDs bring all the advantages of in-system programming (ISP) to an advanced CPLD architecture. Embedded processors can be used to control CPLD in-system programming, resulting in considerable benefits throughout the product life cycle, from initial design to field updates.

Why embedded downloading?

Generally, designers download their CPLD patterns through a serial port driven from a PC or workstation during system development and debug. Once the design is stable and high-volume production begins, production-level programming can be switched to third-party programmers (such as those from Data I/O and BP Microsystems) or third-party ATE systems (such as those from HP, GenRAD and Teradyne). Increasingly, however, designers need to program parts directly using the onboard microprocessor in an embedded system.

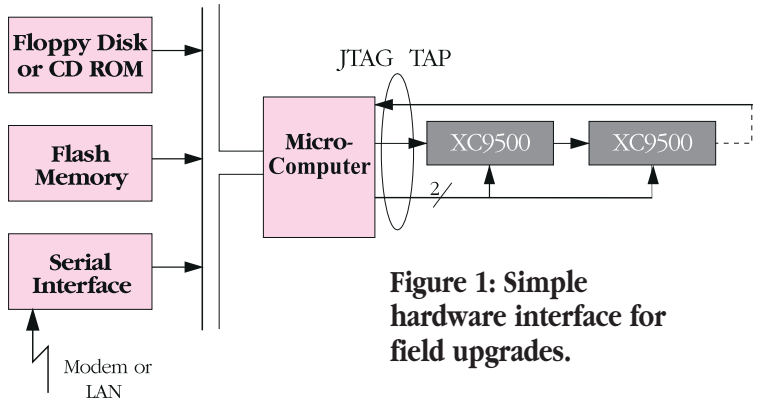


Figure 1: Simple hardware interface for field upgrades.

Having the microprocessor handle design changes on its "own" board fits the "embedded" paradigm. Embedded systems should be designed with a single, unified information port for the programming of all reconfigurable devices on the board. In the case of CPLD devices, the most-frequently used access port is the JTAG boundary scan interface (that same port can provide "double duty" as both a programming and test access port).

With the embedded processor controlling the JTAG interface, the board's CPLDs can be reconfigured by providing new programming information to the processor. As a result, changes can be easily implemented during design, prototyping, manufacturing or in the field. With sufficient prior planning, extensive design changes can be implemented (if needed) without making external physical changes in the system, such as modifications to the printed circuit board — perhaps even without opening the system enclosure!

This approach allows changes after field installation with minimal risk to overall system behavior. End users can update their own hardware. For systems with a floppy disk or CD drive, field upgrades can be implemented just like a software update. Remote updating is possible using a modem or other communication link — the embedded controller would capture update information from an external data stream and channel it to the ISP CPLDs on the board, as well as on-board flash memories (or volatile memories).

The non-volatile XC9500 CPLDs do not need reloading with each power cycle. However, because they can coexist in the same JTAG download chain with FPGAs, it may be easier and more convenient to reload their configurations during every power-up sequence. The 10,000 reprogramming cycles offered by XC9500 CPLD FastFLASH™ technology makes that strategy possible. By using the advanced JTAG capabilities contained in the XC9500 devices, the internal UserCode register can maintain a reprogramming counter, if needed.

Keeping Up with Changing Standards

There are many benefits to embedded in-system programming. Products can be updated to the "leading edge" just before shipping and then updated in the field as technology changes, rather than wait to ship until all expected upgrades are complete. For example, this capability could allow a manufacturer to ship products based on new and evolving standards because once a standard has been established, previously shipped systems can be updated in the field to maintain compliance (see **Figure 1**).

To accommodate potential field upgrades, choose a CPLD device with a robust architecture to ensure that ample speed and capacity are available to tolerate future changes. The XC9500 architecture is specifically designed to tolerate a wide range of changes while retaining the pinouts initially dictated by the PCB design. By choosing the right XC9500 device and including embedded programming capabilities in the system, embedded download success is assured.

Embedded Download App Note

Xilinx has developed the tools needed to deliver this powerful capability to designers. The package includes a thoroughly tested, transportable C program, a detailed application note on its use, and the Xilinx EZTag™ software. The design was initially developed for an 80C51-type microcontroller, but the processor-specific aspects are kept to a minimum, with a simple assembler level call. This keeps all JTAG protocols at the fully transportable ANSI C level, for which there is an abundance of available compilers. The package covers all the necessary details, including the conversion of intermediate files to formats compatible with EPROM programmers.

To obtain the embedded download application note and software, simply access the WebLINX web site at www.xilinx.com and look for the CPLD applications section. Alternately, make your request via e-mail to isp@xilinx.com. ◆

TECHNICAL SUPPORT RESOURCES

HOTLINE SUPPORT, U.S.

Customer Support Hotline: 800-255-7778
Hrs: 8:00 a.m.-5:00 p.m. Pacific time

Customer Support Fax Number: 408-879-4442
Avail: 24 hrs/day-7 days/week

E-mail Address: hotline@xilinx.com

Customer Service*: 408-559-7778, ask for customer service

** Call for software updates, authorization codes, documentation updates, etc.*

HOTLINE SUPPORT, INTERNATIONAL

UK, London Office
telephone: (44) 1932 820821
fax: (44) 1932 828522
Bulletin Board Service:
(44) 1932 333540
e-mail: ukhelp@xilinx.com

France, Paris Office
telephone: (33) 1 3463 0100
fax: (33) 1 3463 0959
e-mail: frhelp@xilinx.com

Germany, Munich Office
telephone: (49) 89 991 54930
fax: (49) 89 904 4748
e-mail: dlhelp@xilinx.com

Japan, Tokyo Office
telephone: (81) 3 3297 9163
fax: (81) 3 3297 0067
e-mail: jhotline@xilinx.com

X-TALK — The Xilinx Network of Electronic Services

Xilinx home page on the World Wide Web ... www.xilinx.com.

Electronic Technical Bulletin Board (U.S.) 408-559-9327

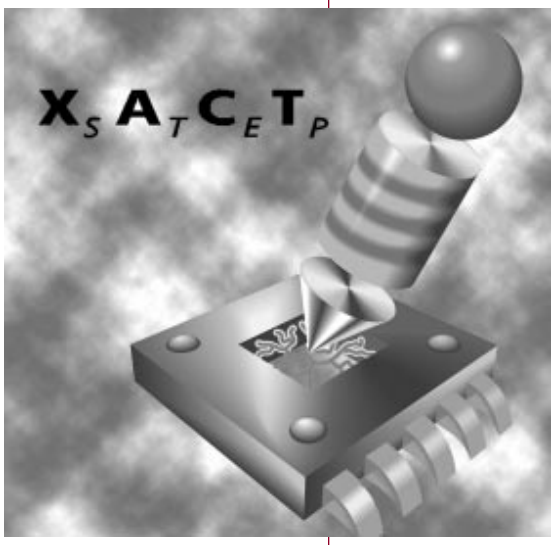
XDOCS E-mail document server- send an E-mail to xdocs@xilinx.com with 'help' as the only item in the subject header. You will automatically receive full instructions via E-mail.

XFACTS fax document server available by calling 408-879-4400.

E-mail addresses for questions on specific applications:

Digital Signal Processing applications ..... dsp@xilinx.com
PCI-bus applications ..... pci@xilinx.com
Plug and Play ISA applications ..... PnP@xilinx.com
PCMCIA card applications ..... pcmcia@xilinx.com
Asynchronous Transfer Mode applications ..... atm@xilinx.com
Reconfigurable Computing applications ..... reconfig@xilinx.com
In-System Programmable CPLD applications ..... isp@xilinx.com
Universal Serial Bus applications ..... usb@xilinx.com

Running XACT*step*™ v5.2.1 in a



XACT*step*™ version 6.0.x (the Windows tools) was compiled and tested for Windows 3.x. It was not compiled for Windows NT. Unlike Windows 95, there is no work-around to enable the Windows tools to work. This release does NOT support Windows NT.

However, we have had some success using XACT*step* v5.2.1 (the DOS tools) within a DOS session under Windows NT. There are a few things that must be done to set up the environment, as described below.

Please note that the next full release of Xilinx software will support Windows NT 4.0. The solution described here should be considered a tactical work-around for Windows NT 3.51 and a temporary work-around for Windows NT 4.0.

All of the instructions apply to both Windows NT versions 3.51 and 4.0, unless otherwise noted.

Windows Setup

Windows NT 3.51: Make sure that your Windows NT 3.51 is up-to-date with the latest set of patches and bug fixes, known as Service Pack 4. To check the status of your system, open the Administrative Tools program group and double-click on the Windows NT Diagnostics icon. Select the OS Version button and check the number next to Service Pack. If it is less than 4, you will need to upgrade. This free upgrade can be found at Microsoft's Web site: www.microsoft.com/kb/softlib/winnt.htm. Select "Service Packs" then "Windows NT 3.51 Service Pack 4 for Intel (x86)" to download. Place this self-extracting file in a temporary directory and run it in DOS. It will expand lots of files into this directory. Then, within Windows NT 3.51, choose File ➡ Run Update.exe from within this temporary directory and the update install program will run.

Windows NT 4.0: You will need to download two items from the Rainbow Technologies Web site. (Rainbow Technologies is the manufacturer of the hardware key.) At their site, www.rnbo.com/tech/drivers/drivers.htm, download "Patch for Windows NT 4.0" and "Rainport Driver for Windows NT". The former is a single executable, NTVDM.EXE. Replace the existing version in your C:\WINNT\SYSTEM32 directory and reboot. This file will be included in Windows NT 4.0 Service Pack 1 when it is built. The latter is the Rainport driver that is explained in the Drivers section.

Installation

The first thing that must be done is the Xilinx install; simply perform a Windows install. Assuming that D:\ is your CD drive, just select File ➡ Run (or Start ➡ Run) and type D:\Wn1\Install\Winstall.exe at the prompt. If you are using Viewlogic tools that support Windows NT, (Workview Office, NOT PROseries), choose the DS-VL-STD-PC1 product (not the Stand-alone) from a Custom install. Select the products you would like to install, but keep in mind that you will be using the DOS tools, so programs like the Floorplanner should be de-selected. Change the target path so the interface tools are copied to C:\WVOFFICE instead of C:\PROSER.

Next, copy the kernel32.dll file from D:\PROSER to both C:\XACT and C:\WVOFFICE.

Then, install the patched version of XNFPREP. This file is located on our FTP

site at ftp://ftp.xilinx.com/pub/swhelp/xact-pc and on our BBS (408-559-9327) in the Software Help ➡ XACT-PC area. The name of the file is PREP_NT.ZIP. After unzipping this file, place the XNFPREP.EXE file in C:\XACT, overwriting the existing XNFPREP.EXE. This new version, 5.2.1c, fixes a bug where the .PRP file would not be written.

Setting the Environment

Next, you must modify the environment variables. Keep in mind that you must have administrator privileges to modify existing system environment variables and to add drivers.

In the Main program group, double-click on Control Panel and then System (NT 3.51) or right click on My Computer (NT 4.0). In the System Environment Variables area, select Path. In the Value field at the bottom of the screen, add

```
C:\XACT;C:\WVOFFICE;
```

before the existing path, so it looks like

```
C:\XACT;C:\WVOFFICE;<rest_of_path>.
```

Hit the Set button, then create a new variable; the Variable is XACT and the Value is

```
C:\XACT;C:\WVOFFICE
```

Then bring C:\WINNT\SYSTEM32\AUTOEXEC.NT into a text editor. Add this line at the end:

```
SET XACT=C:\XACT;C:\WVOFFICE
```

You can verify that these settings have been applied (after rebooting Windows NT) by typing SET in the DOS window. Leave all the C:\WVOFFICE statements out if you are not using the Workview Office tools.

Drivers

Next, you must install the Rainport driver, which is also located on our FTP site at ftp://ftp.xilinx.com/pub/swhelp/xact-pc and on our BBS in the Software Help ➡ XACT-PC area. The file is called RAINPORT.EXE. This driver is required to enable Windows NT to recognize the hardware key. The RAINPORT.EXE contains a readme about how to install the driver. This driver can also be found in the SENTINEL directory on the Workview Office 7.2 CD. Choose Control Panels ➡ Drivers ➡ Add to install this. This version is only for use with Windows NT 3.51.

Windows NT 4.0 users will install the newer version of Rainport mentioned in the Windows Setup section. A readme within the ZIP file explains how to install this driver.

Running the tools

You will be running the tools in an MS-DOS session. Take a look at the Reference Guide Volumes 1, 2 and 3 for specific information about using these tools in a DOS environment.

You will see that some of the Windows tools will work. Besides the Simulation Utility and the Memory Generator, you can create a new icon for the Timing Analyzer. The Command Line for this tool is c:\xact\timingan.exe and the Working Directory is c:\xact. There have been cases where these Windows tools have had problems, and the workaround is to use the DOS equivalent. Tools that will not work are the Design Manager, Flow Engine, and Floorplanner.

If you have any problems using the Adobe Acrobat reader, you can download a copy of Acrobat 2.1 for Windows 95/NT from their Web site, www.adobe.com/acrobat/windows.html.

Hopefully, these hints will get you up and running within your Windows NT environment. There are some differences with different installations of Windows NT, so results may certainly vary. Please keep in mind that these tools were never intended to run in Windows NT, but if you do run into problems, please contact Xilinx Technical Support for assistance. ◆

Foundation

Q Besides the CD-ROM supplied with the product, are there any sources of additional information about using the Xilinx Foundation Series software?

The Foundation Documentation Update Pack contains application notes about the Foundation Logic Simulator, Foundation XVHDL compiler, and a new simulation tutorial. Get FND_DOC1.EXE (self-extracting ZIP file) from the Xilinx FTP site (ftp.xilinx.com/pub/swhelp/foundation) or the Xilinx BBS (Software Help ➡ Aldec).

Mentor Graphics

Q Can XACT*step* 5.2.1 be used with Mentor Graphics' B.*x* release?

A: Under Mentor B.*x*, Gen_sch8 and XBLXGS may fail with either "call to undefined procedure" (SunOS) or "unresolved propagate symbol" (HP-UX) error messages due to problems with dynamically linking to Mentor's Design Data Port (DDP). A patch is available to fix these problems and make XACT*step* 5.2.1 interface smoothly with Mentor B.*x*. The patch may be downloaded from the Xilinx FTP site at:

```
ftp://ftp.xilinx.com/pub/
 swhelp/mentor/b1_521s.tar.Z
 (SunOS)
ftp://ftp.xilinx.com/pub/
 swhelp/mentor/b1_521h.tar.Z
 (HP-UX)
```

Q A schematic originally targeted for the XC4000 family is now targeting an XC4000E device. During Men2XNF8, the following error occurs when running EDIF2XNF:

```
Error: 6 EDIF data "ofd.eds"
 not found in directory
 "/usr/xact/data/unified/
 edif4000e"
```

In this case, the schematic was created using the XC4000 library, but the design is now targeted to an XC4000E device. (Other family combinations may also cause this error.) Certain symbols are primitives in the schematic library with which the design was built (XC4000), but are macros in the library associated with the device being targeted (XC4000E). In this example, OFD is a primitive in the XC4000 library but is a macro in the XC4000E library (since it has, underneath it, the clock-enabled OFDX symbol).

ENWrite (Mentor's EDIF netlister) looks at the XC4000 version of OFD in the schematic. This component has attached to it a COMP=OFD property, indicating that this component is a primitive and should be written as such in the EDIF file. EDIF2XNF then takes this primitive description and looks for the corresponding ofd.eds file in the $LCA/data/unified/edif4000e directory, that contains EDIF descriptions for XC4000E primitives. Since OFD is not a primitive in the XC4000E family, the ofd.eds file does not exist in the directory, resulting in the error.

The correct OFD from the XC4000E library has no COMP=OFD property attached to it, since the COMP property is reserved for primitives. Therefore, if the correct XC4000E component had been used, ENWrite would have written out the hierarchy below OFD. Then, EDIF2XNF would have never seen the OFD "primitive" and would have never tried to look for a non-existent ofd.eds file in the XC4000E data directory.

The proper way to retarget the design to a new device family is to use the Convert Design utility in PLD_DA before running the implementation flow. Convert Design replaces the library components in a schematic or set of schematics so that they come from the proper library. For instructions on how to use Convert Design, see Solution 798, "Retargeting a design in Mentor Design Architect (Convert Design)," from the Xilinx Solutions Database:

```
http://www.xilinx.com/
 techdocs/798.htm
```

Mentor Graphics

(continued)

Q What is happening when Quicksim issues this warning on every primitive in a design:

```
// Warning: Instance
 '/GIVE_ME_AN_E'
// Could not find a
 registered simulation model
 with label: 'xc4000'
// NULL model will be
 inserted. (from: Analysis/
 Digital/Simulation
 Utilities/Dsim 85)
```

This is caused by an incorrectly-written simulation viewpoint for the design, which can result when a design is retargeted to a new device family. The solution is to delete that default viewpoint, then run PLD_DVE_SIM on the design, specifying the correct part family. If done from the command line, an XC4000 design, for example, might use:

```
delete_object
 blanking_design/default
pld_dve_sim blanking_design
 xc4000
```

Note: If Timsim8 -o was used to create the simulation model, be sure to run Timsim8 instead of PLD_DVE_SIM. Timsim8 -o runs PLD_DVE_SIM, then adds links to timing information into the viewpoint afterwards.

Synopsys

Q How are Boundary Scan components for the XC4000 family instantiated in Verilog-based designs?

To use Boundary Scan components in XC4000 Series devices, instantiate the boundary scan symbol (BSCAN) and the associated dedicated I/O. Use the "dont_touch" attribute; otherwise, BSCAN may be deleted by the Synopsys compiler.

The Verilog code for instantiating BSCAN in the XC4000 is shown below. VHDL and Verilog examples for both the XC4000 and XC5000 can be found on the Xilinx Web site (www.xilinx.com), or can be emailed to users via the Xdocs mail server (email xdocs@xilinx.com).

XC4000/XC4000E example of instantiating the BSCAN symbol:

```
module example (a,b,c);

input a, b;
output c;
reg c;

wire tck_net;
wire tdi_net;
wire tms_net;
wire tdo_net;

BSCAN u1 (.TDI(tdi_net), .TMS(tms_net),
 .TCK(tck_net), .TDO(tdo_net));

TDI u2 (.I(tdi_net));
TMS u3 (.I(tms_net));
TCK u4 (.I(tck_net));

TDO u5 (.O(tdo_net));

always@(posedge b)
    c<=a;

endmodule
```

Runscript for compiling the XC4000/XC4000E BSCAN Verilog Example:

```
PART = 4025ehq240-3
TOP = example

read -format verilog "bscan4k.v"

set_port_is_pad "*"
insert_pads

set_dont_touch u1
set_dont_touch u2
set_dont_touch u3
set_dont_touch u4
set_dont_touch u5

compile

replace_fpga

set_attribute TOP "part" -type string
 PART

write -f xnf -h -o "bscan4k.sxnf"
```

COMPONENT AVAILABILITY CHART

PINS	TYPE	CODE	XC3020A	XC3030A	XC3042A	XC3064A	XC3090A	XC3020L	XC3030L	XC3042L	XC3064L	XC3090L	XC3142L	XC3190L	XC3120A	XC3130A	XC3142A	XC3164A	XC3190A	XC3195A	XC4003E	XC4005E	XC4006E	XC4008E	XC4010E	XC4013E	XC4020E	XC4025E	XC4028EX	XC4036EX	XC4044EX	XC4052XL	XC4062XL
44	PLASTIC LCC	PC44		◆												◆																	
	PLASTIC QFP	PQ44																															
	PLASTIC VQFP	VQ44																															
	CERAMIC LCC	WC44																															
48	PLASTIC DIP	PD48																															
64	PLASTIC VQFP	VQ64		◆					◆							◆																	
68	PLASTIC LCC	PC68	◆	◆											◆	◆																	
	CERAMIC LCC	WC68																															
	CERAMIC PGA	PG68																															
84	PLASTIC LCC	PC84	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆								
	CERAMIC LCC	WC84																															
	CERAMIC PGA	PG84	◆	◆	◆										◆	◆	◆																
100	CERAMIC QFP	CQ100																															
	PLASTIC PQFP	PQ100	◆	◆	◆										◆	◆	◆				◆	◆											
	PLASTIC TQFP	TQ100														◆	◆																
	PLASTIC VQFP	VQ100		◆	◆				◆	◆			◆			◆	◆				◆												
	TOP BRZ. CQFP	CB100	◆		◆										◆	◆																	
120	CERAMIC PGA	PG120																			◆												
132	PLASTIC PGA	PP132			◆	◆											◆	◆															
	CERAMIC PGA	PG132			◆	◆											◆	◆															
144	PLASTIC TQFP	TQ144			◆	◆	◆			◆	◆	◆	◆	◆			◆	◆				◆	◆										
	CERAMIC PGA	PG144																															
156	CERAMIC PGA	PG156																				◆	◆										
160	PLASTIC PQFP	PQ160				◆	◆											◆	◆	◆		◆	◆	◆	◆	◆							
164	CERAMIC QFP	CQ164																															
	TOP BRZ. CQFP	CB164					◆												◆	◆													
175	PLASTIC PGA	PP175					◆												◆	◆													
	CERAMIC PGA	PG175					◆												◆	◆													
176	PLASTIC TQFP	TQ176					◆					◆		◆					◆														
184	CERAMIC PGA	PG184																															
191	CERAMIC PGA	PG191																						◆	◆								
196	TOP BRZ. CQFP	CB196																															
208	PLASTIC PQFP	PQ208					◆												◆	◆		◆	◆	◆	◆	◆							
	METAL MQFP	MQ208																															
	HI-PERF QFP	HQ208																							❖	◆	◆		◆				
223	CERAMIC PGA	PG223																		◆						◆	◆	◆					
225	PLASTIC BGA	BG225																							◆	◆							
	WINDOWED BGA	WB225																															
228	TOP BRZ. CQFP	CB228																															
240	PLASTIC PQFP	PQ240																								◆							
	METAL MQFP	MQ240																															
	HI-PERF QFP	HQ240																								◆	◆	◆	◆				
299	CERAMIC PGA	PG299																										◆	◆				
304	HI-PERF. QFP	HQ304																										◆	◆	◆			
352	PLASTIC BGA	BG352																											◆				
411	CERAMIC PGA	PG411																												◆	◆	◆	
432	PLASTIC BGA	BG432																												◆	◆	◆	
475	CERAMIC PGA	PG475																															◆
560	PLASTIC BGA	BG560																														◆	◆

NOVEMBER 1996

PINS	TYPE	CODE	XC4005L	XC4010L	XC4013L	XC5202	XC5204	XC5206	XC5210	XC5215	XC7236A	XC7272A	XC7318	XC7336	XC7336Q	XC7354	XC7372	XC73108	XC73144	XC9536	XC9572	XC95108	XC95216
44	PLASTIC LCC	PC44									◆		◆	◆	◆	◆				◆			
	PLASTIC QFP	PQ44											◆	◆	◆								
	PLASTIC VQFP	VQ44													◆					◆			
	CERAMIC LCC	WC44									◆			◆	◆	◆							
48	PLASTIC DIP	PD48																					
64	PLASTIC VQFP	VQ64																					
68	PLASTIC LCC	PC68										◆				◆	◆						
	CERAMIC LCC	WC68										◆				◆	◆						
	CERAMIC PGA	PG68																					
84	PLASTIC LCC	PC84	◆	◆		◆	◆	◆	◆			◆					◆	◆			❖	◆	
	CERAMIC LCC	WC84										◆					◆	◆					
	CERAMIC PGA	PG84										◆											
100	CERAMIC QFP	CQ100																					
	PLASTIC PQFP	PQ100				◆	◆	◆									◆	◆			❖	◆	
	PLASTIC TQFP	TQ100																			❖	◆	
	PLASTIC VQFP	VQ100				◆	◆	◆															
	TOP BRZ. CQFP	CB100																					
120	CERAMIC PGA	PG120																					
132	PLASTIC PGA	PP132																					
	CERAMIC PGA	PG132																					
144	PLASTIC TQFP	TQ144				◆	◆	◆	◆														
	CERAMIC PGA	PG144																◆					
156	CERAMIC PGA	PG156				◆	◆																
160	PLASTIC PQFP	PQ160					◆	◆	◆	◆								◆	◆			◆	◆
164	CERAMIC QFP	CQ164																					
	TOP BRZ. CQFP	CB164																					
175	PLASTIC PGA	PP175																					
	CERAMIC PGA	PG175																					
176	PLASTIC TQFP	TQ176		◆				◆	◆														
184	CERAMIC PGA	PG184																					
191	CERAMIC PGA	PG191						◆															
196	TOP BRZ. CQFP	CB196																					
208	PLASTIC PQFP	PQ208	◆	◆	◆			◆	◆														
	METAL MQFP	MQ208																					
	HI-PERF QFP	HQ208								◆													◆
223	CERAMIC PGA	PG223							◆														
225	PLASTIC BGA	BG225			◆				◆	◆								◆	◆				
	WINDOWED BGA	WB225																					
228	TOP BRZ. CQFP	CB228																					
240	PLASTIC PQFP	PQ240			◆				◆														
	METAL MQFP	MQ240																					
	HI-PERF QFP	HQ240								◆													
299	CERAMIC PGA	PG299								◆													
304	HI-PERF. QFP	HQ304								◆													
352	PLASTIC BGA	BG352								◆													
411	CERAMIC PGA	PG411																					
432	PLASTIC BGA	BG432																					
499	CERAMIC PGA	PG499																					
596	PLASTIC BGA	BG596																					

◆ = Product currently shipping or planned

❖ = New since last issue of *XCell*

Programmer Support For Xilinx XC7200/XC7300 CPLDS — November 1996

MANUFACTURER	MODEL	7236A	7272A	7318	7336	7336Q	7354	7372	73108	73144
ADVANTECH	PC-UPROG									
	LABTOOL-48	V1.31A	V1.31A	V1.31A	V1.31A	V1.31A	V1.31A	V1.31A	V1.31A	
ADVIN SYSTEMS	PILOT-U40	10.84B	10.84B	10.84B	10.84B	10.84B				
	PILOT-U84	10.84B	10.84B	10.84B	10.84B	10.84B	10.84B	10.84B	10.84B	10.84B
B&C MICROSYSTEMS, INC.	Proteus	1Q97	1Q97	1Q97	1Q97	1Q97	1Q97	1Q97	1Q97	1Q97
BP MICROSYSTEMS	BP-1200	V3.15	V3.15	V3.15	V3.18	V3.15	V3.15	V3.15	V3.15	
	BP-2100	V3.15	V3.15	V3.15	V3.18	V3.15	V3.15	V3.15	V3.15	
DATAMAN	DATAMAN-48	V1.30	V1.30	V1.30	V1.30	V1.30	V1.30	V1.30	V1.30	
DATA I/O	2900			BBS	BBS	BBS	BBS			
	3900/AutoSite			BBS	BBS	BBS	BBS	BBS	BBS	BBS
	UniSite			BBS	BBS	BBS	BBS	BBS	BBS	BBS
DEUS EX MACHINA ENGINEERING	XPGM	V1.40	V1.40	V1.40	V1.40	V1.40	V1.40	V1.40	V1.40	V1.50
ELECTRONIC ENGINEERING TOOLS	ALLMAX/ALLMAX+	V2.4U	V2.4U	V2.4U	V2.4U	V2.4U	V2.4U	V2.4U	V2.4U	
	MEGAMAX	V1.1E	V1.1E	V1.1E	V1.1E	V1.1E	V1.1E	V1.1E	V1.1E	
ELAN	6000 APS				DISQUALIFIED					
HI-LO SYSTEMS RESEARCH	All-03A	V3.09	V3.09	V3.09	V3.09	V3.09	V3.09	V3.09	V3.09	
	All-07	V3.09	V3.09	V3.09	V3.09	V3.09	V3.09	V3.09	V3.09	
ICE TECHNOLOGY LTD	Micromaster 1000/E	V1.1	V1.1	V1.1	V1.1	V1.1	V1.1	V3.1	V1.1	V1.1
	Speedmaster 1000/E	V1.1	V1.1	V1.1	V1.1	V1.1	V1.1	V3.1	V1.1	V1.1
	Micromaster LV	V1.1	V1.1	V1.1	V1.1	V1.1	V1.1	V3.1	V1.1	V1.1
	Speedmaster LV	V1.1	V1.1	V1.1	V1.1	V1.1	V1.1	V3.1	V1.1	V1.1
LEAP ELECTRONIC CO., LTD.	LEAPER-10	V3.2	V3.2	V3.2	V3.2	V3.2	V3.2	V3.2	V3.2	V3.2
	LP U4	V2.1	V2.1	V2.1	V2.1	V2.1	V2.1	V2.1	V2.1	V2.1
LOGICAL DEVICES	ALLPRO-88				DISQUALIFIED					
	ALLPRO-88XR				DISQUALIFIED					
	ALLPRO-96	6.4.26	6.4.26	6.4.26	6.4.26	6.4.26	6.4.26	6.4.26	6.4.26	
	Chipmaster 2000	V2.4U	V2.4U	V2.4U	V2.4U	V2.4U	V2.4U	V2.4U	V2.4U	
	Chipmaster 6000	V1.31A	V1.31A	V1.31A	V1.31A	V1.31A	V1.31A	V1.31A	V1.31A	
	XPRO-1				DISQUALIFIED					
MICROPROSS	ROM9000									
MQP ELECTRONICS	SYSTEM 2000	Nov-96	Nov-96	Nov-96	Nov-96	Nov-96	Nov-96	Nov-96	Nov-96	Nov-96
	PIN-MASTER 48	Nov-96	Nov-96	Nov-96	Nov-96	Nov-96	Nov-96	Nov-96	Nov-96	Nov-96
NEEDHAM'S ELECTRONICS	EMP20	V3.10	V3.10	V3.10	V3.10	V3.10	V3.10	V3.10	V3.10	
SMS	EXPERT									
	OPTIMA									
STAG	ECLIPSE	6.4.26	6.4.26	6.4.26	6.4.26	6.4.26	6.4.26	6.4.26	6.4.26	6.8.9
SUNRISE	T-10 UDP									
	T-10 ULC									
SUNSHINE	POWER-100	V8.40	V8.40	V8.40	V8.40		V8.40	V8.40	V8.40	
	EXPRO-60/80	V8.40	V8.40	V8.40	V8.40		V8.40	V8.40	V8.40	
SYSTEM GENERAL	TURPRO-1/FX	V2.30	V2.30	V2.30	V2.30	V2.30	V2.30	V2.30	V2.30	V2.30
	MULTI-APRO	V3.02	V3.02	V3.02	V3.02	V3.02	V3.02	V3.02	V3.02	V3.02
TRIBAL MICROSYSTEMS	Flex-700	V3.09	V3.09	V3.09	V3.09	V3.09	V3.09	V3.09	V3.09	
	TUP-300	V3.09	V3.09	V3.09	V3.09	V3.09	V3.09	V3.09		
	TUP-400	V3.09	V3.09	V3.09	V3.09	V3.09	V3.09	V3.09		
XELTEK	SUPERPRO									
	SUPERPRO II	2.4B	2.4B	2.4B	2.4B	2.4B	2.4B	2.4B	2.4B	2.4B
	SUPERPRO II/P	2.4B	2.4B	2.4B	2.4B	2.4B	2.4B	2.4B	2.4B	2.4B
XILINX	HW-130	1.14	1.04	1.15	1.15	1.06	1.16	1.07	1.07	1.02

Changes since last issue are noted in color. **Note:** The XC7200 and XC7300 CPLD charts have been combined since the last issue.

Programmer Support For XC9500 — November 1996 — Top Three by Region

UNITED STATES		EUROPE		SOUTHEAST ASIA/JAPAN	
MANUFACTURER	DATE	MANUFACTURER	DATE	MANUFACTURER	DATE
BP MICROSYSTEMS	11/15/96	DATA I/O	NOW	DATA I/O	NOW
DATA I/O	NOW	SMS	12/31/96	SYSTEM GENERAL	12/15/96
LOGICAL DEVICES	12/15/96	STAG	1/17/97	HI-LO	11/6/96
XILINX HW-130	V3.02	XILINX HW-130	V3.02	XILINX HW-130	V3.02

PROGRAMMER SUPPORT FOR XILINX XC1700 SERIAL PROMS-NOVEMBER 1996

MANUFACTURER	MODEL	XC1718D XC1736D XC1765D	XC1718L XC1765L	XC17128D XC17256D	XC17128L XC17256L
ADVANTECH	PC-UPROG LABTOOL-48				
ADVIN	PILOT-U24	10.84B		10.84B	
	PILOT-U28	10.84B		10.84B	
	PILOT-U32	10.84B		10.84B	
	PILOT-U40	10.84B		10.84B	
	PILOT-U84	10.84B		10.84B	
	PILOT-142	10.84B		10.84B	
	PILOT-143	10.84B		10.84B	
	PILOT-144	10.84B		10.84B	
	PILOT-145	10.84B		10.84B	
B&C MICROSYSTEMS INC.	Proteus-UP40	3.7Q		3.7Q	
BP MICROSYSTEMS	CP-1128 EP-1140				
	BP-1200	V3.15	V3.15	V3.15	
	BP-2100	V3.15	V3.15	V3.15	
BYTEK	135H-FT/U MTK-1000 MTK-2000 MTK-4000				
DATAMAN	DATAMAN-48	V1.30		V1.30	
DATA I/O	UniSite	BBS	BBS	BBS	Oct-96
	2900	BBS	BBS	BBS	Oct-96
	3900	BBS	BBS	BBS	Oct-96
	AutoSite	BBS	BBS	BBS	Oct-96
	ChipLab	BBS	BBS	BBS	Oct-96
	2700	BBS	BBS	BBS	Oct-96
DEUS EX MACHINA	XPGM	V1.40	V1.40	V1.40	V1.40
E E TOOLS	ALLMAX/ALLMAX+	V2.4U	V2.4U	V2.4U	
	MEGAMAX	V1.1E	V1.1E	V1.1E	
ELAN DIGITAL SYSTEMS	3000-145 5000-145 6000 APS	Disqualified			
HI-LO SYSTEMS RESEARCH	All-03A	V3.19	V3.19	V3.19	V3.19
	All-07	V3.19	V3.19	V3.19	V3.19
ICE TECHNOLOGY LTD	Micromaster 1000/E	V3.17	V3.17	V3.17	V3.17
	Speedmaster 1000/E	V3.17	V3.17	V3.17	V3.17
	Micromaster LV	V3.17	V3.17	V3.17	V3.17
	LV40 Portable	V3.17	V3.17	V3.17	V3.17
	Speedmaster LV	V3.17	V3.17	V3.17	V3.17
LEAP ELECTRONICS	LEAPER-10	V2.0		V2.0	
	LP U4	V2.0		V2.0	

MANUFACTURER	MODEL	XC1718D XC1736D XC1765D	XC1718L XC1765L	XC17128D XC17256D	XC17128L XC17256L
LINK COMPUTER GRAPHICS	CLK-3100	V5.61		V5.61	
LOGICAL DEVICES	ALLPRO-40				
	ALLPRO-88	V2.7		V2.7	
	ALLPRO-88XR	V2.7		V2.7	
	ALLPRO-96	6.5.10	6.5.10	6.5.10	6.5.10
	CHIPMASTER 2000	V2.4U		V2.4U	
	CHIPMASTER 6000	V1.31A		V1.31A	
	XPRO-1	SPROM.310		SPROM.310	
MICRO PROSS	ROM 5000 B ROM 3000 U ROM9000				
MQP ELECTRONICS	MODEL 200	6.46	6.46	6.46	
	SYSTEM 2000	2.25	2.25	2.25	
	PIN-MASTER 48				
NEEDHAM'S ELECTRONICS	EMP20	V3.10		V3.10	
RED SQUARE	IQ-180		disqualified		
	IQ-280		disqualified		
	Uniwriter 40		disqualified		
	Chipmaster 5000		disqualified		
SMS	Expert Optima Multisyte Sprint Plus48				
STAG	Eclipse Quasar	6.5.10	6.5.10	6.5.10	6.5.10
SUNRISE	T-10 UDP T-10 ULC				
SUNSHINE	POWER-100	V8.40		V8.40	
	EXPRO-60/80	V8.40		V8.40	
SYSTEM GENERAL	TURPRO-1	V2.26H		V2.26H	V2.26H
	TURPRO-1 F/X	V2.26H		V2.26H	V2.26H
	TURPRO-1 T/X				
	APRO	V1.24			
	MULTI-APRO	V1.16	V1.16	V1.16	V1.16
TRIBAL MICROSYSTEMS	TUP-300	V3.19	V3.19	V3.19	V3.19
	TUP-400	V3.19	V3.19	V3.19	V3.19
	FLEX-700	V3.19	V3.19	V3.19	V3.19
XELTEK	SuperPRO				
	SuperPRO II	2.4B		2.4B	
	SuperPRO II/P	2.4B		2.4B	
XILINX	HW-112	5.20		5.20	
	HW-130	2.01	2.01	2.01	1.00

Changes since last issue printed in color; 1736A, 1765 and 17128 columns eliminated since last issue

XILINX ALLIANCE-EDA COMPANIES & PRODUCTS-NOVEMBER 1996-1 OF 2

	Company Name	Product Name	Version	Function	DesignKit	3K/ 4K	XC 5200	CPLD 7K9K	Uni Lib	PC	PLATFORMS Sun	RS6000	HP7
DIAMOND	Aldec	Active-CAD	2.2	Schematic Entry, State Machine & HDL Editor, FPGA Synthesis & Simulation	Included	✓	✓	✓	✓	✓			
	Cadence	Verilog	2.4	Simulation	Xilinx Front End	✓	✓	7k	✓		✓	✓	✓
		Concept	2.1	Schematic Entry	Xilinx Front End	✓		7k	✓		✓	✓	✓
		FPGA Designer	9504	Topdown FPGA Synthesis	Call Xilinx	✓	✓	7k	✓		✓	✓	✓
		Synergy	2.3	FPGA Synthesis	Call Xilinx	✓	✓	7k	✓		✓	✓	✓
		Composer	4.4	Schematic Entry	Xilinx Front End	✓		7k	✓		✓	✓	✓
	Mentor Graphics	Autologic	B.x	Synthesis	Xilinx Synthesis Lib.	✓	✓	7k	✓		✓	✓	✓
		Design Architect	B.x	Schematic Entry	Call Xilinx	✓	✓	7k	✓		✓	✓	✓
		QuickSim II	B.x	Simulation	Call Xilinx	✓	✓	7k	✓		✓	✓	✓
		QuickHDL	B.x	Simulation	Call Xilinx	✓	✓	7k	✓		✓	✓	✓
	OrCAD	Simulate (Win)	6.10	Simulation	Call OrCAD	✓	✓	7k		✓			
		VST 386+ (DOS)	1.2	Simulation	Call OrCAD	✓		7k	✓	✓			
		Capture (Win)	7.0	Schematic Entry	Call OrCAD	✓	✓	7k	✓	✓			
		SDT 386+ (DOS)	1.2	Schematic Entry	Call OrCAD	✓		7k	✓	✓			
		PLD 386+ (DOS)	2.0	Synthesis	Call OrCAD	✓		7k		✓			
	Synario Design Automation	ABEL	6.3	Synthesis, Simulation	ABEL-XCPLD			✓	✓	✓			
		Synario	2.3	Schematic Entry, Synthesis & Simulation	SYRO-LCA, SYRO-XEPLD	✓	✓	✓	✓	✓			
	Synopsys	FPGA Express	1.0	Synthesis	Call Synopsis	✓	✓	TBD		✓			
		FPGA Compiler	3.5	Synthesis	Call Xilinx	✓	✓	✓	✓		✓	✓	✓
		VSS	3.5	Simulation	Call Xilinx	✓	✓	✓	✓		✓	✓	✓
		Design Compiler	3.5	Synthesis	Call Xilinx	✓	✓	✓	✓		✓	✓	✓
	Viewlogic	WorkView Office	7.1.2/7.2	Schem/Sim/Synth	Call Xilinx	✓	XACT6	✓	✓	✓	✓	✓	✓
		ProSynthesis	5.02	Synthesis	Call Xilinx	✓	XACT6	7k	✓	✓	✓	✓	✓
		ProSim	6.1	Simulation, Timing Analysis	Call Xilinx	✓	XACT6	7k	✓	✓	✓	✓	✓
		ProCapture	6.1	Schematic Entry	Call Xilinx	✓	XACT6	7k	✓	✓	✓	✓	✓
		PowerView	6.0	Schem/Sim/Synth/Timing Analysis	Call Xilinx	✓	✓	✓	✓		✓	✓	✓
RUBY	Capilano Computing	Design Works	3.1	Schematic Entry/Sim	XD-1	✓			✓	✓			
	Compass Design Automation	ASIC Navigator		Schematic Entry	Xilinx Design Kit	✓	✓	7k			✓		✓
		X-Syn		Synthesis		✓					✓		✓
		QSim		Simulation		✓	✓	7k			✓		✓
	Escalade	DesignBook	2.0	Design Entry		✓			✓	✓	✓		
	Exemplar Logic	Galileo	3.2	Synthesis/Timing Analysis Simulation	Included	✓	✓	✓	✓	✓	✓		✓
	IK Technology Co.	Ishizue Professionals	1.06	Schematic Entry/Simulation	Xilinx Design Kit	✓	4Q			✓	✓		✓
	IKOS Systems	Voyager	2.31	Simulation	Xilinx Tool Kit	✓	✓				✓		✓
		Gemini	1.21	Simulation	Xilinx Tool Kit	✓	✓				✓		✓
	INCASES Engineering GmbH	Theda	4.1	Design Entry	Xilinx Kit	✓							✓
	ISDATA	LOG/iC Classic	4.2	Synthesis	LCA-PP	✓		7k	✓	✓	✓		✓
		LOG/iC2	4.2	Synthesis Simulation	Xilinx Mapper	✓	✓	7k	✓	✓	✓		✓
	Logic Modeling Corp. (Synopsis Division)	Smart Model		Simulation Models	In Smart Model Lib.	✓	✓	7k,9k		✓	✓	✓	✓
		LM1200		Hardware Modeler	Xilinx Logic Module	✓		7k,9k		✓	✓	✓	
	Model Technology	V-System/VHDL	4.4j (PC) 4.6a (WS)	Simulation		✓			✓	✓	✓	✓	✓
	Protel Technology	Advanced Schematic	3.2	Schematic Entry	Included	✓	✓	7k	✓	✓			
		Advanced PLD	3	PLD/FPGA Design & Simulation	Included	✓	✓	7k		✓			
	Quad Design Technology	Motive	4.3	Timing Analysis	XNF2MTV	✓				✓	✓	✓	✓
	SimuCad	Silos III	96.1	Schematic Entry & Simulation	Included	✓	✓		✓	✓			
	Sophia Sys & Tech	Vanguard	5.31	Schematic Entry	Xilinx I/F Kit	✓		✓		✓	✓		✓
	Summit Design Corp.	Visual HDL	3.0	Graphical Design Entry/Simulation/Debug	EDIF Interface	✓	✓	✓	✓	✓	✓	✓	✓
	Synplicity, Inc.	Synplify-Lite	2.6b	Synthesis	Xilinx Mapper	✓	✓	9k	✓	✓	✓		✓
		Synplify	2.6b	Synthesis	included	✓	✓	9k	✓	✓	✓		✓
	TopDown Design Solutions	V-BAK	1.1	XNF to VHDL translator	XNF interface	✓	✓		✓	✓	✓	✓	
	Veda Design Automation Inc	Vulcan	4.5	Simulation	XILINX Tool Kit	✓					✓		✓

XILINX ALLIANCE-EDA COMPANIES & PRODUCTS-AUGUST 1996-2 OF 2

	Company Name	Product Name	Version	Function	DesignKit	2K/3K/4K	XC 5200	CPLD 7K9K	Uni Lib	PLATFORMS PC	Sun	RS6000	HP7
RUBY	Veribest	Veribest VHDL	14.0	Schematic Entry	Xilinx FPGA Design Kit	3k,4k			✓	✓	✓		✓
		Veribest Verilog	14.0	Simulation	Xilinx FPGA Design Kit	3k,4k			✓	✓	✓		✓
		VeriBest Simulator	14.0	Simulation	Xilinx FPGA Design Kit	3k,4k	✓		✓	✓	✓		✓
		DMM	14.x	Design Management	Xilinx FPGA Design Kit	3k,4k	✓		✓	✓	✓		✓
		VeriBest Synthesis	14.0	Synthesis	Xilinx FPGA Design Kit	3k,4k	✓		✓	✓	✓		✓
		Synovation	12.2	Synthesis	Xilinx FPGA Design Kit	3k,4k			✓	✓	✓		✓
		PLDSyn	12.0	Design Entry Synthesis		✓		7k		✓	✓		✓
		VerBest Design Capture	14.x	Design Capture	Xilinx FPGA Design Kit	3k,4k	✓		✓	✓	✓		✓
EMERALD	Accolade Design Automation	Peak VHDL	2.21	Simulation	Xilinx Plus	✓	✓			✓			
		Peak FPGA	2.20	Synthesis	Included	✓	✓	✓		✓			
	ACEO Technology, Inc.	Asyn	4.1	Synthesis	Included	✓	✓		✓	✓	✓	✓	✓
		Softwire	3.3	Multi-FPGA Partitioning	Included	✓	✓		✓	✓	✓	✓	✓
		Gatran	3.3	ASIC to FPGA Netlist Mapping	Included	✓	✓		✓	✓	✓	✓	✓
	Acugen Software, Inc.	Sharpeye	2.60	Testability Analysis	AALCA interface	✓	✓	7k		✓	✓		✓
		ATGEN	2.60	Automatic Test Generation	AALCA interface	✓	✓	7k		✓	✓		✓
		AAF-SIM	2.60	Fault Simulation	AALCA interface	✓	✓	7k		✓	✓		✓
		PROGBSDL	2.63	BSDL Customization	AALCA interface	✓	✓	7k		✓	✓		✓
		TESTBSDL	2.63	Boundary Scan ATG	AALCA interface	✓	✓	7k		✓	✓		✓
	ALPS LSI Technologies	Edway Design Systems		Synthesis/Simlulation		✓		✓		✓			
	Aptix Corporation	System Explorer	3.1	System Emulation	Axess 3.1	✓	✓	✓			✓		✓
		ASIC Explorer	2.3	ASIC Emulation	Axess 2.3	4K	✓		✓				
	Aster Ingenierie S.A.	XILLAS	4.2	LASAR model generation	Worst Case Simulation	✓		7k		✓	✓		✓
	Auspy Development Co.	APS	1.2.3	Multi-FPGA Partitioning	Included	✓				✓	✓		
	Chronology Corporation	TimingDesigner	3.0	Timing Specification and Analysis	Included	✓	✓	7k,9k	✓	✓	✓		✓
		QuickBench	1.0	Visual Test Bench Generator	Included	✓	✓	7k,9k	✓	✓	✓		✓
	CINA-Computer Integrated Network Analysis	SmartViewer	1.0e	Schematic Generation	XNF Interface	✓		7k		✓			
	Epsilon Design Systems	Logic Compressor		Synthesis optimization		✓	✓			✓	✓	✓	✓
	Flynn Systems	Probe	3.0	Testability Analysis	Xilinx Kit	✓	✓	7k		✓			
		FS-ATG	3.0	Test Vector Generation	Xilinx Kit	✓	✓	7k		✓			
		CKTSIM	3.0	Logic Analysis	Xilinx Kit	✓	✓	7k		✓			
		FS-SIM	3.0	Simulation	Xilinx Kit	✓	✓	7k		✓			
	Fujitsu LSI	PROVERD		Top-Down Design System	Included	3k,4k				✓			
	Harmonix Corporation	PARTHENON	2.3	Synthesis		4k		7k		✓	✓		
	Logical Devices	Total Designer	4.7	Simulation & Synthesis	Call Xilinx	✓	✓	✓	✓	✓			
		Ulysa	1.0	VHDL Synthesis	Call Xilinx	✓	✓	✓	✓	✓			
	MEMEC Design Services	One-Hot State Mach. Lib.		Grph. Design for One-Hot S.Mach	Xilinx Kit	✓	✓		✓	✓	✓	✓	✓
	MINC	PLDesigner-XL/PL-Synthesizer	3.3/3.2.2	Synthesis	Xilinx Design Module	✓				✓	✓		✓
	Teradyne	Lasar	6	Simulation	Xilinx I/F Kit	✓					✓		✓
	Tokyo Electron Limited	ViewCAD	1.2	FLDL to XNF translator	XNFGEN	✓							
	Trans EDA Limited	TransPRO	1.2	Synthesis	Xilinx Library	✓					✓		✓
	Visual Software Solutions	Statecad	3.0	Grph. Design Entry, Sim., Debug		✓	✓	✓	✓	✓	✓		✓
	Zuken	Tsutsuji		Synthesis/Simulation	XNF Interface	3k,4k					✓	✓	✓
	Zycad	Paradigm RP		Rapid Prototyping		✓					✓		✓
		Paradigm XP		Gate-level Sim		✓					✓		✓

Items that have changed since the last issue (XCell 22) are in color.
The following entry was removed: The Rockland Group.

Diamond: These partners have strong strategic relationships with Xilinx and have a direct impact on our releases. Typically, Xilinx is directly involved in the development and testing of the interface to XACT*step* software for these products.

Ruby: These partners have a high degree of compatibility and have repeatedly shown themselves to be significant contributors to our users' development solutions.

Emerald: Proven Xilinx compatibility

XILINX ALLIANCE-EDA CONTACTS-NOVEMBER 1996

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Changes since last issue (XCell 22) printed in color. • *The following two entries deleted: ITS, The Rockland Group*

XILINX RELEASED SOFTWARE STATUS-NOVEMBER 1996

XILINX INDIVIDUAL PRODUCTS

Key	Product Category	Product Description	Product Function	Xilinx Part Reference Number	Current Version by Platform PC1 *6.2*	SN2 *4.1.x*	HP7 *9.01*	Last Updt Comp	Previous Version Release	Notes/ Features
	CORE XEPLD	XC7K Support	Core Implementation	DS-550-xxx	6.0.1	5.2.1	5.2.1	7/96	5.2/6.0	PC update by request only
*	XABEL-CPLD	XC7K, XC9500 Support	Entry/Simulation/Core	DS-571-PC1	6.1.1			7/96	6.10	New version w/XC9500; First ship 4/29/96
*	XACT-CPLD	XC7K, XC9500 Support	Core + Interface	DS-560-xxx	6.0.1	6.0.1	6.0.1	7/96	6.0	
	Mentor	8.4=A.4	Interface and Libraries	DS-344-xxx		5.2.1	5.2.1	7/96	5.20	
	OrCAD		Interface and Libraries	DS-35-PC1	6.0.1			7/96	6.0	Support for SDT+, VST+ v1.2
	Synopsys		Interface and Libraries	DS-401-xxx		5.2.1	5.2.1	7/96	5.20	Includes XC5200 X-BLOX Support
	Viewlogic	PROcapture	Interface and Libraries	DS-390-PC1	6.0.1			7/96	5.2/6.0	Includes PRO Series 6.1
	Viewlogic	PROsim	Interface and Libraries	DS-290-PC1	6.0.1			7/96	6.0	Includes PRO Series 6.1
	Viewlogic		Interface and Libraries	DS-391-xxx	6.0.1	5.2.1	5.2.1	7/96	6.0	
	XABEL		Entry,Simulation,Lib, Optimizer	DS-371-xxx	5.2.1	5.2.1	5.2.1	7/96	5.2/6.0	Now available on HP7
	XBLOX		Module Generator & Optimizer	DS-380-xxx	5.2.1	5.2.1	5.2.1	7/96	5.2/6.0	
E	Verilog	2K,3K,4K,7K Libraries	Models & XNF Translator	ES-VERILOG-xxx		1.00	1.00	na	na	Sun and HP
E	XC4000EX	XC4000EX Support	Core Implementation	DS-4EX-WS		beta	beta	na	na	Available to pre-determined users

XILINX PACKAGES

		Silicon Support 2K	3K	4K/E	5K	7K	9K						
	Cadence	X	X	X	X	X	X	DS-CDN-STD-xxx		5.2.1	5.2.1	7/96	5.20	
	Mentor	X	X	X	X	X	X	DS-MN8-STD-xxx		5.2.1	5.2.1	7/96	5.20	No AP1 update
	Mentor	X	X	X	X	X	X	DS-MN8-ADV-xxx		7.00	7.00	na	na	
U	OrCAD	X	X	X	X	X	X	DS-OR-BAS-PC1	6.0.1			7/96	6.0	Customer w/v6.0 will receive v6.0.1 update
	OrCAD	X	X	X	X	X	X	DS-OR-STD-PC1	6.0.1			7/96	6.0	
	Synopsys		X	X	X	X	X	DS-SY-STD-xxx		5.2.1	5.2.1	7/96	5.20	Includes DS-401 v5.2
	Synopsys		X	X	X	X	X	DS-SY-ADV-xxx		7.00	7.00	na	na	Includes DS-401 v5.2
U	Viewlogic	X	X	X	X	X	X	DS-VL-BAS-PC1	6.0.1			7/96	6.0	Customer w/v6.0 will receive v6.0.1 update
	Viewlogic	X	X	X	X	X	X	DS-VL-STD-xxx	6.0.1	5.2.1	5.2.1	7/96	5.26.0	DA1 platform remains at v6.0
	Viewlogic	X	X	X	X	X	X	DS-VL-ADV-xxx	7.00	7.00	7.00	na	na	
	Viewlogic/S	X	X	X	X	X	X	DS-VLS-BAS-PC1	6.0.1			7/96	6.0	Includes PROSeries 6.1
	Viewlogic/S	X	X	X	X	X	X	DS-VLS-STD-PC1	6.0.1			7/96	6.0	Includes PROSeries 6.1
	Viewlogic/S	X	X	X	X	X	X	DS-VLS-EXT-PC1	6.0.1			7/96	6.0	Incl PROSeries 6.1/PROsynth 5.02X
	Viewllogic/S	X	X	X	X	X	X	DS-VLS-ADV-PC1	7.00			na	na	
U	3rd Party Alliance	X	X	X	X	X	X	DS-3PA-BAS-xxx	6.0.1			7/96	na	Customer w/v6.0 will receive v6.0.1 update
	3rd Party Alliance	X	X	X	X	X	X	DS-3PA-STD-xxx	6.0.1	5.2.1	5.2.1	7/96	5.2/6.0	Includes 502/550/380
	3rd Party Alliance	X	X	X	X	X	X	DS-3PA-ADV-xxx	7.00	7.00	7.00	na	na	Includes 502/550/380 & Foundry
	Foundation Series	X	X	X	X	X	X	DS-FND-BAS-PC1	6.0.1			7/96	6.0	Includes support for XC4000E and XC9500
	Foundation Series	X	X	X	X	X	X	DS-FND-BSV-PC1	6.0.1			7/96	6.0	Includes support for XC4000E and XC9500
	Foundation Series	X	X	X	X	X	X	DS-FND-STD-PC1	6.0.1			7/96	6.0	Includes support for XC4000E and XC9500
	Foundation Series	X	X	X	X	X	X	DS-FND-STV-PC1	6.0.1			7/96	6.0	Includes support for XC4000E and XC9500
	LogiCore-PCI Slave			X				LC-DI-PCIS-C	1.10	1.10	1.10	na	na	Requires signed license agreement
	LogiCore-PCI Master			X				LC-DI-PCIM-C	1.10	1.10	1.10	8/96	1.0	Requires signed license agreement
	Evaluation	X	X	X	X	X	X	DS-EVAL-XXX-C	2.00	2.00	2.00	na	na	PC, Sun, HP kits with v5.2.1 and v6.0.1

***KEY**: N=New Product E= Engineering software for in-warranty users by request only U= Update by request only * = Check BBS or FTP site.*

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