XCELL

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XILINX®

The Programmable Logic Company℠

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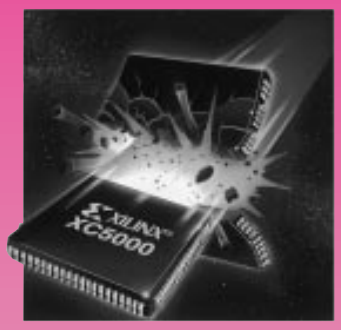
XC5200 FPGAs: Prices Go Down and Performance Goes Up



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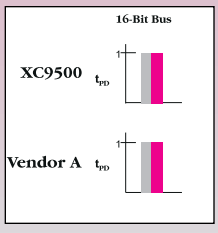

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Reconfigurable Computing: Coming of Age

By BRADLY FAWCETT ◆ Editor

This past June, Xilinx held its first Reconfigurable Computing Developer's Program Conference at a hotel in Santa Clara, not far from company headquarters. Planned to be an annual event, the conference brought together representatives from 11 of the more than 20 companies that are participants in the Developer's Program.

The Reconfigurable Computing (RC) Developer's Program was founded in mid-1995 to proactively spur commercial development of reconfigurable computing applications and products *(see* XCell *#19, page 35)*. The program is designed to aid commercial companies through technical, marketing and, in some cases, financial assistance. In this context, reconfigurable computing is loosely defined as the practice of using in-system-configurable FPGAs as computing elements to accelerate operations in general-purpose computers. In these systems, FPGAs are reconfigured during system operation to perform a variety of operations directly in hardware, off-loading the host processor and dramatically increasing system performance.

> *"The conference provided some valuable insights into the nature of the nascent but growing market for RC-based products."*

Each company attending the meeting gave a short presentation about the products it has developed or is developing. Several companies brought demonstration systems to the meeting. The conference was an ideal forum for letting representatives of the member companies interact with Xilinx R&D personnel and each other.

The conference provided some valuable insights into the nature of the nascent but growing market for RC-based products. Among this small sampling, there were *two main business models.* Some companies specialize *in providing hardware and software tools to OEM accounts* that develop their own products, while other member companies are *focused on their own specific end applications.*

The first category includes Annapolis Micro Systems (Annapolis, MD), Virtual Computer Corp. (Reseda, CA), and Giga Operations (Berkeley, CA). All are making significant strides in the development of RC-based hardware platforms and software tools. One of the most interesting aspects of their presentations was the mention of the types of large corporate OEM accounts that are using or evaluating those products — names like Boeing, Ericsson, Loral, NTT, Delco, E-Systems and TRW.

Other companies are using RC-based systems in their end products to tackle a wide variety of high-performance computing tasks, ranging from satellite communications to automated searches of DNA sequences to 3-D graphic rendering for video games.

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GUEST EDITORIAL

Xilinx Takes the Lead in ISP Standardization Effort

By NEIL G. JACOBSON ◆ *Manager, JTAG Research & Development*

In-system programming (ISP) allows users to program and re-program parts that are already soldered on a system board to facilitate prototyping, streamline manufacturing flows and enable remote system updating.

As ISP proliferates, end-users are strained by the difficulty of finding third party applications solutions that address the system-level issues for the wide variety of ISP parts available. In addition, their own test and diagnostic software development costs escalate as new devices come on-line, requiring extensive programming algorithm re-work.

At the last IEEE 1149.1 (JTAG) working group meeting, it was recognized that the use of the 4-pin 1149.1 test access port (TAP) as the platform for ISP development is becoming a de facto standard among most PLD manufacturers. (For example, XC9500 family CPLDs are always programmed through the TAP, and XC4000 series FPGAs optionally can be programmed through the TAP). The working group chose to take a active role in bringing an ISP extension to 1149.1 under its purview, with Xilinx taking the lead in this effort.

Xilinx and Hewlett Packard organized a meeting of more than 30 participants from about 20 companies. This first 'study group' meeting was held on April 19 at Hewlett Packard's Manufacturing Test Division in Loveland, CO. The attendees included PLD manufacturers such as Xilinx, Altera, Lattice, AMD, Cypress and IBM; third-party tool manufacturers such as Asset Intertech, Corelis, Intellitech and APG Test Consultants; automatic test equipment manufacturers such as HP, GenRad and Teradyne; and ISP end-users such as Cisco Systems and HP.

"As ISP proliferates, end-users are strained by the difficulty of finding third party applications solutions that addresss the system-level issues for the wide variety of ISP parts available."

There was broad agreement that the value of standardization was great. Immediate applications could be envisioned in fields as diverse as emulation technologies and remote field test and diagnostics. The vendor approaches to ISP were close enough to one another for the development of a standard approach to be meaningful. General consensus seems to be forming in the following areas:

A. The IDCODE and USERCODE registers are a vital part of any ISP device and will probably be made mandatory.

The XC9500 CPLD architecture already includes these optional 1149.1 functions. Indeed, not supporting these part, program content and version identification instructions makes ISP impractical since the revision level and contents of a system would be otherwise unobtainable.

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> *"The enormous potential of reconfigurable computing is beginning to attract the attention of the CAE tool vendors."*

Products that have already reached the marketplace include *Digital Wings for Audio* from Metalithic Systems (Sausalito, CA), satellite ground station communications systems from TSI Telsys (Columbia, MD), the *DeCypher II* 'Genetics Supercomputing PC' from Time Logic (Incline Village, NV), and the *X-CIM* line of DSP acceleration modules from MiroTech Microsystems (Saint Laurent, Quebec, Canada).

- Available soon in retail music equipment stores, *Digital Wings* is a 128-track audio authoring system that operates in the Windows environment on a PC (*see XCell #20, page 42*). Metalithic Systems is targeting the 'music enthusiasts' market with this product, and is developing a lower-cost version for the consumer market.
- TSI Telsys recently sold several of its satellite 'gateway' systems to NASA's Marshall Space Flight Center, where it will support programs such as the Space Station project.
- Time Logic's *DeCypher II* system, designed for screening DNA sequence data, is proving popular with both pharmaceutical companies and medical research facilities, where it outperforms multi-million-dollar supercomputers.
- MiroTech Microsystems is addressing the FPGA-based DSP market. Its DSP acceleration modules are fully

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B. The system-level issues related to ISP (i.e., safe pin states during ISP operations, describing how parts can safely initialize after ISP is completed, etc.) must be addressed.
The XC9500 ISPEN and ISPEX instructions provide a framework for protecting the user's system during ISP operations. This type of functionality is absolutely critical for developing a truly workable ISP-based system — Xilinx has it now.

C. The interchange of information should be included as part of the overall standard. Serial vector format (SVF), suitably modified, might best serve as that vehicle.
The EZTag software generates SVF files to describe all XC9500 ISP operations.

D. The RUN-TEST/IDLE state is the "action" state in which programming or erase latency times are spent.
This is exactly the way XC9500 parts function.

A final report will be made to the 1149.1 working group at the International Test Conference in October. At that time, it will be decided whether to pursue this as a separate standard within the 1149 framework or as an application of the 1149.1 standard.

Either way, Xilinx has already equipped the new XC9500 family with the industry's best JTAG/ISP capabilities and is spearheading the next generation of programming and testing standards. ◆

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compliant with Texas Instrument Modules (TIM) specifications and are supported by a library of common DSP functions. MiroTech has signed an OEM agreement with a major manufacturer of DSP boards.

The remaining companies at the conference previewed products in development. enVia Inc. (Menlo Park, CA) is developing consumer telecommunications equipment that uses reconfigurable FPGAs to address the growing problem of incompatible wireless telecommunications standards. Octree Corp. (Cupertino, CA) has implemented 3D volume rendering systems on Annapolis Micro Systems and Giga Operations platforms, and is developing products for both medical equipment and video game manufacturers. Start-up Adaptive CAD Technologies (Sunnyvale, CA) and consulting firm Memec Design Services (Garden Valley, CA) also attended, and are applying RC technology in some new application areas (but it's too early to reveal them).

Another encouraging sign was the presence of representatives from several of the CAE companies in the Xilinx Alliance Program. The enormous potential of reconfigurable computing is beginning to attract the attention of the CAE tool vendors. For many of these vendors, this conference was their first chance to talk with the early adopters of reconfigurable computing technology; it is certainly not inconceivable that some cooperative product development efforts will eventually result from this meeting.

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In summary, reconfigurable computing technology is continuing to 'come of age,' with several companies already garnering revenue from a wide variety of RC-based products, penetration of RC technology into large, well-known electronic equipment manufacturers, and the attention of leading design tool vendors. I'm already looking forward to next year's conference. ◆

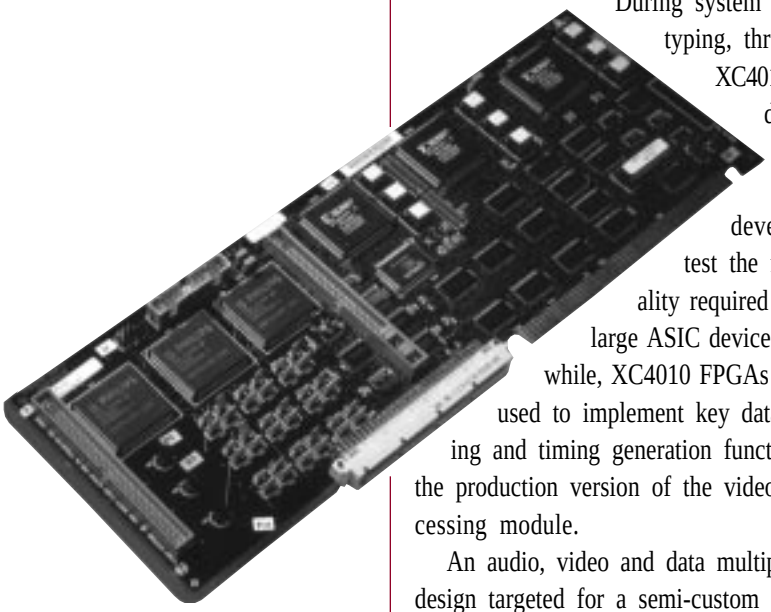
Sharp-eyed readers may notice a slight change to the format of *XCell* in this issue. The tables listing component availability, Xilinx software status, Alliance partner information, and device programmer status have been moved from the "General Information" section to the last few pages of the newsletter. As a few readers have suggested, this will make the tables easier to find as well as providing for better continuity for those who read the whole journal front-to-back.

We are always interested in reader feedback. This issue includes a short reader survey on page 47. We would greatly appreciate if you would take a few minutes to fill out this questionnaire and mail or FAX it back to us. Alternatively, you can send your comments directly to me via E-mail at brad.fawcett@xilinx.com. We're looking forward to hearing from you. ◆

Videoconferencing with XC4000 FPGAs

GPT Video Systems (Maidenhead, Berks, U.K.) designs and manufactures high-quality videoconferencing solutions under the brand name FOCUS. GPT Video Systems is a long time user of Xilinx products; its designers use FPGA technology to maintain the flexibility and rapid time-to-market required in the fast moving multimedia market.

The flexibility of FPGA technology was evident in the design of the latest FOCUS videoconferencing systems, where XC4000™ series FPGAs were used for both prototyping and production applications.



During system prototyping, three XC4013 devices were used to develop and test the functionality required for a large ASIC device. Meanwhile, XC4010 FPGAs were used to implement key data routing and timing generation functions in the production version of the video processing module.

An audio, video and data multiplexer design targeted for a semi-custom gate array implementation was prototyped with three XC4013 devices. The development was carried out using Cadence Verilog software running on a Sun SparcStation. The FPGAs provided a fast and flexible development route, culminating in a fully-functional ASIC on the first try. The ASIC device holds about 30,000 gates of logic, with a 20 MHz system clock rate. Verifying the design with the FPGAs saved significant additional NRE costs and development time that would have been incurred if changes to the design had been required after committing to custom silicon. Furthermore, this development route allowed beta versions of the system to be shipped with the FPGA solution before production volumes of the ASIC were available, further accelerating time-to-market.

Three XC4010 FPGAs hold the majority of the logic in the video processing module in the main codec design. Two of the FPGAs share a common design and act as video routers, passing CCIR601 digital video data from various input sources to the desired outputs. Each device is designed to route data in the form of an 8-bit data bus, requiring two to be used for the 16-bit data in the CCIR601 format. Thus, one device handles the routing and control of the luminance data, and the other handles the chrominance data.

These two devices also perform the task of overlaying the graphical user interface directly onto the video outputs. This includes a patented function that produces semi-transparent video, allowing on-screen text to be displayed in an easily-readable format while not obscuring the live video beneath. The design makes specific use of the XC4000 architecture's on-chip RAM capability to implement fast look-up tables.

The third XC4010 FPGA in the video processing module is a timing generator, providing all the timing functions for the various video field store read and write operations. This FPGA also contains the state machines that control the reading and writing of captured video images to and from the graphics frame stores.

The XC4010 designs were entered using a combination of schematic capture and ABEL hardware descriptions and verified with the ViewSim simulator, using a PC-based Viewlogic environment. All three FPGAs are about 80% full and run at a system clock speed of 13.5 MHz, a

performance level that was easily reached using timing constraints and automatic placement and routing tools.

To further reduce hardware costs during volume production of the codecs, the XC4010 FPGA designs were frozen and converted into HardWire™ XC4310 devices. Since the HardWire devices are pin and function compatible with the FPGAs that they replace, system flexibility is maintained; the HardWire devices can be replaced with newly-designed FPGAs if the design evolves at a later date. According to Richard McCandless, Project Leader at GPT Video Systems, "The HardWire conversion went extremely well, with very little engineering effort required at all, and they came in on time! In fact, it surprised us how little engineering effort was needed."

As noted by McCandless, "These video interface designs were fairly complex, but the FPGAs proved to be very flexible and easy to work with. The high level of integration provided by the FPGA devices has helped to create the most user-friendly graphical user interface in the video-conferencing industry." ◆

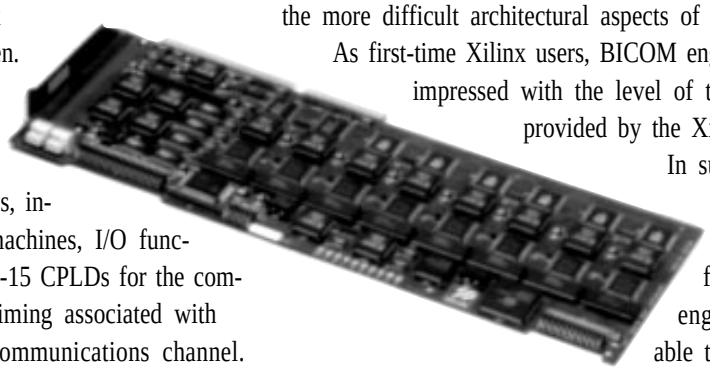
Video Processing With XC7300 CPLDs

BICOM, Inc., (Monroe, CT) is a provider of hardware and software "building blocks" for developing a wide range of voice processing applications. BICOM's products are used in the development of systems for voice mail, interactive voice response, audiotex, dictation and call center management.

The recent design of their new Gemini series of high-density computer telephony platforms required a high-performance CPLD to integrate a variety of logic functions. With cost and ease-of-use considerations in mind, the Xilinx XC7300™ CPLD family was chosen.

The voice processing board contains 14 XC7336 devices. The XC7336-5 CPLDs are used to hold a variety of logic functions, including address decoders, state machines, I/O functions and glue logic, with XC7336-15 CPLDs for the complicated timing associated with the telecommunications channel. If BICOM had used traditional PALs for these logic functions, the design would have encompassed two boards rather than one.

The design was entered and implemented on a PC using OrCAD schematic entry tools. The complexity of the design (which included a mix of analog and digital technologies) and tight development schedules dictated the use of programmable devices with predictable performance and good pin-locking capabilities. The XC7336 CPLD fulfilled both these needs. Pinouts were preassigned and maintained throughout multiple design iterations. This allowed the designers to concentrate on the more difficult architectural aspects of the design.



As first-time Xilinx users, BICOM engineers were impressed with the level of technical support provided by the Xilinx team.

In summary, by using the XC7300 CPLD family, BICOM engineers were able to meet their performance needs, reduce design complexity and cost, and save valuable board space as well. ◆

Xilinx Helps Fund New Seiko-Epson Foundry

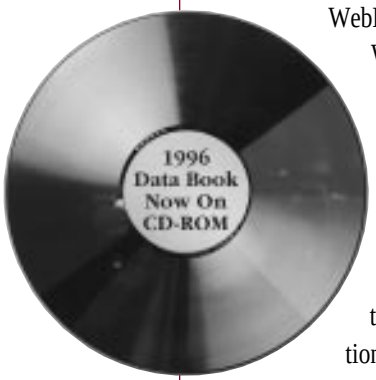
Xilinx has announced its funding of up to $300 million for the construction of a new semiconductor manufacturing facility. The facility will be built and operated by Seiko-Epson Corp. in Sakata, Japan (about 200 miles north of Tokyo). Xilinx will make incremental advance payments over the next two and one-half years to help finance construction of the facility. In return, Xilinx will receive a specified number of wafers from the new line through the year 2002.

The new operation will manufacture 8" wafers using advanced 0.35 to 0.25 micron CMOS technology. In time, these advanced processes will enable the development of programmable logic devices with capacities reaching 500,000 gates. Production at the facility is expected to begin in early 1998.

"We're confident that our continuing partnership with Seiko-Epson will enhance our competitive position and allow us to design products with ever higher densities and faster performance, " stated Xilinx Chief Executive Officer Willem Roelandts. "Just as important, it will help us meet growing customer demand worldwide for our products into the next century."

This investment agreement further strengthens the close relationship between Xilinx and Seiko-Epson; Seiko-Epson has been a supplier to Xilinx for more than a decade. Xilinx also will maintain its existing foundry partnerships with Yamaha, Taiwan Semiconductor Manufacturing Company (TSMC), United Microelectronics Corporation (UMC) and IC Works. As reported in *XCell #20*, Xilinx owns a 25% equity stake in a new foundry being constructed by UMC in Taiwan and scheduled to come on-line in the first half of 1997. ◆

New Data Book Now Available



Both CD-ROM and printed versions of the new "Xilinx Programmable Logic Data Book" are now available. The material in the new data book also is available on WebLINX™, the Xilinx World Wide Web site (www.xilinx.com), in the form of individual product specifications.

The CD-ROM, a first with this edition, works with PCs, Sun workstations, and HP workstations. Detailed tables of contents and the ability to search for keywords makes the CD-ROM a valuable tool. The entire data book resides in a single ".pdf" file. The Acrobat™ Reader program (that allows users to view .pdf files) and its installer are included on the CD-ROM. The main table of contents, chapter tables of contents and the index all include hypertext links to immediately jump to the appropriate pages in the book.

At 900 pages, the data book includes data sheets for the XC7300, XC9500, XC3000A/L, XC3100A/L, XC4000E, XC4000EX/XL, XC5200, XC6200, and XC1700D device families. Product specifications for the older XC2000, XC3000, XC3100, and XC4000/A/H/D/L families are not included, but are still available on WebLINX. The military/high-reliability and HardWire™ product lines are overviewed, but detailed product specifications are still found in separate, dedicated documents.

To obtain a copy, contact your local Xilinx sales representative. ◆

What's New on WebLINX™

Xilinx Home Page • www.xilinx.com

WebLINX was recently named an Infoworld HotSite! Here are a few of the reasons why:

- **SmartSearch™ Agents Released**
  Come visit the industry-wide search engine made specifically for topics involving programmable logic. You can create your own agents to notify you by e-mail as material you want becomes available in any of multiple sites on the web.
- **Xilinx Guided Tour**
  Check out this on-line company and product overview covering topics such as Xilinx corporate and product strategies, device selection, XACT*step*™ software solutions, quality assurance and Xilinx technical support services.
- **Product Spotlights**
  Examine a showcase of our latest products, currently featuring the XC4000EX and XC9500 device families and the Foundation Series software, with its easy-to-use, low-cost VHDL synthesis solution.
- **On-Line Net Seminars**
  In cooperation with Marshall Industries, Xilinx holds live seminars on the Internet, complete with an on-line slide and audio presentation and a live chat-response forum for asking questions. Recorded seminars on the XC5200 and XC9500 device families also are available to review at your convenience. ◆

TECHNICAL TRAINING UPDATE

Both Schematic- and Synthesis-Based Classes Offered

Two basic classes are available from Xilinx, a **schematic-based** and a **synthesis-based** class.

Actually, both classes focus more on overall design methodologies for using Xilinx devices, rather than the specific front-end tools. (The tutorials shipped with the development systems provide the specific tool training for the new user.) The schematic-based class has traditionally utilized ViewLogic tools in the examples and labs. However, with the introduction of XACT*step* version 6.0.1, the class has been updated to use the Foundation™ Development System and its front-end tools from Aldec.

The synthesis-based class uses the Synopsys tools. The course goes beyond explaining and demonstrating the basic concepts behind HDL-based design by examining many of the specific language constructs that should be used when designing with these tools.

All designers can benefit from taking one of these classes. Even designers already familiar with Xilinx technology can learn some new methods to reduce design time and increase device performance.

Remember, either class (and even customized classes) can be presented right at your own facility. Please contact your local Sales office or our training registrar with your needs. The latest schedule of classes and contact information is always available on WebLINX, our World Wide Web site (www.xilinx.com). ◆

New Product Literature

Learn about the newest Xilinx products and services through our extensive library of product literature. The most recent pieces are listed below. To order or to obtain a complete list of all available literature, please contact your local Xilinx sales representative. ◆

TITLE	DESCRIPTION	NUMBER
1996 Programmable Logic Data Book	*Technical Data*	0010303
1996 Programmable Logic Data Book on CD-ROM	*Technical Data*	500360
Product Overview Brochure	*Features & Benefits*	0010130-05
Software Selector Guide	*Features & Benefits*	0010304
FPGA Brochure	*Features & Benefits*	0010305

UPCOMING EVENTS

Look for Xilinx technical papers and/or product exhibits at these upcoming industry forums. For further information about any of these conferences, please contact Kathleen Pizzo (Tel: 408-879-5377 FAX: 408-879-4676). ◆

EuroDAC & EuroVHDL
Sept. 16-20
Geneva, Switzerland

International Workshop on Field Programmable Logic and Applications
Sept. 23-25
Darmstadt, Germany

PCI Europe
Oct. 1-2
Paris, France

DSP Germany
Oct. 1-2
Munich, Germany

DSP World/ICSPAT
Oct. 8-10
Boston, MA

Silicon Design Conference
Oct. 9-10
Birmingham,
United Kingdom

WESCON
Oct. 22-24
Anaheim, California

DSP France
Oct. 22-24
Paris, France

Electronica
Nov. 12-15
Munich, Germany

Photonics East
Nov. 18-22
Boston, Massachusetts

BIAS & DSP Italy
Nov. 26-29
Milan, Italy

DSP UK
Dec. 3-4
London, United Kingdom

FINANCIAL RESULTS

Quarterly Revenue Tops $150M

Sales revenues rose to $150.2 million in the first fiscal quarter of 1977 (ending June 30, 1996), a 19% increase over the same quarter one year ago and a 0.3% increase from the immediately preceding quarter.

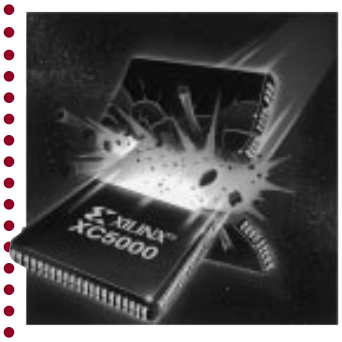
"The June quarter was a difficult quarter for the semiconductor industry," noted Xilinx Chief Executive Officer Willem Roelandts. "Although Xilinx was not immune to this widespread slowdown, we did experience minor sequential revenue growth. The bright spot was the North American distribution channel, which grew 10% over the prior quarter."

The XC5000 FPGA family continued its torrid growth rate, with sales up 30% over the previous quarter. Recently announced price cuts *(see page 11)* should even further expand the market for this cost-optimized FPGA family.

Xilinx stock is traded on the NASDAQ exchange under stock symbol XLNX. ◆

XC5200 Family:

Lower Prices & Higher Performance



Xilinx recently announced significant price reductions and performance improvements for the XC5200 FPGA family, further advancing its position as the industry's most cost-effective FPGA family.

Prices Reduced by up to 50%

XC5200 sales have risen at a record pace. The rapid increase in shipments and a shift to a 0.5 µ process have resulted in significant cost advantages; these savings are being passed on directly to our users. With its segmented interconnect structure and an architecture optimized for its submicron, triple-layer metal (TLM) process, the XC5200 FPGA family has a significant technological advantage over other architectures. The family's small die sizes — in some cases even approaching today's gate array die sizes — lead to correspondingly low component costs.

The chart below shows current high-volume pricing and projected pricing one year from now.

XC5200 Family Volume Pricing*

Device	Maximum Logic Gates	End of 1996	2H97
XC5202	3K	$5.00	**$4.50**
XC5204	6K	$10.00	**$8.00**
XC5206	10K	$17.00	**$12.00**
XC5210	16K	$27.00	**$18.00**
XC5215	23K	$47.00	**$33.00**

** Plastic package, -6 speed grade, 25,000 unit quantity, U.S. direct pricing only*

Performance Improved by 30%

In addition to price reductions, a patented charge-pump transistor design has been added to the XC5200 family. When combined with a semiconductor process shrink from 0.6µm to 0.5µm triple-layer metal technology, the result is a new -3 speed-grade that offers up to a 30% performance improvement over the -5 speed grade *(see table)*.

The XC5200 family delivers 2,000 to 23,000 usable gates and robust features, such as the VersaRing™ I/O interface that maximizes overall utilization and pin assignment flexibility, dedicated JTAG boundary scan logic for increased testability, and fast carry logic for high speed arithmetic functions. The XC5200 FPGA family continues to lead the industry as the lowest cost/gate programmable logic solution. ◆

XC5200 Performance Benchmarks

	XC5210-5	XC5210-3	%Improvement
16-Bit Decoder	8 ns	6 ns	**25%**
24-Bit Accumulator	39 MHz	50 MHz	**28%**
16-to-1 Multiplexer	13 ns	9 ns	**31%**
16-Bit Adder	20 ns	15 ns	**25%**
16-Bit Up/Down Counter	50 MHz	65 MHz	**30%**

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XC7300 CPLDs & XABEL-CPLD: The Industry's

The combination of ultra-low-cost 44-pin XC7300 CPLDs and easy-to-use XABEL-CPLD development software provides users with the best value in programmable logic. Three XC7300 family members are now available in 44-pin PLCC, PQFP or VQFP packages — the XC7336, XC7336Q and XC7354 devices.

Xilinx 44-pin XC7300 CPLDs provide a greater range of performance and significantly lower costs than PALs and GALs. In fact, the logic from several PAL /GAL devices can be integrated into a single XC7300 CPLD at a lower device cost than the replaced PALs/GALs (and sometimes at a component cost equivalent to a single high-speed PAL). The XC7300 CPLDs also can replace TTL bus drivers, further reducing component count and cost. Advanced system features such as 3.3V or 5V I/O signaling levels and 100% PCI compliance provide support for the newest CPUs and high-performance memories.

44-pin CPLDs also have proven extremely adept at fixing " broken" ASICs. ASIC users are discovering that 44-pin CPLD solutions can be used to safeguard or repair ASIC functionality. Sometimes fixed-function ASICs can be rendered "unusable" by specification changes, process variations that disrupt system timing or design errors. Planning ahead by reserving board space for a small form factor, 44-pin CPLD can provide ASIC designers with "system insurance." The CPLD can be used to implement control circuitry or correct sensitive timing paths. In this way, the flexibility to fix unwanted surprises is built-in to the design.

	XC7336	XC7336Q	XC7354	BENEFITS
22V10 equiv. 16V8 equiv.	3 4	3 4	5 6	lower inventory & production costs
macrocells	36	36	54	
usable gates	800	800	1500	
t_{PD}	5.0 ns	10 ns	7.5 ns	XC7336-world's fastest CPLD
I_{CC} (typ.)	126 mA	50 mA	140 mA	Significant power savings over multiple PALs/GALs
3.3V/5V I/O	Y	Y	Y	Interface with high performance memories and MPUs
24 mA high drive I/O	Y	Y	Y	PCI Bus compliance
packages	PC44, PQ44	PC44, PQ44, VQ44	PC44	VQ44 53% smaller than PC44

Push-Button Software Gets the Job Done

Low-cost XABEL-CPLD software obsoletes all PAL/GAL and low-end CPLD tools and provides push-button ease of use. Based on ABEL 6.0, XABEL-CPLD offers instant productivity enhancement to all PAL/GAL users and makes the migration to higher-density, cost-effective CPLD technology quick and easy.

The combination of highly-capable, low-cost silicon and software makes Xilinx 44-pin CPLD solutions the best choice in a world where product development schedules and system component budgets are shrinking at an ever-accelerating pace.

continued

Best 44-Pin PLD Value

FEATURES	BENEFITS
Familiar Data I/O ABEL, Windows-based environment for design entry, simulation and fitting	Push button design flow improves productivity
Industry-standard-ABEL- HDL supports state machines, high level logic descriptions, truth tables and equation entry	ABEL-HDL familiar to PAL users, optimized for PAL and CPLD development
Hierarchical design entry and JEDEC file conversion for integration of existing PAL designs into Xilinx CPLDs	Enables reuse of existing PAL codes, simplifying design effort
Functional simulation with graphical Waveform Viewer and Static Timing Reports	Facilitate rapid design verification
Advanced XACT*step*v6 XC7K & XC9K fitter with automatic device selection, multiple pass optimization, partitioning and mapping, and timing driven fitting	Fitter's architecture-specific knowledge frees the user to focus on design functionality
Animated tutorial and on-line help	Reduces learning curve: • tutorial leads users through entire design process in minutes - extensive on-line help places all documentation a mouse-click away

ANNOUNCEMENT

XC8100 FPGA Product Family is Discontinued

Citing the strong market succcess of SRAM and FLASH technologies, Xilinx announced on Aug. 31, 1996, that it will discontinue the XC8100™ family of one-time programmable antifuse FPGA devices. The XC8100 family, first introduced last autumn, was just entering production.

No layoffs or reductions in R&D spending are associated with this decision. Xilinx employees involved with antifuse development are taking on new duties in other areas of the company. Resources and research and development spending are being redirected to focus more effectively on SRAM-based FPGAs, CPLDs and new opportunities more closely aligned with those products, such as LogiCore modules.

"The XC8100 team successfully developed a number of patented, industry-first innovations in antifuse architecture, design, programming and processes — accomplishments no one else in the entire semiconductor industry has been able to achieve so far with this difficult technology," stated Xilinx CEO Wim Roelandts.

"But, compared to SRAM development, there are very few people working in antifuse. As a result, antifuse will lag behind SRAM, entail disproportionately large development costs, and be relegated to limited markets. For these reasons we believe further investment in antifuse product development are too large to be justified."

A number of options are available to support current XC8100 users, including assistance in moving designs to other pin-compatible Xilinx devices, software upgrades to support other programmable logic products and refunds for XACT*step*™ 8000 software. ◆

"compared to SRAM development, there are very few people working in antifuse. As a result, antifuse will lag behind SRAM, entail disproportionately large development costs, and be relegated to limited markets."

XC4000EX Family FPGAs Entering Production

The XC4000EX family elevates the XC4000 series to new heights in density and performance, with up to 125,000 logic gates and 66 MHz system speeds. Designed "from the ground up" for speed and density using a deep-submicron, triple-layer-metal process, the XC4000EX family has abundant routing resources for high utilization and buffered interconnect to provide maximum performance. *(See* XCell *#20, page 21.)*

Xilinx has started sample shipments of the first two members of the high-density XC4000EX family. The XC4036EX, with a typical gate range of 22,000 to 65,000 gates, and the XC4028EX, with a typical gate range of 18,000 to 50,000 gates, will enter volume production in the fourth quarter of this year.

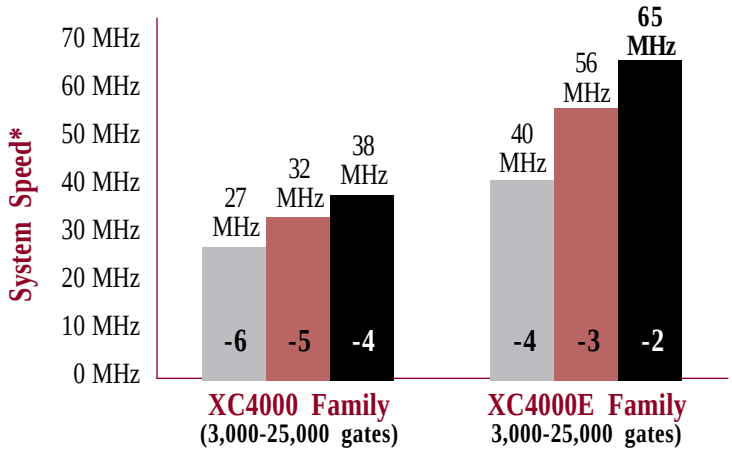
The next member of the family to be introduced is the XC4062XL, featuring a typical gate range of 40,000 to 130,000 gates. The XC4062XL will begin sampling in December. ◆

Faster XC4000E FPGAs Now Available

Continuing process improvements have led to the release of a new, faster speed grade for XC4000E™ FPGAs, available now for every member of the device family.

The new -2 speed grade achieves a 15-20 percent performance improvement over the -3 speed grade as a result of a logic block propagation time (T_{ILO}) of 1.6 ns, clock-to-output delays (T_{OKPOF}) of under 5 ns and global-clock-to-out, pin-to-pin delays (T_{ICKOF}) ranging from 8.7 ns for the XC4003E to 10.7 ns for the XC4025E . *See* ***Figure 1*** *for a comparison of the maximum chip-to-chip system speeds of the XC4000 and XC4000E devices for their available speed grades.*

Figure 1: *Speed Grade Comparisons for XC4000 and XC4000E*



**Maximum chip-to-chip system speed*

The XC4000 series (i.e., the XC4000, XC4000E and XC4000EX families) incorporates the world's most widely used FPGA architecture with advanced features such as Select-RAM™ memory, wide edge decoders, internal three-state buffers and multiple global clock distribution networks. The high performance levels offered from the -2 speed grade, when combined with these leading-edge architectural features, further extends the range of possible applications for these popular devices.

For example, the capabilities of the XC4000E-2 device enable the delivery of the LogiCore™ PCI Initiator module — an implementation that requires extremely high performance levels, especially for FIFO buffer and registered I/O operations *(see page 17).*

For further technical information, please refer to the product specifications and application notes on WebLINX, the Xilinx web site (www.xilinx.com). For pricing and availability, contact your local Xilinx sales representative. ◆

Synopsys Introduces *FPGA Express*

New Logic Synthesis Tool Targets Xilinx FPGA Families

Xilinx Alliance member Synopsys unveiled its first entry into the Win95/Windows NT market at the Design Automation Conference in Las Vegas on June 3. "FPGA Express" is a PC-based FPGA synthesis tool for leading FPGA architectures. The first version has Xilinx XC3000 family, XC4000 series and XC5200 family support. It is scheduled for production shipment in September. Later versions will support the XC9500 CPLD family, as well as other programmable logic vendors.

FPGA Express is unique in its knowledge of Xilinx architectures and tools, allowing designers who are new to HDL to get high-quality results. The expert user will find the sophisticated controls needed to work with very challenging designs.

FPGA Express is not a rewrite of FPGA Compiler, although for compatibility it uses the same VHDL and Verilog compiler technology as Synopsys' workstation tools (Design Compiler and FPGA Compiler). FPGA Express was designed "from the ground up" with PC users specifically in mind.

The Xilinx/Synopsys relationship was key in the development of this product. "This is an excellent example of Xilinx and one of its Alliance partners working together to meet user requirements with a quality product," noted Wallace Westfeldt, manager of the Xilinx Alliance program.

Xilinx supplied architectural information and assisted in the market research, definition and development of FPGA Express. As a result, FPGA Express makes optimum use of Xilinx device features to maximize density and performance. For example, it includes an automatic module generator that can infer various operations within the HDL source, such as adders, comparators and multipliers, as well as automatically build the circuits using the dedicated carry logic in the XC4000 series and XC5200 family architectures.

FPGA Express also makes full use of complex I/O structures present in the Xilinx devices, including the clock enable feature of the XC4000E IOB registers. Global clock buffers are assigned based on an intelligent algorithm that allocates the available buffers based on clock signal fanout while

Continued on the next page

> *"FPGA Express is unique in its knowledge of Xilinx architectures and tools, allowing designers who are new to HDL to get high-quality results."*

XILINX®

FPGA Express

Continued from the previous page

filtering out gated clocks. If desired, users can specify specific input pins that need to be connected to a global buffer.

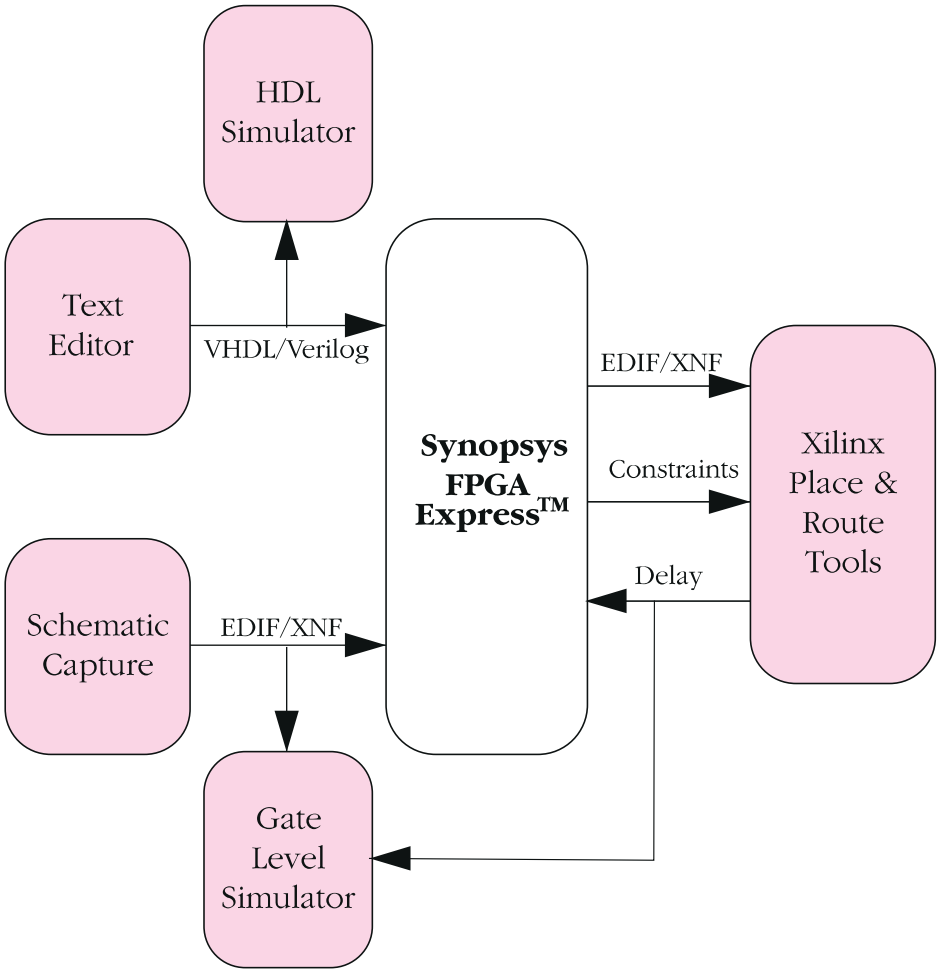
Synopsys revised the mapping and optimization algorithms to provide all HDL users with the best possible synthesis results for area, performance and predictability. Testing has shown that FPGA Express can improve area and performance by up to 25% over existing PC-based synthesis tools. Run times are excellent — a 3,000-gate design compiled in under a minute and a 20,000-gate design required approximately 10 minutes using a Pentium-class computer.

Xilinx also collaborated with Synopsys to integrate FPGA Express into the XACT*step*™ system. FPGA Express uses a sophisticated constraint-entry GUI, with an "XACT*step*-like" from/to syntax for timing constraints that directly translates to the XACT*step* TIMESPEC format. All netlist and constraint translation is done by FPGA Express, eliminating the need for external translators. The tool outputs Unified Library XNF with group TIMESPECS. The result is a "plug & play" interface between FPGA Express and the XACT*step* tools (v6.0.x and beyond).

Pricing and Availability

Sold by Synopsys, FPGA Express starts at $12,000 (one HDL language and support for one FPGA vendor). It will be available in full production in September, running on Windows 95 and Windows NT-based personal computers.

For more information about FPGA Express contact Bruce Jorgens, Product Line Manager for FPGA Products at Synopsys 415-528-4955. ◆



FPGA Express provides a smooth interface to other Xilinx FPGA development tools

LogiCore™ PCI Intitiator Debuts

Xilinx recently announced the delivery of its second, 100% compliant PCI core, the LogiCore™ PCI "Master" (Initiator/Target) module. Previously, the LogiCore PCI "Slave" (Target only) module could only perform slave functions. With the new module, a user can now complete a master interface design in which the Master module acts as a controller for the PCI bus. The implementation of critical paths in the core are pre-defined to ensure PCI compliance. As a result, designers can reduce design risk and cut development time by at least nine months.

The new -2 speed grade for the XC4013E FPGA enables the delivery of the PCI Master module, which requires a high level of design complexity and performance *(see article about -2 speed grade on page 14)*. The LogiCore PCI modules were closely developed with beta users who have successfully implemented the design in XC4013-2 FPGAs. These devices operate at 33 MHz and include high-speed burst synchronous FIFOs. The modules can be customized to fit individual design requirements, resulting in a cost-effective, single-chip solution.

The LogiCore PCI Master module (LC-DI-PCIM-C) for Xilinx FPGA and HardWire devices, complete with a data sheet, comprehensive user guide and PCI Systems Architecture textbook, is available for designing with Viewlogic schematics, VHDL and Verilog for $8,995. The PCI Slave module (LC-DI-PCIS-C) is available for $4,995.

For further information about the LogiCore PCI Interface or other modules in the program, please contact your local Xilinx representative or visit the LogiCore section of the WebLINX World Wide Web site. ◆

MEMBER
PCI LOCAL BUS
SPECIAL INTEREST GROUP

Foundation Series Enjoys Successful Introduction

The number of Foundation Series™ users has been growing rapidly since the inaugural release of this fully integrated PLD design software package in 2Q96. User feedback has been extremely positive, especially regarding the ease-of-use resulting from the tight integration of all the design tools. There also has been high praise for the HDL Wizard, including the HDL Editor, with color coding, and the Language Assistant, with templates for easy and quick coding of VHDL and ABEL-HDL.

The Foundation Series development tools for FPGA and CPLD design include a highly integrated set of Windows-based design tools. Along with the Xilinx XACT*step*™ implementation tools, it includes an HDL editor, synthesis compiler, schematic editor and simulator.

Xilinx has added more features to the Foundation packages in the v6.0.1 release, which is now shipping. Features in this release include support for the latest Xilinx device families: the XC9500 CPLDs and XC4000E FPGAs. Both device families are integrated into the easy-to-use, shrink-wrapped solution, making it simple to access and convert designs for these new families. All users who purchased Foundation v6.0 will automatically receive this new update. ◆

"Xilinx has added more features to the Foundation packages in the v6.0.1 release, which is now shipping."

Benchmarks Confirm XC9500 CPLD

The Xilinx XC9500 CPLD family provides the most-advanced, most-reliable pin-locking capability in the industry. This important feature allows designers to maintain pinouts after making design changes, eliminating costly, time-consuming PC board re-work. CPLDs that do not have adequate pin-locking capability often require pinout changes even after minor design changes, leaving no room for error and no possibility for field upgrades or field customization.

Pin-Locking Issues

In most CPLDs, each I/O pin is driven directly by a macrocell through an I/O block, as shown in **Figure 1.** When the design is pinlocked, the fitter is forced to map logic into specific macrocells to maintain the pinout. If the device architecture is limited, with inadequate routing in the central switch matrix, the fitter may not be able to place and route the design when the pins are locked.

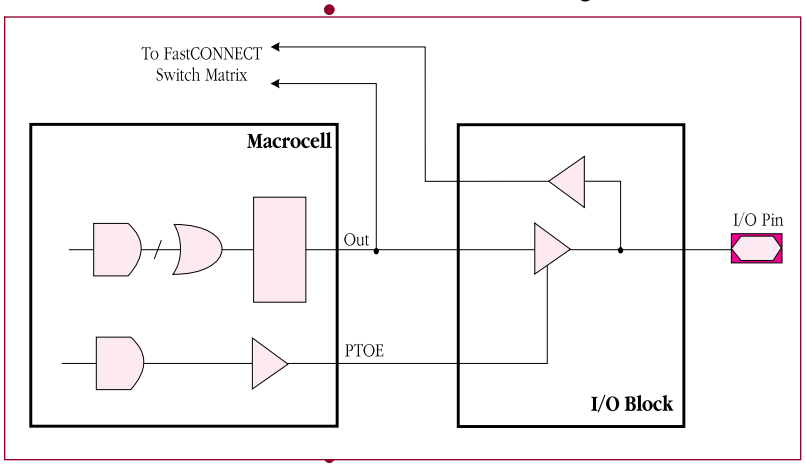


Figure 1: *Simplified XC9500 I/O Architecture*

Some CPLDs use an output routing pool to compensate for their primary routing deficiencies. However, output routing pools introduce additional delays and do not prevent the fitter from having to consume logic resources as routing feedthroughs, impacting both design performance and resource utilization.

Logic requirements also affect the ability of the fitter to place and route the design when the pinout is locked. Slow speed designs with simple, narrow logic functions requiring few inputs, feedbacks and product terms are inherently easier to pinlock than high speed designs with wide fan-in and product term intensive logic functions.

The Keys to Reliable Pin-Locking

To address these pin-locking issues, Xilinx XC9500 CPLDs feature abundant routing resources, wide function block fan-in and flexible product term allocation. The XC9500 fitter also optimizes the initial placement to maximize the design's pin-locking capability.

Pin-locking restricts the fitter's capability to place design resources; therefore, good routability is crucial. The routing resources of a CPLD determine how much of the logic block resources (inputs, product terms and registers) can be used to accommodate design changes after the pins are locked in a design. In a fully routable CPLD, buried logic can be moved without regards to routing restrictions, freeing function block resources that may be needed by the logic that drives the I/O pins.

The XC9500 family provides the most routing resources of any available CPLD family. All devices in the XC9500 family are 100% routable; if there are enough function block resources to implement the design, it will route.

Wide function block fan-in is another important requirement for pin-locking. Since CPLDs typically are used for high-speed, signal-intensive logic functions, wide function block fan-in is a requirement for implementing functions in a single logic

Pin-Locking Capabilities

level. The number of available function block inputs affects the fitter's ability to add more signals to any logic that must remain in that function block (because it drives I/O pins). Wide fan-in capability also helps the fitter implement that logic in a single pass though the device.

Each XC9500 function block has 36 inputs from the switch matrix. Competing in-system programmable CPLDs have as few as 16 inputs.

Product term allocation is important to pin-locking because it allows design changes that increase the product term requirement. All XC9500 devices allocate individual product terms from anywhere in the function block to the macrocell that needs them, accommodating logic changes when the design is pinlocked.

In the XC9500 family, up to 90 product terms can be allocated to any macrocell in the function block. This is in contrast to competing CPLDs that restrict the product term availability (from 5 to 32 pterms) on the basis of macrocell location in the function block.

Fitter software is a key component of any successful CPLD pin-locking solution. The fitter must work in conjunction with the device architecture, spreading the outputs to accommodate design changes when the design is pinlocked.

The XC9500 fitter is optimized to take full advantage of the hardware resources of the XC9500 family. The Xilinx fitter is capable of intelligently utilizing all available device resources to retain pinouts and still maintain the required performance, even after significant design changes.

The Pin-locking Benchmarks

The following three sets of benchmark data show the relative pin-locking performance of the XC9500 CPLDs and two competitor's ISP CPLD families. These benchmarks are based on typical applications such as address decoders, datapath designs and address counters. They illustrate the CPLD device's capability to accommodate design changes while maintaining an acceptable level of design performance; not only must the iterated design reroute when the pinout is maintained, it must do so with minimal impact on design performance. Therefore, all of the benchmark data is normalized to the design performance that is achieved when the fitters are free to choose the pinouts without restrictions.

"The benchmark results confirm the superior pin-locking performance of the Xilinx XC9500 family. This performance is consistent across all devices and package types."

Address Decoder Benchmark

This benchmark design contains two 16-, 32- or 36-bit busses which are decoded to generate two chip select outputs and is intended to measure the effect of routing resources and function block fan-in on the CPLD's pin-locking capability. A typical design change involves the correction of an error in which the outputs are decoded incorrectly.

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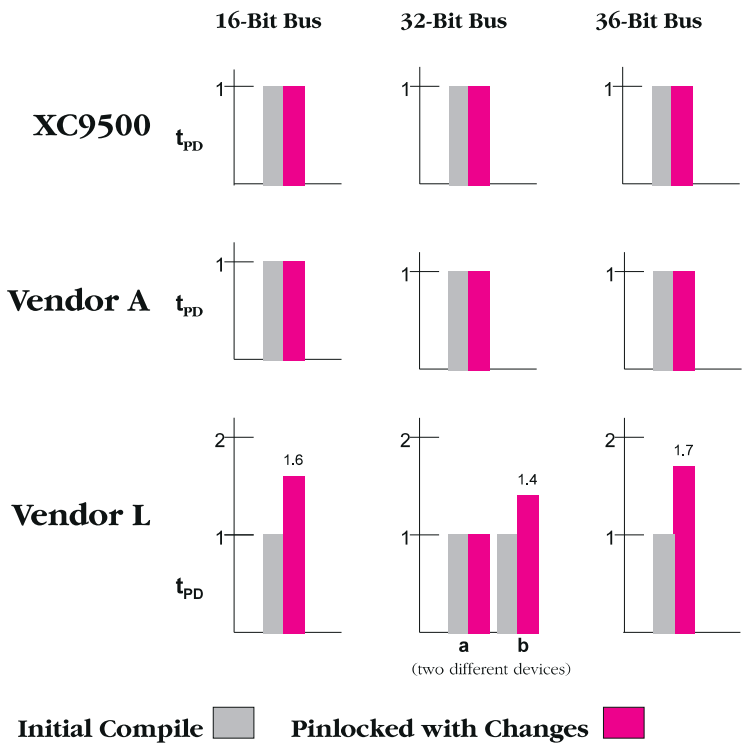

Figure 2: *Address Decoder-Normalized Benchmark Results*

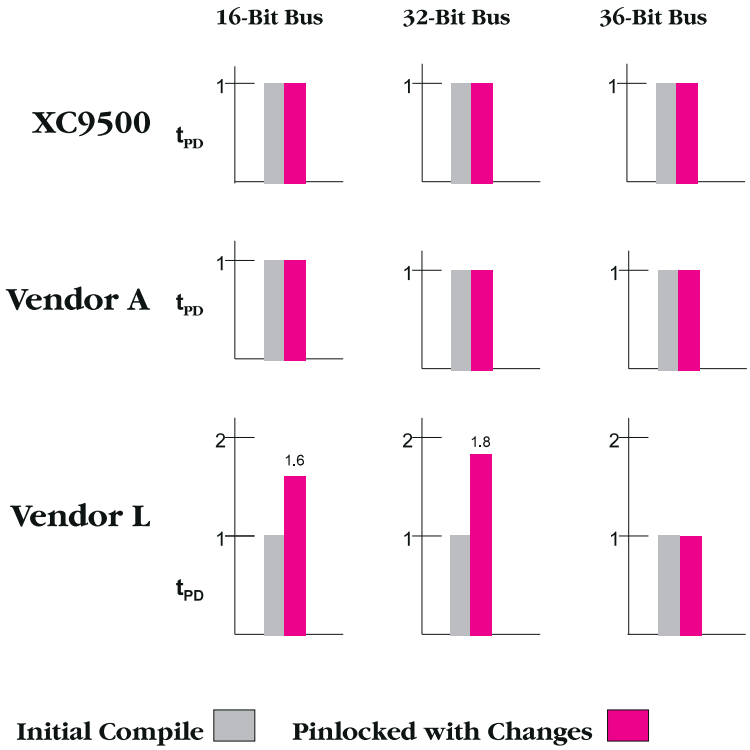

Figure 3: *Data Path-Normalized Benchmark Results*

XC9500 Benchmarks

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The benchmark results in **Figure 2** demonstrate that both the Xilinx XC9500 family and the Vendor A devices were able to accommodate the design changes without any impact on design performance. Vendor L devices maintained the same pinout, but with a significant (up to 60%) performance penalty. Since the Vendor L devices have 16 input logic blocks, the performance degradation of the 16-bit address decoder can be attributed to poor routing resources while the performance of the 32 and 36-bit decodes is degraded by both poor routing and narrow logic block fan-in.

Datapath Benchmark

This benchmark design measures the affect of routing resources on the CPLD's pin-locking capability. This design contains a single 16-, 32- or 36-bit wide data bus. A typical design change involves the reordering of data bits.

The benchmark results shown in **Figure 3** show that both the Xilinx XC9500 family and Vendor A devices were able to accommodate the design changes without any impact on design performance. Vendor L devices sacrificed performance (up to 80%) to reroute the design when pinlocked. Since only one logic block input was required for each output, this performance degradation can be attributed to poor routing resources, or fitter performance, or both, but cannot be attributed to logic block fan-in.

Address Counter Benchmark

This benchmark design contains two 16-, 24- or 32-bit loadable address counters loaded from separate buses but with common clock and hold signals. A typical design change alters the initial count load value. This benchmark measures the effect of routing resources and function block fan-in on the CPLDs pin-locking capability

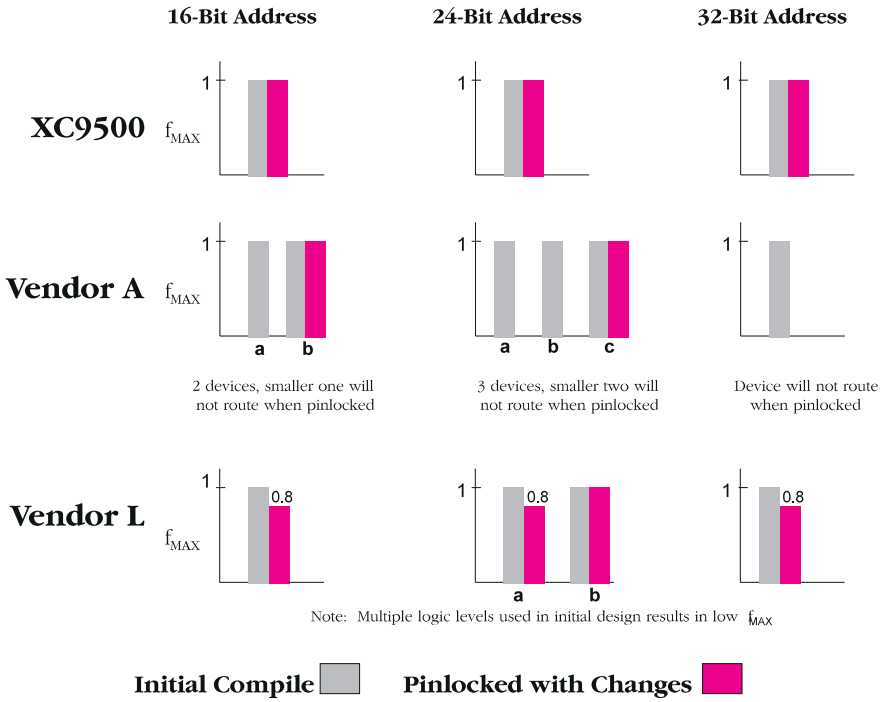

Figure 4: *Address Counter-Normalized Benchmark Results*

when macrocell feedbacks and other high fan-out signals are involved.

The benchmark results shown in **Figure 4** demonstrate the superiority of the XC9500 CPLD architecture. All XC9500 devices were able to accommodate the design changes without any impact on design performance. When Vendor A's routing resources were stressed, performance didn't just degrade, the devices completely failed to route. Vendor L devices used several layers of logic in the initial design, with correspondingly low f_{MAX}. This enabled the fitter to reroute the design using alternate routing paths, with less performance degradation (20%) than designs initially requiring only one logic level.

Conclusions

The benchmark results confirm the superior pin-locking performance of the Xilinx XC9500 family. This performance is consistent across all devices and package types. The wide function block fan-in enables pin-locking of wide, high-speed logic functions. Furthermore, because feedthroughs are not needed for routing, there is no performance degradation due to routing congestion. This timing consistency is as important as routing ability for maintaining pin-locked designs.

The XC9500 CPLD devices feature the industry's best pin-locking capability, eliminating the need for PCB modifications due to design changes. This feature not only shortens design cycles and decreases design costs but also facilitates the use of in-system programmability to upgrade or modify systems in the field. ◆

Using XC9500 Slew Rate Controls

Designers need options for managing the many signal switching conditions that occur in their systems. One simple but effective option is the output slew rate control provided in the XC9500 family CPLDs. This feature permits the simple selection between a slew-rate-limited output drive and a high-speed output drive. The result is easy, convenient control of switching characteristics on a pin-by-pin basis.

Currently, the default condition of the design software provides a slew-rate-limited configuration on all output pins. This is consistent with the default condition provided by the Xilinx FPGA development tools. To obtain faster switching speeds, the designer must configure the appropriate output buffers for the fast slew rate.

Since the slower slew rate is the default, reported timing for an implemented design may be slower than expected for a given speed grade. This is simply due to the fact that a slower slew rate output crosses the switching threshold at a later time than a faster slewing signal *(see **Figure 1**)*. The Xilinx timing report simply adds a small time delay to the output signal, accounting for the added delay.

A number of methods are available for specifying the fast slew rate, dependent on the design style chosen.

- For XABEL-CPLD, include one or more of the following directives:

  ```
  XEPLD Property 'FAST ON';
  ```
  Sets all pins to fast slew rate

  ```
  XEPLD Property 'FAST ON A B C';
  ```
  Pins A,B and C will be fast & all others remain slew rate limited

- For schematic entry, attach a FAST attribute to the appropriate output pad symbol.
- For Synopsys VHDL, use the following DC Shell commands to set all outputs for the fast slew rate:

  ```
  set_port_is_pad "*"
  set_pad_type -slewrate NONE all_outputs()
  insert_pads
  ```

  Alternatively, the fast slew rate can be specified for individual outputs by replacing the second line above with commands of the form:

  ```
  set_pad_type -slewrate NONE port_name
  ```

- For Metamor VHDL, add the Metamor library to your VHDL file with the commands:

  ```
  library metamor;
  use metamor.attributes.all
  ```

Then, after your signal declarations, assign the fast attribute to a signal with the command:

```
attribute property of port_name : signal is "Fast"
```

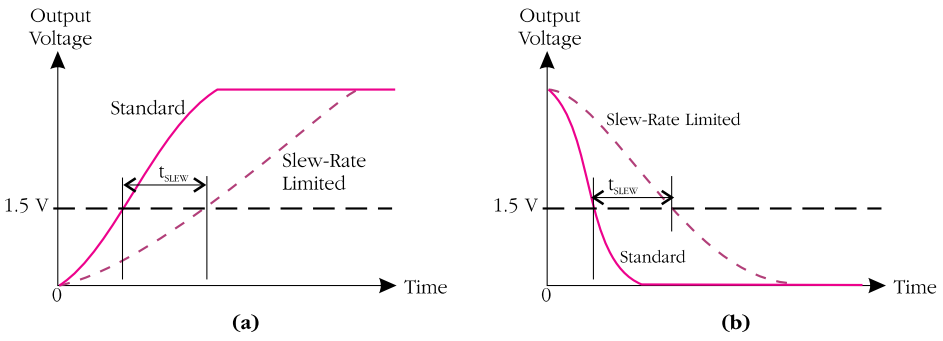

Figure 1: *Effect of slew rate control on output switching times*

Designing With XC5200 Carry Logic

Simple design makes XC5200 carry logic even more flexible than that of XC4000 Series

The XC5200 FPGA's carry logic is deceptively simple. While this architecture only provides a series of multiplexers interconnected by dedicated carry nets, the use of function generators to control these multiplexers makes the XC5200 FPGA's carry logic extremely flexible — more flexible, in fact, than the XC4000 carry logic with its multiplicity of modes.

In the XC5200 architecture, one bit of a simple adder uses two function generators and a carry chain multiplexer, as shown in **Figure 1**. However, not all of the function generator's capability is utilized in the basic adder. In the input function generator, the adder input, b_i, can be any function of the three inputs that are available. For example, one of these inputs could be used as an add/subtract control, inverting b_i in an XOR gate when necessary.

Similarly, the adder output can be combined in any way with the two remaining function generator inputs. In a typical counter application, these might be used for a multiplexer to load the counter or, alternatively, for an AND gate to provide a synchronous clear.

A more complex example uses this additional capability in a carry-select adder that trades additional logic for higher performance (**Figure 2**). The adder is divided into two sections. The lower half operates normally, but in the upper half two carry chains are used in parallel, one initialized with a '0' and the other with a '1.' The carry output of the lower half is used to select which carry chain is used to complete the sum. The carry propagates simultaneously in the upper and lower halves of the adder; thus, the settling time is reduced.

Since a single function generator can both select the carry and complete the sum, the incremental cost over the basic adder is only 25%. The direct access to the carry chain minimizes the timing overhead associated with this technique, which is effective even for relatively short adders.

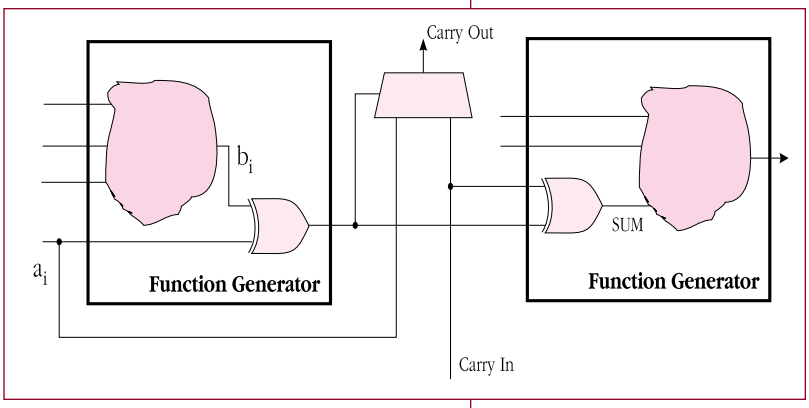

Figure 1:
XC5200 Carry Structure

The corresponding acceleration technique for long adders in the XC4000 architecture is the conditional-sum technique. In the upper half of a conditional-sum adder, two complete adders are implemented with '0' and '1' carry inputs, and

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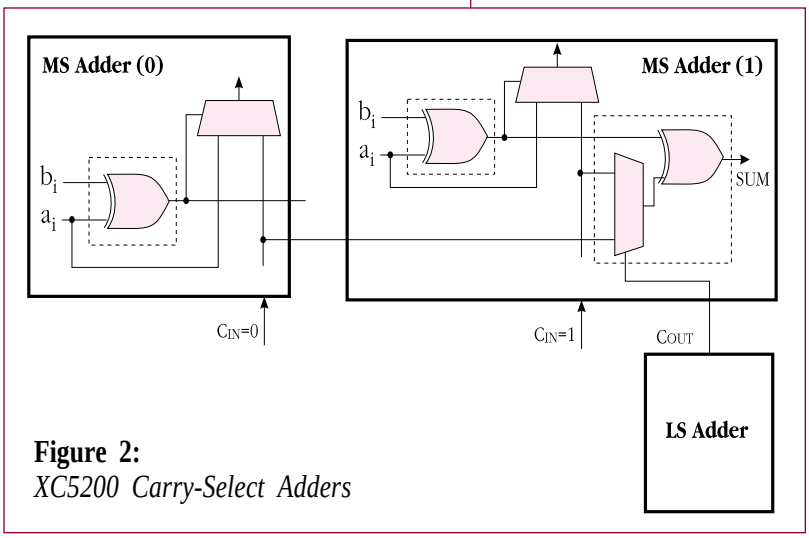

Figure 2:
XC5200 Carry-Select Adders

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additional CLBs are required to select between the outputs of these adders according to the carry output from the lower half. The technique is only effective for relatively long adders; the incremental cost is 100%.

It is interesting to note that, in the XC5200 architecture, the carry-select and conditional-sum techniques cannot always be distinguished. Both sums of the conditional-sum adder can be completed in the same function generator. This function generator can be further used to select between them. If this is done, all the function-generator truth tables and all the interconnections become identical to the carry-select adder. This should not be surprising, however, since both techniques implement the same uniquely defined adder function.

In a simple multiplier, the product is computed using a cascade of gated adders together with appropriate shifts (**Figure 3**). A more detailed view of a single bit slice through the first two adders of this multiplier is shown in **Figure 4**. One of the two AND gates that precedes the first adder is combined into the function generator that controls the carry multiplexer. The other AND gate, however, must use a separate function generator because there is a fan-out point at the second input to the adder.

In the second and subsequent adders, the AND gates again use separate function generators. This permits the XOR gates that complete the previous sums to be merged adder inputs, thus saving both logic resources and critical-path delay. If, instead, the AND gates had been merged into the

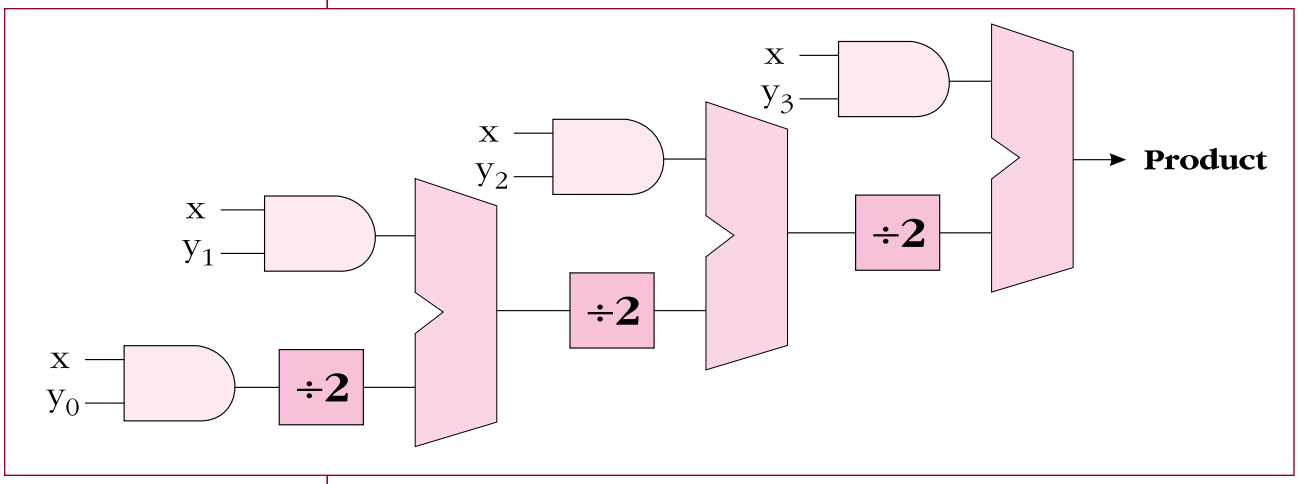


Figure 3:
4-Bit Cascade Multiplier

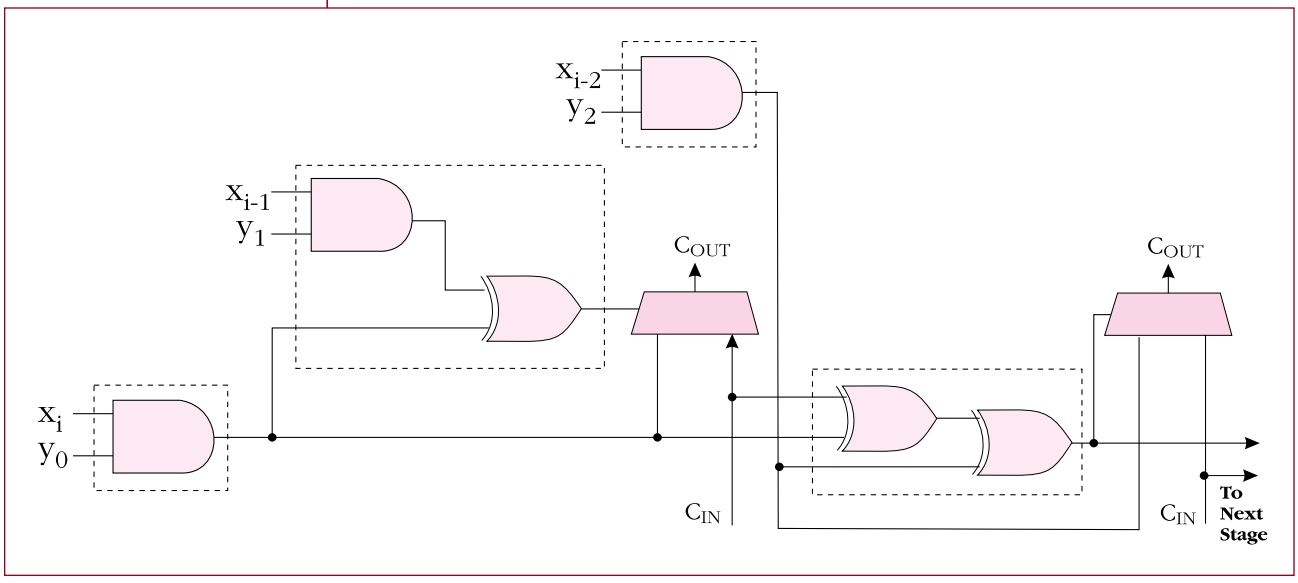
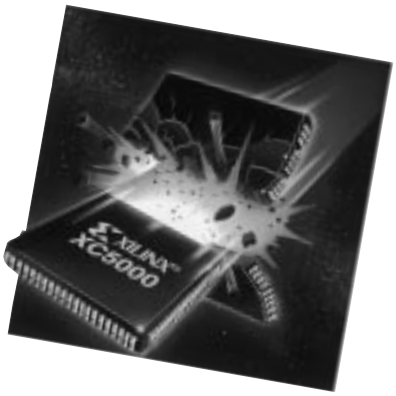


Figure 4:
Bit-Slice of First Two Adders



inputs, the XOR gates would have required function generators. In this case, the resource utilization would have been the same, but the delay longer. Only in the final adder is a separate function generator needed for the XOR gate.

The speed of the multiplier can be increased by rearranging the cascade of adders into a tree, as in **Figure 5**. After the first set of adders, the input of each adder can absorb the output XOR gate of one of the two preceding adders, as described in the cascade multiplier. The other preceding adder, however, must use a separate function generator for its XOR gate.

In the first set of adders, the objective is to multiply the X input by bit pairs of Y, creating products that are 0X, 1X, 2X or 3X. This is usually achieved by gating X and 2X into an adder, as is shown in Figure 5.

However, a different, more direct approach may be used in XC5200 FPGA.

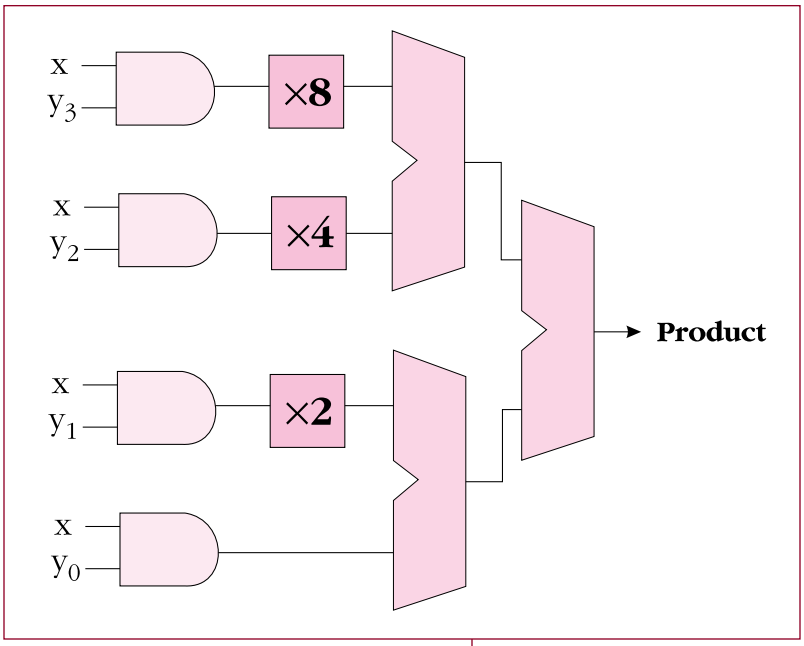
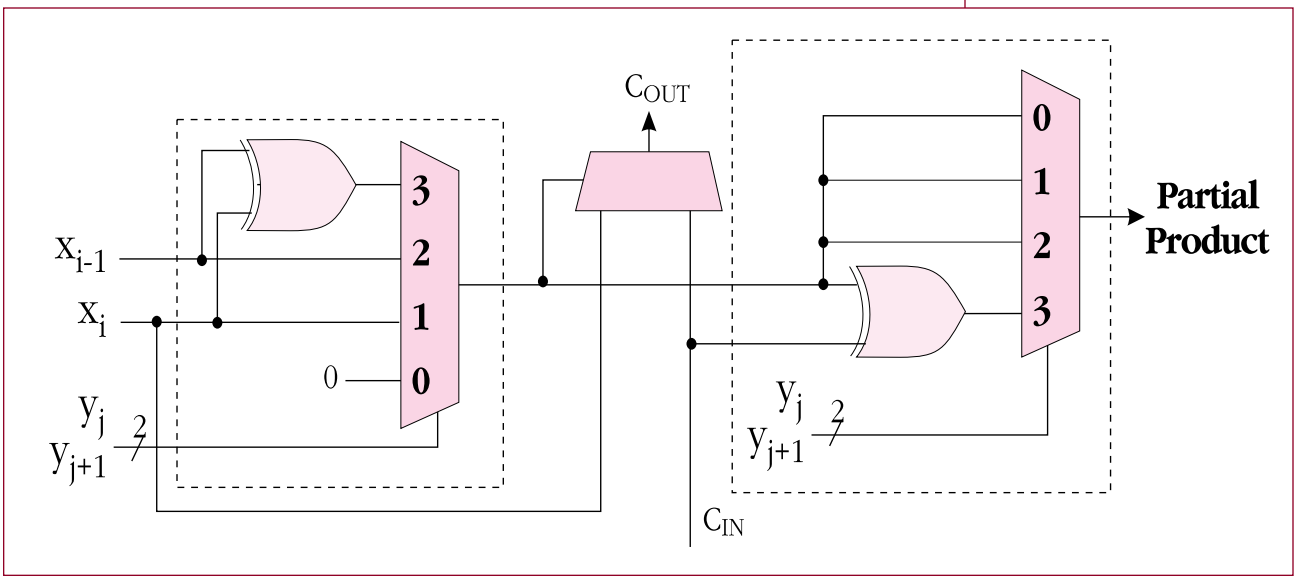


Figure 5:
Adder-Tree Multiplier

A bit slice of this more efficient approach is shown in **Figure 6**. The carry chain is only used to add X and 2X when the 3X output is required. Otherwise, 0, X or 2X is selected in the first function generator and routed to the second function generator where it passes through unaltered. While the carry chain continues to operate in a meaningless way, it cannot damage itself, and its outputs are not required. When 3X is required, the first function generator XORs X and 2X to control the carry chain in a normal addition. The sum is completed in the XOR gate that precedes the multiplexer in the second function generator. ◆

Figure 6:
First Stage of a Tree-Adder Multiplier



XC4000 Series Select-RAM Memory:

Advantages and Uses

The XC4000 Series of FPGA devices (i.e., the XC4000E and XC4000EX families, and their low-voltage counterparts, the XC4000L and XC4000XL families) includes several architectural improvements over the highly-successful XC4000 FPGA family. One of the most important new features is Select-RAM™ memory. Select-RAM memory can be defined as the capability of programming the look-up tables in Configurable Logic Blocks (CLBs) as ROM or as single- or dual-port RAM, with edge-triggered (synchronous) or level-sensitive (asynchronous) timing. Select-RAM memory also can be initialized to a known value in all RAM and ROM modes.

Select-RAM memory is unique in its range of options and ability to deliver high-speed dual-port memory. The advantages of the Select-RAM capability include flexibility, increased ease-of-use, shorter design cycles and increased performance.

Flexibility

Clearly, the options of edge-triggered or level-sensitive and single-port or dual-port RAM provide a wide selection of choices for the designer. The distributed nature of the RAM, which is implemented in individual CLBs, also contributes to the flexibility of Select-RAM memory. Only sufficient CLBs to implement a given memory block need be allocated as RAM: the memory block size can be scaled to exactly match the requirements of the application. Each RAM block can be placed close to related logic. There is no need to consume a large block of dedicated memory to implement a small RAM function, nor to route control and data lines across the device to reach such dedicated blocks. Each CLB can be individually configured, so the designer can "mix and match" RAM modes. Select-RAM is the most flexible memory implementation available in an FPGA today.

Ease of Use

Traditional RAM capability, now referred to as the level-sensitive or asynchronous option to Select-RAM memory, has never been simple to use. Meeting the required timing relationships often involved careful layout and detailed timing analysis. To guarantee correct behavior, a 2X clock is typically required, in order to generate the Write Enable during the third quadrant of the write clock cycle. This type of RAM is the only available option in the original XC4000 family devices.

None of these delicate timing relationships need be maintained when using one of the edge-triggered Select-RAM modes available in XC4000-Series devices. Instead, writing to a memory block is just like writing to a data register: set up the address and data, enable the RAM and apply the effective clock edge. A conceptual model for a Select-RAM block in edge-triggered mode is shown in the **Figure 1**.

The ability to initialize RAM, as well as ROM, as part of device configuration eliminates the need for logic to perform that initialization. Reduced logic results in smaller, simpler and more reliable designs.

All of the Select-RAM options are directly and easily implemented using any of the schematic entry, MemGen memory block generator tool, X-BLOX™ schematic-based synthesis, or HDL synthesis design environments. Detailed information on how to use these tools to implement Select-RAM is available in the new Xilinx application note "Using Select-RAM Memory in XC4000 Series FPGAs."

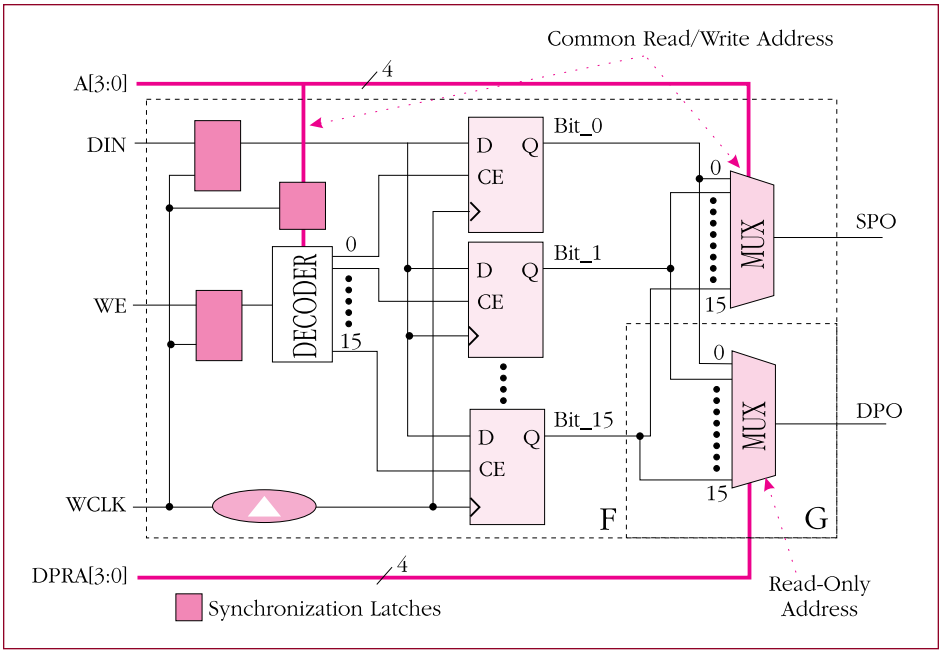


Figure 1: *XC4000 Series Conceptual Model for Edge-Triggered Memory*

Shorter Design Cycles

The ease-of-use associated with edge-triggered memory design results in shorter design cycles as compared to using level-sensitive RAM. The design, simulation and testing steps are all simplified.

Performance

As mentioned above, level-sensitive RAM designs may require both a 2X clock and significant signal manipulation to meet the stringent timing requirements on the Write Enable signal. The Address and Data inputs must be set-up at the RAM input pins by the time the Write Enable signal arrives, typically halfway through the write cycle.

When the same design is implemented using edge-triggered RAM, Address and Data may change in response to (for example) the rising edge of the input clock. The Write can occur on the next rising edge of the same clock. Therefore, the Address and Data have the full write cycle to set-up at the RAM input pins. The result is a memory block that operates at approximately twice the speed of the level-sensitive version of the design. When the simultaneous read/write capability of the dual-port Select-RAM option is taken into account, data throughput can be doubled again, resulting in a total four-fold increase in effective data rates. These results are demonstrated in a simple FIFO design in the Xilinx application note "Implementing FIFOs in XC4000 Series RAM."

Distributed RAM provides an additional speed advantage: locating RAM blocks closer to related logic minimizes routing delays on critical paths.

Uses of Select-RAM Memory

The edge-triggered RAM capability can and should be used in all new designs requiring RAM. These applications include register files, FIFO buffers, multipliers, shift registers and pseudo-random sequence generators.

The dual-port option adds the ability to read and write simultaneously from two different addresses. This ability considerably simplifies FIFO designs and is useful for constructing dual-port register files. ◆

The Application Notes referenced in this article are available on the Xilinx WebLINX web site at www.xilinx.com, or by contacting the Xilinx Technical Hotline.

Trading Off Among the Three Ps

Power, Package & Performance

There are well-defined relationships between chip power consumption, package thermal characteristics, ambient and junction temperature, and device performance.

In many cases, the user has no control over the maximum ambient temperature, but can choose the device and package, and then strive for an acceptable power consumption. In other cases, chip, package, power consumption and ambient temperature are given, and the resulting achievable performance level must be calculated. If performance cannot be sacrificed, thermal management techniques (e.g, airflow and heat sinks) can be used to lower the thermal resistance.

The governing equation is

$$T_J = T_A + P \times \Theta_{J\text{-}A}$$

where T_J = junction temperature

T_A = ambient temperature

$\Theta_{J\text{-}A}$ (Theta J-A) = Thermal resistance of the package-die combination

P = power dissipation

$\Theta_{J\text{-}A}$ is expressed in degrees C of junction temperature rise over the ambient temperature for every Watt dissipated in the device. $\Theta_{J\text{-}A}$ is primarily a function of the package and the airflow, with die size a secondary factor. (Larger die have a lower $\Theta_{J\text{-}A}$ value). *See Table 1.*

When the junction is hotter than 85°C, where Xilinx tests and guarantees performance parameters, delays increase 0.35% for every additional degree C. At 125°C, the maximum allowed junction temperature in a plastic package, delays are 14% longer, and speed is thus 12% lower than the guaranteed values in the data book and the software. In ceramic packages, the maximum allowed junction temperature is 150°C. ◆

Typical thermal resistance for various packages with and without airflow

Package	Still Air	250 ft/min (1.3 m/s)	500 ft/min (2.5 m/s)	750 ft/min (3.8 m/s)	
HQ304	11	7	6	5	°C/W
HQ240	12	9	7	6	°C/W
HQ208	14	10	8	7	°C/W
MQ240	17	12	11	10	°C/W
MQ208	18	14	13	12	°C/W
PQ240	23	17	15	14	°C/W
PQ208	32	23	21	19	°C/W
PQ160	32	24	21	20	°C/W
PQ100	33	29	28	27	°C/W
PC84	33	25	21	17	°C/W
TQ100	31	26	24	23	°C/W
VQ100	38	32	30	29	°C/W

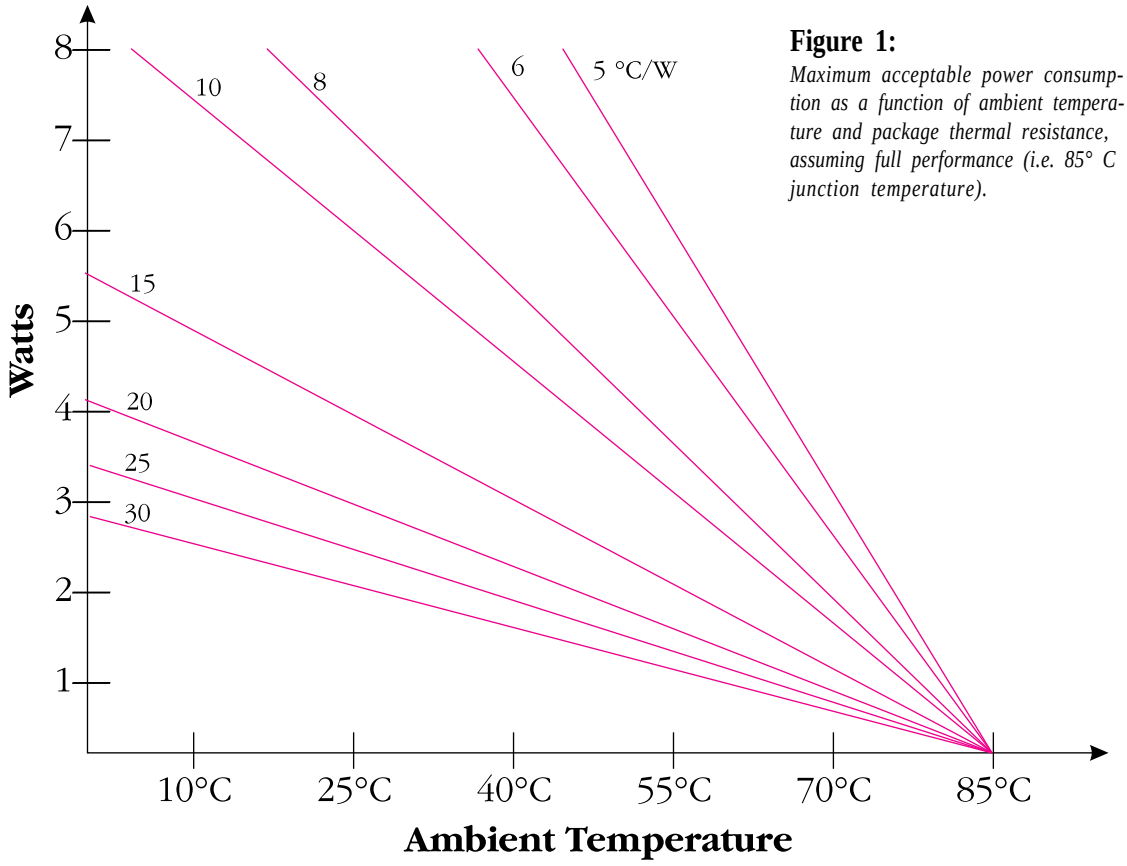


Figure 1:
Maximum acceptable power consumption as a function of ambient temperature and package thermal resistance, assuming full performance (i.e. 85° C junction temperature).

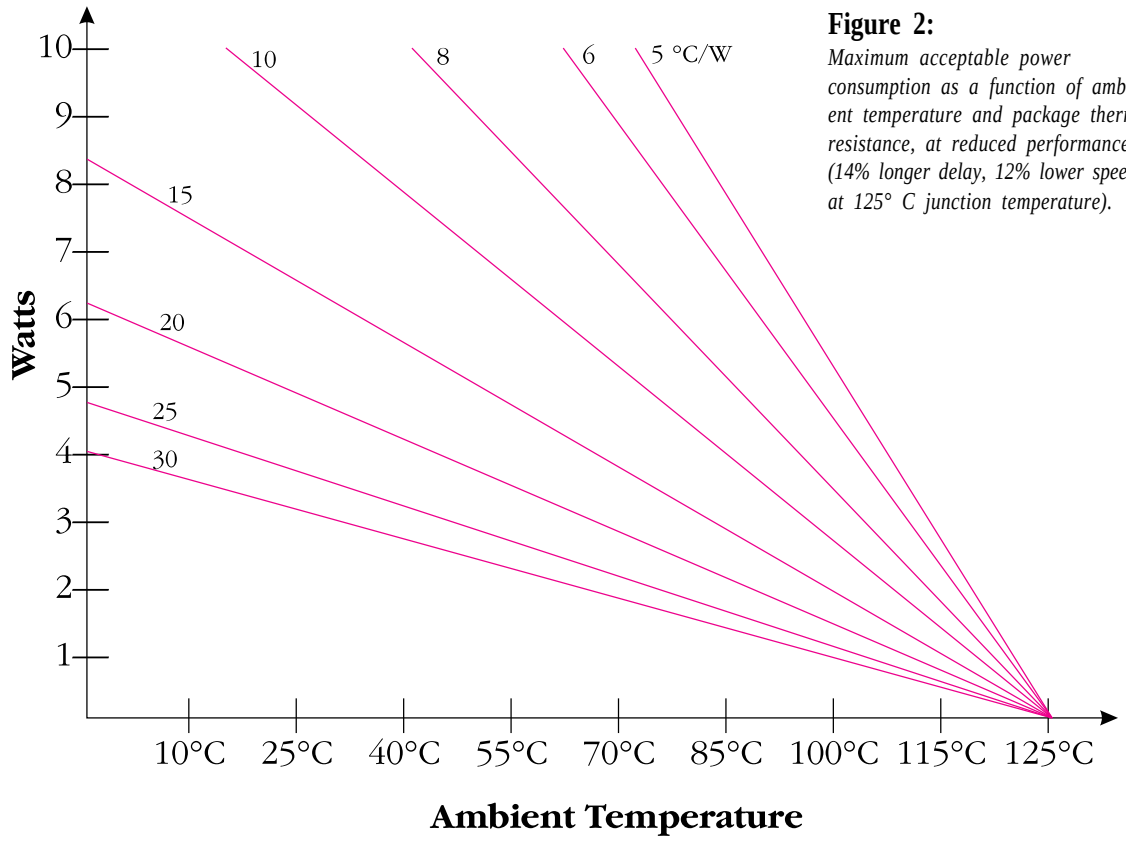


Figure 2:
Maximum acceptable power consumption as a function of ambient temperature and package thermal resistance, at reduced performance (14% longer delay, 12% lower speed at 125° C junction temperature).

Metastability Recovery in Xilinx FPGAs

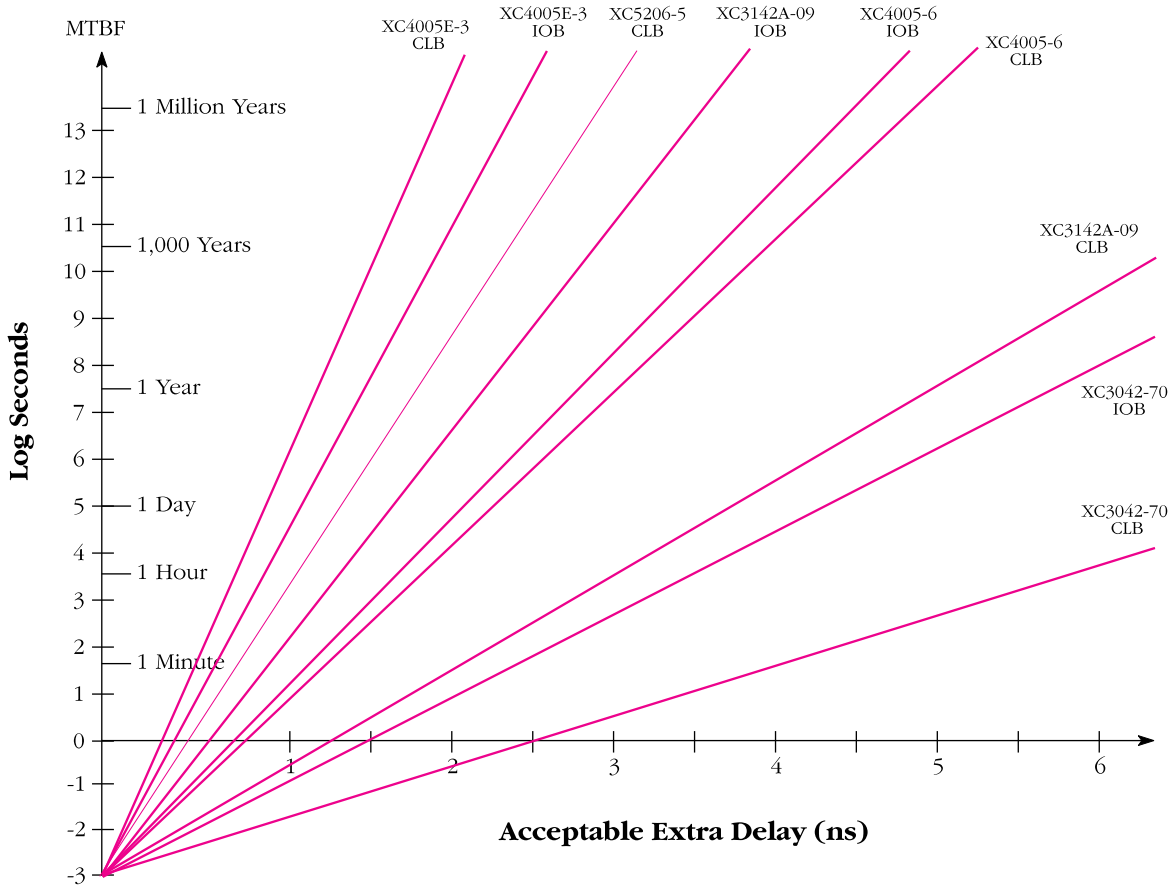
Whenever a clocked flip-flop synchronizes an asynchronous input, there is a small probability that the flip-flop output will exhibit an unpredictable delay. This happens when the input transition not only violates the setup and hold-time specifications, but actually occurs within the tiny timing window where the flip-flop accepts the new input. Under these circumstances, the flip-flop can enter a symmetrically-balanced transitory state, called a metastable state.

While the slightest deviation from perfect balance will cause the output to revert to one of its two stable states, the delay in doing so depends not only on the gain-bandwidth product of the circuit, but also on how perfect the balance was and on the noise level within the circuit; the delay can, therefore, only be described in statistical terms. The problem for the system designer is not the illegal logic level in the balanced state (it's easy enough to translate that arbitrarily to either a 0 or a 1), but the unpredictable timing of the final change to a valid logic state. If the metastable flip-flop drives two destinations with differing path delays, one destination might clock in the final data state while the other does not.

Metastability Measurements

Recently, the metastable delays of four different Xilinx FPGA devices were measured: two cutting-edge devices using 0.5 micron, 3-layer-metal technology, the

Figure: *Mean Time Between Failure for various IOB and CLB flip-flop outputs when synchronizing a 1 MHz asynchronous input with a 10 MHz clock.*



XC4005E-3 and the XC3142A-09; and, for comparison purposes, two older-technology devices, the XC4005-6 and the XC3042-70. In each device, two different implementations test the IOB and CLB flip-flops. The XC5200-5 CLB flip-flop was also tested. (There is no IOB flip-flop in XC5200 architecture.)

The XC4000E amd XC4000 devices showed little difference between IOB and CLB behavior, but in the XC3000-series devices, the IOB flip-flops showed dramatically better metastable performance than the CLB flip-flops. This difference can be traced to subtle differences in circuit design and layout and will guide us to further improvements in metastable performance of future designs.

Metastable measurement results are listed in the table and plotted in the figure. The results for XC4000E-3 IOB and CLB flip-flops, XC5200-5 CLB flip-flops and XC3100A-09 IOB flip-flops are outstanding, far superior to most metastability data published anywhere else. When granted 2 or 3 ns of extra settling delay, these devices come close to eliminating the problems caused by metastability, since their mean-time-between-failure exceeds millions of years. The older-technology devices are slightly less impressive, but still show very acceptable performance, especially the IOB input flip-flops that are normally used to synchronize asynchronous input signals.

Metastability Calculations

The Mean Time Between Failures (MTBF) can only be defined statistically. It is inversely proportional to the product of the two frequencies involved, the clock frequency and the average frequency of the asynchronous data changes, provided that these two frequencies are independent and have no correlation. The generally accepted equation for MTBF is

$$\mathbf{MTBF} = \frac{e^{K2 \times t}}{F1 \times F2 \times K1}$$

K2 is an exponent that describes the speed with which the metastable condition is being resolved.

K1 represents the metastability-catching setup time window that describes the likelihood of going metastable

F1 is the frequency of the asynchronous data input

F2 is the flip-flop clock frequency

t is the settling time

K2 is an indication of the gain-bandwidth product in the feedback path of the master latch in the flip-flop. A small decrease in the time constant 1/K2 results in an enormous improvement in MTBF.

With F1 = 1 MHz, F2 = 10 MHz and K1 = 0.1 ns,

$$\mathbf{MTBF\ (in\ seconds)} = 10^{-3} \times e^{K2 \times t}$$

The values of K2 under these conditions — expressed as 1/K2 in the table — were experimentally derived *(as described in the "1996 Programmable Logic Data Book," page 14-41).*

The MTBF under other operating conditions can be estimated using the data in the diagram. Simply divide the appropriate MTBF from the diagram by the product of the two relative frequencies. For example, for a 10 MHz asynchronous input synchronized by a 40 MHz clock, the MTBF is 40 times shorter than plotted, and for a 50 KHz signal and a 1 MHz clock, the MTBF is 200 times longer than plotted here. ◆

Metastability Measurement Results

Tested Flip-Flop		Value of 1/K2 in picoseconds
XC4005E-3	CLB	52
	IOB	62
XC4005-6	CLB	127
	IOB	118
XC3142A-09	CLB	208
	IOB	79
XC3042-70	CLB	385
	IOB	238
XC5200-5	CLB	73

XACT*step* and Alternate Operating Systems

The Xilinx XACT*step*™ development system software is available for both workstation and PC platforms. The PC-based version is designed for Windows 3.1, and the Sun-based version for the Sun OS. However, with some exceptions as detailed below, XACT*step* software can run on some variants of these popular operating systems.

Running XACT*step* v6.0.1 in Windows 95

The majority of the XACT*step* 6.0.1 software will run in Windows 95. However, there are some known compatibility issues:

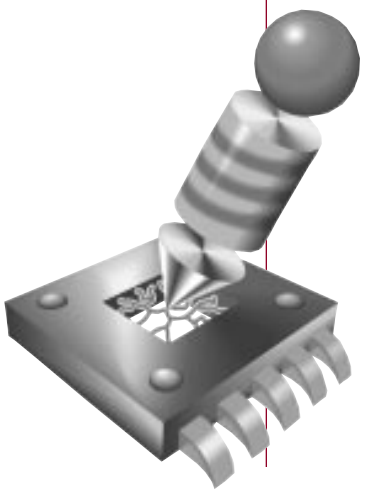
- The Design Manager will cause a General Protection fault when it is closed. This causes no system problems and can be ignored.
- The Hardware Debugger does not run. There is no known workaround.
- The ProSeries software does not run under Windows 95. WorkView Office is available on an as-needed basis. Contact the Xilinx Technical Hotline for more information.

Running XACT*step* v5.2.1 in Windows NT

The XACT*step* v6.0.1 GUI tools (DM, Floorplanner, Prom File Formatter, Hardware Debugger) will not run in Windows NT, but the v5.2.1 executables can be made to run in a DOS box with the addition of **RAINPORT.EXE**, available in the SWHLP\XACTFPGA directory of the Bulletin Board Service (BBS). This program fixes parallel port access problems that occur when the security key is checked.

Solaris Support for XACT*step* v5.2.1

Although not officially supported and tested by Xilinx, most of the XACT*step* tools work with Solaris 2.5. The XChecker program, which did not work with Solaris version 2.4, will run under 2.5 when the SunOS 4.1.3 backwards-compatibility option is used. However, the Install program still does not work in Solaris. As a workaround to the Install problem, a script called **cdi.csh** has been developed that will install the software in a non-graphical mode. This script can be found on the Xilinx BBS (408-559-9327) and on the Xilinx FPT site (xilinx.com). Unfortunately, the Xilinx-Mentor Graphics interface (DS-344) does not work under Solaris, so Mentor Graphics' users should stay with SunOS 4.1.X. ◆



New, Independent E-Mail User Group Dedicated to Xilinx Technology

XUMA: Xilinx User MAiling list

Alain Arnaud of ECLA, Inc. (Newton, Massachusetts), a design consultant and experienced FPGA and ASIC designer, was pondering how to best field his customers' questions — a mix that included both system-level and FPGA-level issues. To assist in this task, Alain started an e-mail address list of colleagues and industry contacts. This effort has grown into XUMA — the Xilinx User MAiling List — a new, independent forum for the communication of technical subjects across the Xilinx user community. XUMA, initiated in May,1996, currently has over 250 subscribers and is growing rapidly.

XUMA mailings are e-mails of technical questions and answers sent to Alain by anybody and forwarded to everyone on the XUMA mailing list.

Xilinx users can subscribe to the list, unsubscribe from the list or submit a change of address by sending mail to:

```
xuma-request@ecla.com
```

To send a technical question, answer or related information to the list, mail it to:

```
xuma@ecla.com
```

Mention in your mail if you would like to remain anonymous. Alain sends out digests of messages sent to him about twice each week.

XUMA is more focused than the "comp.arch.fpga" news group *(see XCell #21, page 41)*. Comp.arch.fpga is a general FPGA forum that typically deals with broad-based questions and issues, while XUMA is dedicated to trading technical information regarding Xilinx devices and software. As a result, it takes less time to review XUMA digests for pertinent information. Furthermore, Alain is actively designing with a range of Xilinx parts and is up-to-date on Xilinx products.

XUMA is completely independent from Xilinx, Inc. Many engineers want an independent technical forum for openly discuss key concerns and issues, both at the system- and device-level, and get objective answers from others in their professional community. ◆

Remember, Xilinx users can contact the Xilinx Technical Support Hotline *(see page 35)* with technical questions on Xilinx products.

TO:	xuma-request@ecla.com
CC:	
TOPIC:	Xilinx mailing list
MESSAGE:	Alain -- please add my name to the XUMA list for Xilinx technical issues.

TO:	xuma@ecla.com
CC:	
TOPIC:	XC4000 Series tip
MESSAGE:	Alain -- I think I have discovered a way to use an XC4025E as a barrier to protect my desk from the harmful effects of excess moisture building up on the bottom of my coffee mug.

New Technical Support Choices

Callers to the Technical Support Hotline at the Xilinx headquarters in San Jose now encounter a friendly, ease-to-use telecommunications system that allows better access to the resources and solutions needed to ensure design progress and success.

Efficient and Speedy Access to Engineers on the Hotline Through Increased *Choices*

We are continuously investing in state-of-the-art customer support systems to provide customers with choices, efficient access to support resources and reliable connections.

When contacting the Technical and Applications Support Hotline in San Jose, you will be prompted to input the purpose of your inquiry to ensure that you reach the most appropriate person as soon as possible. In addition, you will be asked to provide your *"personal ID number"* or your *"case ID number."*

Anytime during the process, you can bypass the automated inquiries to speak directly with a live support representative or leave a voicemail message for a support engineer.

PHOTO FOR ILLUSTRATION PURPOSES ONLY

What is my personal ID number?

The first time you contact the Xilinx hotline, your *personal ID number* will be assigned by our customer case management system. On subsequent calls, you may use this number to speed up the support process. Once the telecommunications system receives your ID number, you will skip directly to a menu of topics to choose from so that your call can be routed to the most helpful resource or qualified support engineer available.

Cases opened under your ID number are tracked under your name. If your colleagues wish to contact Xilinx, advise them that they can receive their own *personal ID numbers* by calling the hotline directly.

What is my case ID number?

Each time you call with a new support need, a *case ID number* will be assigned and communicated to you by a support professional. If you have further need to contact the hotline regarding an open case, you can speed your access to your case worker by inputting the case number directly into the telecommunications system.

What is the fastest way to reach an engineer with a new question?

On a typical day, the fastest path to reach a support engineer is through the telecommunications system using your personal ID number:

- Select your situation: New Case or Existing Open Case.
- Enter your *Personal ID* or the *Open Case ID*
- For a new case, you will be prompted to select a product topic area.
- Your call is directed to the most appropriate available resource.

Increased On-Line Technical Information

The Xilinx BBS mirrored on the World Wide Web.

Xilinx Bulletin Board Service files and resources can now be accessed through the Xilinx Internet FTP site.

Xilinx offers increased on-line support resources and choices.

In the coming months, keep an eye on the Xilinx Technical Support resources on WebLINX, the Xilinx web site (www.xilinx.com). In addition to the above mentioned BBS resources, you will see increased access to applications materials, product support materials, and commonly asked questions and solutions.

TECHNICAL SUPPORT RESOURCES

HOTLINE SUPPORT, U.S.

Customer Support Hotline:
800-255-7778
Hrs: 8:00 a.m.-5:00 p.m. Pacific time

Customer Support Fax Number:
408-879-4442
Avail: 24 hrs/day-7 days/week

E-mail Address:
hotline@xilinx.com

Customer Service*:
408-559-7778, ask for customer service
** Call for software updates, authorization codes, documentation updates, etc.*

HOTLINE SUPPORT, EUROPE

UK, London Office
telephone: (44) 1932 820821
fax: (44) 1932 828522
Bulletin Board Service: (44) 1932 333540
e-mail: ukhelp@xilinx.com

France, Paris Office
telephone: (33) 1 3463 0100
fax: (33) 1 3463 0959
e-mail: frhelp@xilinx.com

Germany, Munich Office
telephone: (49) 89 991 54930
fax: (49) 89 904 4748
e-mail: dlhelp@xilinx.com

Japan, Tokyo Office
telephone: (81) 3 3297 9163
fax: (81) 3 3297 0067
e-mail: jhotline@xilinx.com

X-TALK: The Xilinx Network of Electronic Services

- **Xilinx home page on the World Wide Web** ..... www.xilinx.com.
- **Electronic Technical Bulletin Board (U.S.)** 408-559-9327
- **XDOCS E-mail document server-**
  send an E-mail to xdocs@xilinx.com with 'help' as the only item in the subject header. You will automatically receive full instructions via E-mail.
- **XFACTS fax document server** ..... available by calling 408-879-4400.

E-mail addresses for questions related to specific applications:

Digital Signal Processing applications ..... dsp@xilinx.com
PCI-bus applications ..... pci@xilinx.com
Plug and Play ISA applications ..... PnP@xilinx.com
PCMCIA card applications ..... pcmcia@xilinx.com
Asynchronous Transfer Mode applications ..... atm@xilinx.com
Reconfigurable Computing applications ..... reconfig@xilinx.com

Mentor Graphics

Q While compiling my Autologic design through Timsim8, PLD_DVE_BA returns the following warning, that may repeat several times:

```
# WARNING: Unknown design
  object: /JE/I1101S$37$5
```

What does this mean and how can I fix it?

Autologic may write out percent signs (%) in its instance names. Although this is legal in Mentor schematics, it is *not* legal in Xilinx netlists. To remedy this, EDIF2XNF changes each "%" in a netlist to "37" (so used because 37 is the ASCII code for the percent sign). Unfortunately, the Mentor back-annotation file is written with this change, so that I1101S$37$5 in the MBA file does not match up with the true I1101S%5 in the schematic.

The problem may be fixed by modifying the mbapp.nawk script, which processes the MBA file for use in PLD_DVE_BA, to change the 37's back to %'s. For more information, send E-mail to **xdocs@xilinx.com** with **send 618** in the subject line. Once this modification is made, Timsim8 should run smoothly.

Q I have an Autologic design that, during Men2XNF8, gives me the following error in EDIF2XNF:

```
Error: 5 No direction/pintype
  for port:PINBALL/WIZARD
```

What's happening and how can I fix this?

The pin in question does not have a PINTYPE property associated with it. The PINTYPE property indicates a pin's directionality, and is required in XACT 5.*x* by EDIF2XNF and XNFMerge. Autologic may omit PINTYPE properties when synthesizing hierarchical symbols, following the rules of pre-XACT 5.0 software.

If the offending symbol was created by Autologic II, a patch is available on Mentor Graphics' FTP site at supportnet.mentorg.com (137.202.128.4).

Autologic II version A.*x* requires Patch 244, located in the directory:

```
/pub/patches/release_A/
  autologic2
```

with the filenames:

```
README_P244
  (patch information)
INSTALL_P244
  (installation instructions)
sg_p244.sss.tar.Z
  (SunOS 4.x)
sg_p244.ss5.tar.Z
  (Solaris 2.x)
sg_p244.hpu.tar.Z
  (HP-UX)
```

Autologic II version B.*x* requires Patch 320, located in the directory:

```
/pub/patches/release_B/
  autologic2
```

with the filenames:

```
README_P320
  (patch information)
INSTALL_P320
  (installation instructions)
sg_p320.sss.tar.Z
  (SunOS 4.x)
sg_p320.ss5.tar.Z
  (Solaris 2.x)
sg_p320.hpu.tar.Z
  (HP-UX)
```

Q After running Fncsim -o (use original schematic) on a design that contains X-BLOX components, I see no-connect symbols on certain pins in the simulation schematic. What's happening?

These no-connects will appear in the simulation schematic any place where two pin vertices are laying on top of each other. In the original schematic, the pins would be connected by a zero-length net. In the simulation schematic, however, the coincident pins will *not* be connected (hence, the no-connect symbol).

The best fix for this problem is to go back to the original schematic and move any coincident vertices apart, so that the net between them may be seen.

Synopsys

Q How can I prevent FPGA Compiler from writing my timing constraints into the .sxnf file?

During its optimization process, Synopsys' FPGA Compiler attempts to meet the timing constraints issued by you; and subsequently writes out the timing constraints into the netlist (.sxnf) file for the Xilinx tools to use. You may want to issue these constraints to the Xilinx tools in a separate constraints file, where you have the ablility to be more specific about particular paths that you want to constrain.

To do this, issue the following command just prior to writing out the .sxnf file:

```
xnfout_constraints_per_
 endpoint = 0
```

This will result in a netlist (.sxnf) that does not contain any timing constraints. You may then issue XACT Performance constraints in a .cst which will be used by the Xilinx tools. For more information on XACT Performance, see the Development Systems Reference Guide. ◆

COMPONENT AVAILABILITY CHART

PINS	TYPE	CODE	XC3020A	XC3030A	XC3042A	XC3064A	XC3090A	XC3020L	XC3030L	XC3042L	XC3064L	XC3090L	XC3142L	XC3190L	XC3120A	XC3130A	XC3142A	XC3164A	XC3190A	XC3195A	XC4003E	XC4005E	XC4006E	XC4008E	XC4010E	XC4013E	XC4020E	XC4025E	XC4028EX	XC4036EX	XC4044EX	XC4052XL	XC4062XL
44	PLASTIC LCC	PC44		◆												◆																	
	PLASTIC QFP	PQ44																															
	PLASTIC VQFP	VQ44																															
	CERAMIC LCC	WC44																															
48	PLASTIC DIP	PD48																															
64	PLASTIC VQFP	VQ64		◆					◆							◆																	
68	PLASTIC LCC	PC68	◆	◆											◆	◆																	
	CERAMIC LCC	WC68																															
	CERAMIC PGA	PG68																															
84	PLASTIC LCC	PC84	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆								
	CERAMIC LCC	WC84																															
	CERAMIC PGA	PG84	◆	◆	◆										◆	◆	◆																
100	CERAMIC QFP	CQ100																															
	PLASTIC PQFP	PQ100	◆	◆	◆										◆	◆	◆				◆	◆											
	PLASTICTQFP	TQ100														◆	◆																
	PLASTIC VQFP	VQ100		◆	◆				◆	◆			◆			◆	◆				◆												
	TOP BRZ. CQFP	CB100	◆		◆										◆	◆																	
120	CERAMIC PGA	PG120																			◆												
132	PLASTIC PGA	PP132			◆	◆											◆	◆															
	CERAMIC PGA	PG132			◆	◆											◆	◆															
144	PLASTICTQFP	TQ144			◆	◆	◆			◆	◆	◆	◆	◆			◆	◆				◆	◆										
	CERAMIC PGA	PG144																															
156	CERAMIC PGA	PG156																				◆	◆										
160	PLASTIC PQFP	PQ160				◆	◆											◆	◆	◆		◆	◆	◆	◆	◆							
164	CERAMIC QFP	CQ164																															
	TOP BRZ. CQFP	CB164					◆												◆	◆													
175	PLASTIC PGA	PP175					◆												◆	◆													
	CERAMIC PGA	PG175					◆												◆	◆													
176	PLASTICTQFP	TQ176					◆					◆		◆					◆														
184	CERAMIC PGA	PG184																															
191	CERAMIC PGA	PG191																						◆	◆								
196	TOP BRZ. CQFP	CB196																															
208	PLASTIC PQFP	PQ208					◆												◆	◆		◆	◆	◆	◆	◆							
	METAL MQFP	MQ208																															
	HI-PERF QFP	HQ208																								◆	◆		◆				
223	CERAMIC PGA	PG223																		◆						◆	◆	◆					
225	PLASTIC BGA	BG225																							◆	◆							
	WINDOWED BGA	WB225																															
228	TOP BRZ. CQFP	CB228																															
240	PLASTIC PQFP	PQ240																								◆							
	METAL MQFP	MQ240																															
	HI-PERF QFP	HQ240																								◆	◆	◆	◆				
299	CERAMIC PGA	PG299																										◆	◆				
304	HI-PERF QFP	HQ304																										◆	◆	◆			
352	PLASTIC BGA	BG352																											◆				
411	CERAMIC PGA	PG411																												◆	◆	◆	
432	PLASTIC BGA	BG432																												◆	◆	◆	
499	CERAMIC PGA	PG499																															◆
596	PLASTIC BGA	BG596																														◆	◆

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PINS	TYPE	CODE	XC4005L	XC4010L	XC4013L	XC5202	XC5204	XC5206	XC5210	XC5215	XC7236A	XC7272A	XC7318	XC7336	XC7336Q	XC7354	XC7372	XC73108	XC73144	XC9536	XC95108	XC95216
44	PLASTIC LCC	PC44									◆		◆	◆	◆	◆				◆		
	PLASTIC QFP	PQ44											◆	◆	◆							
	PLASTIC VQFP	VQ44													◆					◆		
	CERAMIC LCC	WC44									◆			◆	◆	◆						
48	PLASTIC DIP	PD48																				
64	PLASTIC VQFP	VQ64																				
68	PLASTIC LCC	PC68										◆				◆	◆					
	CERAMIC LCC	WC68										◆				◆	◆					
	CERAMIC PGA	PG68																				
84	PLASTIC LCC	PC84	◆	◆		◆	◆	◆	◆			◆					◆	◆			◆	
	CERAMIC LCC	WC84										◆					◆	◆				
	CERAMIC PGA	PG84										◆										
100	CERAMIC QFP	CQ100																				
	PLASTIC PQFP	PQ100				◆	◆	◆									◆	◆			◆	
	PLASTIC TQFP	TQ100																			◆	
	PLASTIC VQFP	VQ100				◆	◆	◆														
	TOP BRZ. CQFP	CB100																				
120	CERAMIC PGA	PG120																				
132	PLASTIC PGA	PP132																				
	CERAMIC PGA	PG132																				
144	PLASTIC TQFP	TQ144				◆	◆	◆	◆													
	CERAMIC PGA	PG144																◆				
156	CERAMIC PGA	PG156				◆	◆															
160	PLASTIC PQFP	PQ160					◆	◆	◆	◆								◆	◆		◆	◆
164	CERAMIC QFP	CQ164																				
	TOP BRZ. CQFP	CB164																				
175	PLASTIC PGA	PP175																				
	CERAMIC PGA	PG175																				
176	PLASTIC TQFP	TQ176		◆				◆	◆													
184	CERAMIC PGA	PG184																				
191	CERAMIC PGA	PG191						◆														
196	TOP BRZ. CQFP	CB196																				
208	PLASTIC PQFP	PQ208	◆	◆	◆			◆	◆													
	METAL MQFP	MQ208																				
	HI-PERF QFP	HQ208								◆												◆
223	CERAMIC PGA	PG223							◆													
225	PLASTIC BGA	BG225			◆				◆	◆								◆	◆			
	WINDOWED BGA	WB225																				
228	TOP BRZ. CQFP	CB228																				
240	PLASTIC PQFP	PQ240			◆				◆													
	METAL MQFP	MQ240																				
	HI-PERF QFP	HQ240								◆												
299	CERAMIC PGA	PG299								◆												
304	HI-PERF QFP	HQ304								◆												
352	PLASTIC BGA	BG352								◆												
411	CERAMIC PGA	PG411																				
432	PLASTIC BGA	BG432																				
499	CERAMIC PGA	PG499																				
596	PLASTIC BGA	BG596																				

Please note that the XC8100 family has been discontinued.

See page 13.

◆ = Product currently shipping or planned
❖ = New since last issue of XCELL (none appear in this issue)

XILINX RELEASED SOFTWARE STATUS-AUGUST 1996

XILINX INDIVIDUAL PRODUCTS

Key	Product Category	Product Description	Product Function	Xilinx Part Reference Number	Current Version by Platform PC1 6.2	SN2 4.1.x	HP7 9.01	Last Updt Comp	Previous Version Release	Notes/ Features
	COREXEPLD	XC7K Support	Core Implementation	DS-550-xxx	6.01	5.2.1	5.2.1	7/96	5.2/6.0	PC update by request only
	XABEL-CPLD	XC7K, XC9500 Support	Entry/Simulation/Core	DS-571-PC1	6.11			7/96	6.10	New version w/XC9500; First ship 4/29/96
	XACT-CPLD	XC7K, XC9500 Support	Core + Interface	DS-560-xxx	6.0.1	6.0.1	6.0.1	7/96	6.0	
	Mentor	8.4=A.4	Interface and Libraries	DS-344-xxx		5.2.1	5.2.1	7/96	5.20	
	OrCAD		Interface and Libraries	DS-35-PC1	6.0.1			7/96	6.0	Support for SDT+, VST+ v1.2
	Synopsys		Interface and Libraries	DS-401-xxx		5.2.1	5.2.1	7/96	5.20	Includes XC5200 X-BLOX Support
	Viewlogic	PROcapture	Interface and Libraries	DS-390-PC1	6.0.1			7/96	5.2/6.0	Includes PRO Series 6.1
	Viewlogic	PROsim	Interface and Libraries	DS-290-PC1	6.0.1			7/96	6.0	Includes PRO Series 6.1
	Viewlogic		Interface and Libraries	DS-391-xxx	6.0.1	5.2.1	5.2.1	7/96	6.0	
	XABEL		Entry,Simulation,Lib, Optimizer	DS-371-xxx	6.0.1	5.2.1	5.2.1	7/96	5.2/6.0	Now available on HP7
	XBLOX		Module Generator & Optimizer	DS-380-xxx	6.0.1	5.2.1	5.2.1	7/96	5.2/6.0	
E	Verilog	2K,3K,4K,7K Libraries	Models & XNF Translator	ES-VERILOG-xxx		1.00	1.00	na	na	Sun and HP

XILINX PACKAGES

Key	Product Category	Silicon Support 2K	3K	4K	5K	7K	9K	Xilinx Part Reference Number	PC1 6.2	SN2 4.1.x	HP7 9.01	Last Updt Comp	Previous Version Release	Notes/ Features
	Cadence	X	X	X	X	X	X	DS-CDN-STD-xxx		5.2.1	5.2.1	7/96	5.20	
	Mentor	X	X	X	X	X	X	DS-MN8-STD-xxx		5.2.1	5.2.1	7/96	5.20	
	Mentor	X	X	X	X	X	X	DS-MN8-ADV-xxx		7.00	7.00	na	na	
U	OrCAD	X	X	X	X	X	X	DS-OR-BAS-PC1	6.0.1			7/96	6.0	Customer w/v6.0 will receive v6.0.1 update
	OrCAD	X	X	X	X	X	X	DS-OR-STD-PC1	6.0.1			7/96	6.0	
	Synopsys		X	X	X	X	X	DS-SY-STD-xxx		5.2.1	5.2.1	7/96	5.20	Includes DS-401 v5.2
	Synopsys		X	X	X	X	X	DS-SY-ADV-xxx		7.00	7.00	na	na	Includes DS-401 v5.2
U	Viewlogic	X	X	X	X	X	X	DS-VL-BAS-PC1	6.0.1			7/96	6.0	Customer w/v6.0 will receive v6.0.1 update
	Viewlogic	X	X	X	X	X	X	DS-VL-STD-xxx	6.00	6.0.1		7/96	6.0	
	Viewlogic	X	X	X	X	X	X	DS-VL-ADV-xxx	7.00	7.00	7.00	na	na	
	Viewlogic/S	X	X	X	X	X	X	DS-VLS-BAS-PC1	6.0.1			7/96	6.0	Includes PROSeries 6.1
	Viewlogic/S	X	X	X	X	X	X	DS-VLS-STD-PC1	6.0.1			7/96	6.0	Includes PROSeries 6.1
	Viewlogic/S	X	X	X	X	X	X	DS-VLS-EXT-PC1	6.0.1			7/96	6.0	Incl PROSeries 6.1/PROsynth 5.02X
	Viewllogic/S	X	X	X	X	X	X	DS-VLS-ADV-PC1	7.00			na	na	
U	3rd Party Alliance	X	X	X	X	X	X	DS-3PA-BAS-xxx	6.0.1			7/96	6.0	
	3rd Party Alliance	X	X	X	X	X	X	DS-3PA-STD-xxx	6.0.1	5.2.1	5.2.1	7/96	5.2/6.0	Includes 502/550/380
	3rd Party Alliance	X	X	X	X	X	X	DS-3PA-ADV-xxx	7.00	7.00	7.00	na	na	Includes 502/550/380 & Foundry
	Foundation Series	X	X	X	X	X	X	DS-FND-BAS-PC1	6.0.1			7/96	6.0	Includes support for XC4000E and XC9500
	Foundation Series	X	X	X	X	X	X	DS-FND-BSV-PC1	6.0.1			7/96	6.0	Includes support for XC4000E and XC9500
	Foundation Series	X	X	X	X	X	X	DS-FND-STD-PC1	6.0.1			7/96	6.0	Includes support for XC4000E and XC9500
	Foundation Series	X	X	X	X	X	X	DS-FND-STV-PC1	6.0.1			7/96	6.0	Includes support for XC4000E and XC9500
	LogiCore-PCI Slave			X				LC-DI-PCIS-C	1.10	1.10	1.10	na	na	Target only; Req signed lic agreement
	LogiCore-PCI Master			X				LC-DI-PCIM-C	1.10	1.10	1.10	8/96	1.0	Initiator and target; Req signed lic agreement
	Evaluation	X	X	X	X	X	X	DS-EVAL-XXX-C	2.00	2.00	2.00	na	na	PC, Sun, HP kits now available with v5.2.1 and v6.0.1

***KEY**: N=New Product, E= Engineering software for in-warranty users by request only, U= Update by request only, PR = Pre-release requiring in-warranty status or Product Marketing apporval*

PROGRAMMER SUPPORT FOR XILINX XC1700 SERIAL PROMS-AUGUST 1996

MANUFACTURER	MODEL	XC1718D XC1736D XC1765D	XC1718L XC1765L	XC17128D XC17256D	XC17128L XC17256L
ADVANTECH	PC-UPROG				
	LABTOOL-48	Aug-96	Aug-96	Aug-96	Aug-96
ADVIN	PILOT-U24	10.84B		10.84B	
	PILOT-U28	10.84B		10.84B	
	PILOT-U32	10.84B		10.84B	
	PILOT-U40	10.84B		10.84B	
	PILOT-U84	10.84B		10.84B	
	PILOT-142	10.84B		10.84B	
	PILOT-143	10.84B		10.84B	
	PILOT-144	10.84B		10.84B	
	PILOT-145	10.84B		10.84B	
B&C MICROSYSTEMS INC.	Proteus-UP40	3.7Q		3.7Q	
BP MICROSYSTEMS	CP-1128				
	EP-1140				
	BP-1200	V3.15	V3.15	V3.15	
	BP-2100	V3.15	V3.15	V3.15	
BYTEK	135H-FT/U				
	MTK-1000				
	MTK-2000				
	MTK-4000				
DATAMAN	DATAMAN-48	V1.30	V1.30	V1.30	
DATA I/O	UniSite	Aug-96	Aug-96	Aug-96	Aug-96
	2900	Aug-96	Aug-96	Aug-96	Aug-96
	3900	Aug-96	Aug-96	Aug-96	Aug-96
	AutoSite	Aug-96	Aug-96	Aug-96	Aug-96
	ChipLab	Aug-96	Aug-96	Aug-96	Aug-96
	2700	Aug-96	Aug-96	Aug-96	Aug-96
DEUS EX MACHINA	XPGM	V1.40	V1.40	V1.40	V1.40
EETOOLS	ALLMAX/ALLMAX+	V2.4U	V2.4U	V2.4U	
	MEGAMAX	V1.1E	V1.1E	V1.1E	
ELAN DIGITAL SYSTEMS	3000-145				
	5000-145				
	6000 APS	3Q96	3Q96	3Q96	
HI-LO SYSTEMS RESEARCH	All-03A	Aug-96	Aug-96	Aug-96	Aug-96
	All-07	Aug-96	Aug-96	Aug-96	Aug-96
ICE TECHNOLOGY LTD	Micromaster 1000/E	V3.17	V3.17	V3.17	V3.17
	Speedmaster 1000/E	V3.17	V3.17	V3.17	V3.17
	Micromaster LV	V3.17	V3.17	V3.17	V3.17
	LV40 Portable	V3.17	V3.17	V3.17	V3.17
	Speedmaster LV	V3.17	V3.17	V3.17	V3.17
LEAP ELECTRONICS	LEAPER-10	V2.0		V2.0	
	LP U4	V2.0		V2.0	

MANUFACTURER	MODEL	XC1718D XC1736D XC1765D	XC1718L XC1765L	XC17128D XC17256D	XC17128L XC17256L
LINK COMPUTER GRAPHICS	CLK-3100	V5.61		V5.61	
LOGICAL DEVICES	ALLPRO-40				
	ALLPRO-88	V2.7		V2.7	
	ALLPRO-88XR	V2.7		V2.7	
	ALLPRO-96	6.5.10	6.5.10	6.5.10	6.5.10
	CHIPMASTER 2000	V2.4U		V2.4U	
	CHIPMASTER 6000	V1.31A	Aug-96	V1.31A	Aug-96
	XPRO-1	SPROM.310	SPROM.310	SPROM.310	SPROM.310
MQP ELECTRONICS	MODEL 200	6.46	6.46	6.46	
	SYSTEM 2000	2.25	2.25	2.25	
	PIN-MASTER 48	Aug-96	Aug-96	Aug-96	
MICROPROSS	ROM 5000 B	3Q96		3Q96	
	ROM 3000 U	3Q96		3Q96	
	ROM9000		3Q96		
NEEDHAM'S ELECTRONICS	EMP20	V3.10		V3.10	
RED SQUARE	IQ-180				
	IQ-280				
	Uniwriter 40				
	Chipmaster 5000				
SMS	Expert	3Q96		3Q96	
	Optima	3Q96		3Q96	
	Multisyte	3Q96	3Q96		
	Sprint Plus48	3Q96			
STAG	Eclipse	6.5.10	6.5.10	6.5.10	6.5.10
	Quasar				
SUNRISE	T-10 UDP	Aug-96		Aug-96	
	T-10 ULC	Aug-96		Aug-96	
SUNSHINE	POWER-100	Aug-96		Aug-96	
	EXPRO-60/80	Aug-96		Aug-96	
SYSTEM GENERAL	TURPRO-1	V2.26H		V2.26H	V2.26H
	TURPRO-1 F/X	V2.26H		V2.26H	V2.26H
	TURPRO-1 T/X				
	APRO	V1.24			
	MULTI-APRO	V1.16	V1.16	V1.16	V1.16
TRIBAL MICROSYSTEMS	TUP-300	Aug-96	Aug-96	Aug-96	Aug-96
	TUP-400	Aug-96	Aug-96	Aug-96	Aug-96
	FLEX-700	Aug-96	Aug-96	Aug-96	Aug-96
XELTEK	SuperPRO				
	SuperPRO II	2.4B	2.4B	2.4B	2.4B
	SuperPRO II/P	2.4B	2.4B	2.4B	2.4B
XILINX	HW-112	5.00	5.00	5.00	
	HW-130	2.01	2.01	2.01	1.00

WHITE=changed since last issue; 1736A, 1765 and 17128 columns eliminated since last issue

PROGRAMMER SUPPORT FOR XILINX XC7200 CPLDS—AUGUST 1996

MANUFACTURER	MODEL	XC7236A	XC7272A
ADVANTECH	PC-UPROG		
	LabTool-48	V1.31A	V1.31A
ADVIN SYSTEMS	Pilot-U40	10.84B	10.84B
	Pilot-U84	10.84B	10.84B
B&C MICROSYSTEMS INC.	Proteus	Aug-96	Aug-96
BP MICROSYSTEMS	BP-1200	3.15	3.15
	BP-2100	3.15	3.15
DATAMAN	DATAMAN-48	V1.30	V1.30
DATA I/O	UniSite	Aug-96	Aug-96
	2900	Aug-96	Aug-96
	3900	Aug-96	Aug-96
	AutoSite	Aug-96	Aug-96
DEUS EX MACHINA ENGINEERING	XPGM	V1.40	V1.40
EE TOOLS	ALLMAX/ALLMAX+	V2.4U	V2.4U
	MEGAMAX	V1.1E	V1.1E
ELAN DIGITAL SYSTEMS	6000 APS	3Q96	3Q96
HI-LO SYSTEMS RESEARCH	All-03A	V3.09	V3.09
	All-07	V3.09	V3.09
ICE TECHNOLOGY LTD	Micromaster 1000/E	V1.1	V1.1
	Speedmaster 1000/E	V1.1	V1.1
	Micromaster LV	V1.1	V1.1
	Speedmaster LV	V1.1	V1.1
LEAP ELECTRONICS	LEAPER-10	V2.0	V2.0
	LP U4	V2.0	V2.0
LOGICAL DEVICES	ALLPRO-88		
	ALLPRO-88XR		
	ALLPROF-96	6.4.26	6.4.26
	Chipmaster 2000	V2.4U	V2.4U
	Chipmaster 6000	V1.31A	V1.31A
	XPRO-1		
MICROPROSS	ROM9000	3Q96	3Q96
MQP ELECTRONICS	SYSTEM 2000	Aug-96	Aug-96
	PIN-MASTER 48	Aug-96	Aug-96
NEEDHAM'S ELECTRONICS	EMP20	V3.10	V3.10
SMS	Expert	3Q96	3Q96
	Optima	3Q96	3Q96
	Multisyte	3Q96	3Q96
STAG	Eclipse	6.4.26	6.4.26
SUNRISE ELECTRONICS	T-10 UDP	Aug-96	Aug-96
	T-10 ULC	Aug-96	Aug-96
SUNSHINE ELECTRONICS	POWER-100	Aug-96	Aug-96
	EXPRO-60/80	Aug-96	Aug-96
SYSTEM GENERAL	TURPRO-1/FX	Aug-96	Aug-96
	MULTI-APRO	Aug-96	Aug-96
TRIBAL MICROSYSTEMS	TUP-300	V3.09	V3.09
	TUP-400	V3.09	V3.09
	FLEX-700	V3.09	V3.09
XELTEK	SUPERPRO		
	SUPERPRO II	2.4B	2.4B
	SUPERPRO II/P	2.4B	2.4B
XILINX	HW-130	1.14	1.04

WHITE=changed since last issue

Note: The XC7236 and XC7272 columns have been eliminated

PROGRAMMER SUPPORT FOR XILINX XC7300 CPLDS-AUGUST 1996

MANUFACTURER	MODEL	7318	7336	7336Q	7354	7372	73108	73144
ADVANTECH	PC-UPROG							
	LABTOOL-48	V1.31A	V1.31A	V1.31A	V1.31A	V1.31A	V1.31A	
ADVIN SYSTEMS	PILOT-U40	10.84B	10.84B	10.84B	10.84B			
	PILOT-U84	10.84B	10.84B	10.84B	10.84B	10.84B	10.84B	10.84B
B&C MICROSYSTEMS, INC.	PROTEUS	Aug-96	Aug-96	Aug-96	Aug-96	Aug-96	Aug-96	Aug-96
BP MICROSYSTEMS	BP-1200	V3.15	V3.18	V3.15	V3.15	V3.15	V3.15	
	BP-2100	V3.15	V3.18	V3.15	V3.15	V3.15	V3.15	
DATAMAN	DATAMAN-48	V1.30	V1.30	V1.30	V1.30	V1.30	V1.30	
DATA I/O	2900	Aug-96	Aug-96	Aug-96	Aug-96			
	3900/AUTOSITE	Aug-96	Aug-96	Aug-96	Aug-96	Aug-96	Aug-96	Aug-96
	UNISITE	Aug-96	Aug-96	Aug-96	Aug-96	Aug-96	Aug-96	Aug-96
DEUS EX MACHINA ENGINEERING	XPGM	V1.40	V1.40	V1.40	V1.40	V1.40	V1.40	
EE TOOLS	ALLMAX/ALLMAX+	V2.4U	V2.4U	V2.4U	V2.4U	V2.4U	V2.4U	
	MEGAMAX	V1.1E	V1.1E	V1.1E	V1.1E	V1.1E	V1.1E	
ELAN	6000 APS	3Q96	3Q96	3Q96	3Q96	3Q96	3Q96	
HI-LO SYSTEMS RESEARCH	ALL-03A	V3.09	V3.09	V3.09	V3.09	V3.09	V3.09	
	ALL-07	V3.09	V3.09	V3.09	V3.09	V3.09	V3.09	
ICE TECHNOLOGY LTD	Micromaster 1000/E	V1.1	V1.1	V1.1	V1.1	V1.1	V1.1	V1.1
	Speedmaster 1000/E	V1.1	V1.1	V1.1	V1.1	V1.1	V1.1	V1.1
	Micromaster Lv	V1.1	V1.1	V1.1	V1.1	V1.1	V1.1	V1.1
	Speedmaster Lv	V1.1	V1.1	V1.1	V1.1	V1.1	V1.1	V1.1
LEAP ELECTRONICS	LEAPER-10	V2.0	V2.0	V2.0	V2.0	V2.0	V2.0	V2.0
	LP U4	V2.0	V2.0	V2.0	V2.0	V2.0	V2.0	V2.0
LOGICAL DEVICES	ALLPRO-88							
	ALLPRO-88XR							
	ALLPRO-96	6.4.26	6.4.26	6.4.26	6.4.26	6.4.26	6.4.26	
	Chipmaster 2000	V2.4U	V2.4U	V2.4U	V2.4U	V2.4U	V2.4U	
	Chipmaster 6000	V1.31A	V1.31A	V1.31A	V1.31A	V1.31A	V1.31A	
	XPRO-1						73108.304	
MICROPROSS	ROM9000	3Q96	3Q96	3Q96	3Q96	3Q96	3Q96	
MQP ELECTRONICS	SYSTEM 2000	Aug-96	Aug-96	Aug-96	Aug-96	Aug-96	Aug-96	Aug-96
	PINMASTER 48	Aug-96	Aug-96	Aug-96	Aug-96	Aug-96	Aug-96	Aug-96
NEEDHAM'S ELECTRONICS	EMP20	V3.10	V3.10	V3.10	V3.10	V3.10	V3.10	
SMS	EXPERT	3Q96	3Q96	3Q96	3Q96	3Q96	3Q96	3Q96
	OPTIMA	3Q96	3Q96	3Q96	3Q96	3Q96	3Q96	3Q96
STAG	ECLIPSE	6.4.26	6.4.26	6.4.26	6.4.26	6.4.26	6.4.26	
SUNRISE	T-10 UDP	Aug-96	Aug-96	Aug-96	Aug-96	Aug-96	Aug-96	Aug-96
	T-10 ULC	Aug-96	Aug-96	Aug-96	Aug-96	Aug-96	Aug-96	Aug-96
SUNSHINE ELECTRONICS	POWER-100	Aug-96	Aug-96	Aug-96	Aug-96	Aug-96	Aug-96	Aug-96
	EXPRO-60/80	Aug-96	Aug-96	Aug-96	Aug-96	Aug-96	Aug-96	Aug-96
SYSTEM GENERAL	TURPRO-1/FX	Aug-96	Aug-96	Aug-96	Aug-96	Aug-96	Aug-96	Aug-96
	MULTI-APRO	Aug-96	Aug-96	Aug-96	Aug-96	Aug-96	Aug-96	Aug-96
TRIBAL MICROSYSTEMS	Flex-700	V3.09	V3.09	V3.09	V3.09	V3.09	V3.09	
	TUP-300	V3.09	V3.09	V3.09	V3.09	V3.09		
	TUP-400	V3.09	V3.09	V3.09	V3.09	V3.09		
XELTEK	SUPERPRO							
	SUPERPRO II	2.4B	2.4B	2.4B	2.4B			
	SUPERPRO II/P	2.4B	2.4B	2.4B	2.4B			
XILINX	HW-130	1.15	1.15	1.06	1.16	1.07	1.07	1.02

WHITE=changed since last issue

XILINX ALLIANCE-EDA COMPANIES & PRODUCTS-AUGUST 1996-1 OF 2

	Company Name	Product Name	Version	Function	DesignKit	2K/3K/4K	XC5200	CPLD 7K9K	Uni Lib	PLATFORMS PC	Sun	RS6000	HP7
DIAMOND	Aldec	Active-CAD	2.0	Schematic Entry & Simulation & HDL Editor	Included	✓	✓	✓	✓	✓			
	Cadence	Verilog	2.4	Simulation	Xilinx Front End	✓	✓	7k	✓		✓	✓	✓
		Concept	2.1	Schematic Entry	Xilinx Front End	✓		7k	✓		✓	✓	✓
		FPGA Designer	9504	Topdown FPGA Synthesis	Call Xilinx	✓	✓	7k	✓		✓	✓	✓
		Synergy	2.3	FPGA Synthesis	Call Xilinx	✓	✓	7k	✓		✓	✓	✓
		Composer	4.4	Schematic Entry	Xilinx Front End	✓		7k	✓		✓	✓	✓
	Mentor Graphics	Autologic	B.x	Synthesis	Xilinx Synthesis Lib.	✓	✓	7k	✓		✓	✓	✓
		Design Architect	B.x	Schematic Entry	Call Xilinx	✓	✓	7k	✓		✓	✓	✓
		QuickSim II	B.x	Simulation	Call Xilinx	✓	✓	7k	✓		✓	✓	✓
		QuickHDL	B.x	Simulation	Call Xilinx	✓	✓	7k	✓		✓	✓	✓
	OrCAD	Simulate (Win)	6.10	Simulation	Call Xilinx	✓	✓	7k		✓			
		VST 386+ (DOS)	1.2	Simulation	Call Xilinx	✓		7k	✓	✓			
		Capture (Win)	7.0	Schematic Entry	Call Xilinx	✓	✓	7k	✓	✓			
		SDT 386+ (DOS)	1.2	Schematic Entry	Call Xilinx	✓		7k	✓	✓			
		PLD 386+ (DOS)	2.0	Synthesis	Call OrCAD	✓		7k		✓			
	Synario Design Automation	ABEL	6.2	Synthesis, Simulation	XEPLD Fitter			✓	✓	✓			
		Synario	2.2	Schematic Entry, Synthesis & Simulation	SYN-LCA	✓	✓	✓	✓	✓			
	Synopsys	FPGA Compiler	3.4b	Synthesis	Call Xilinx	✓	✓	✓	✓		✓	✓	✓
		VSS	3.4b	Simulation	Call Xilinx	✓	✓	✓	✓		✓	✓	✓
		Design Compiler	3.4b	Synthesis	Call Xilinx	✓	✓	✓	✓		✓	✓	✓
		FPGA Express	1.0	Synthesis	Call Xilinx	✓	✓			✓			
	Viewlogic	WorkView Office	7.1.2/7.2	Schem/Sim/Synth	Call Xilinx	✓	XACT6	✓	✓	✓	✓	✓	✓
		ProSynthesis	5.02	Synthesis	Call Xilinx	✓	XACT6	7k	✓	✓	✓	✓	✓
		ProSim	6.1	Simulation, Timing Analysis	Call Xilinx	✓	XACT6	7k	✓	✓	✓	✓	✓
		ProCapture	6.1	Schematic Entry	Call Xilinx	✓	XACT6	7k	✓	✓	✓	✓	✓
		PowerView	6.0	Schem/Sim/Synth/Timing Anal	Call Xilinx	✓	✓	✓	✓		✓	✓	✓
RUBY	Capilano Computing	Design Works	3.1	Schematic Entry/Sim	XD-1	✓			✓	✓			
	Compass Design Automation	ASIC Navigator		Schematic Entry	Xilinx Design Kit	✓	✓	7k			✓		✓
		X-Syn		Synthesis		✓					✓		✓
		QSim		Simulation		✓	✓	7k			✓		✓
	Escalade	DesignBook	2.0	Design Entry		✓			✓	✓	✓		
	Exemplar Logic	Galileo	3.2	Synthesis/Timing Analysis Simulation	Included	✓	✓	✓	✓	✓	✓		✓
	IK Technology Co.	Ishizue Professionals	1.05.02	Schematic Entry/Simulation	Xilinx Design Kit	✓				✓	✓		✓
	IKOS Systems	Voyager	2.11	Simulation	Xilinx Tool Kit	✓					✓		✓
	INCASES Engineering GmbH	Theda	4.0	Schematic Entry	Xilinx Kit	✓							✓
	ISDATA	LOG/iC Classic	4.2	Synthesis	LCA-PP	✓		7k	✓	✓	✓		✓
		LOG/iC2	4.2	Synthesis Simulation	Xilinx Mapper	✓	✓	7k	✓	✓	✓		✓
	Logic Modeling Corp. (Synopsis Division)	Smart Model		Simulation Models	In Smart Model Lib.	✓	✓	7k,9k		✓	✓	✓	✓
		LM1200		Hardware Modeler	Xilinx Logic Module	✓		7k,9k		✓	✓	✓	
	Model Technology	V-System/VHDL	4.4j (PC) 4.6a (WS)	Simulation		✓			✓	✓	✓	✓	✓
	Protel Technology	Advanced Schematic	3.1	Schematic Entry/Client Server	Xilinx Interface	✓		7k		✓			
	Quad Design Technology	Motive	4.3	Timing Analysis	XNF2MTV	✓				✓	✓	✓	✓
	SimuCad	Silos III	95.100	Simulation	Included	✓			✓	✓			
	Sophia Sys & Tech	Vanguard	5.31	Schematic Entry	Xilinx I/F Kit	✓		✓		✓	✓		✓
	Summit Design Corp.	Visual HDL	3.0	Graphical Design Entry/Simulation/Debug	EDIF Interface	✓	✓	✓	✓	✓	✓	✓	✓
	Synplicity, Inc.	Synplify-Lite	2.6a	Synthesis	Xilinx Mapper	✓	✓	9k	✓	✓	✓		✓
		Synplify	2.6a	Synthesis	included	✓	✓	9k	✓	✓	✓		✓
	TopDown Design Solutions	V-BAK	1.1	XNFto VHDL translator	XNFinterface	✓	✓		✓	✓	✓	✓	

XILINX ALLIANCE-EDA COMPANIES & PRODUCTS-AUGUST 1996-2 OF 2

	Company Name	Product Name	Version	Function	DesignKit	2K/3K/4K	XC 5200	CPLD 7K9K	Uni Lib	PLATFORMS PC	Sun	RS6000	HP7
RUBY	Veda Design Automation Inc	Vulcan	4.5	Simulation	XILINX Tool Kit	✓					✓		✓
RUBY	Veribest	Veribest VHDL	14.0	Schematic Entry	Xilinx FPGA Design Kit	3k,4k			✓	✓	✓		✓
		Veribest Verilog	14.0	Simulation	Xilinx FPGA Design Kit	3k,4k			✓	✓	✓		✓
		VeriBest Simulator	14.0	Simulation	Xilinx FPGA Design Kit	3k,4k	✓		✓	✓	✓		✓
		DMM	14.x	Design Management	Xilinx FPGA Design Kit	3k,4k	✓		✓	✓	✓		✓
		VeriBest Synthesis	14.0	Synthesis	Xilinx FPGA Design Kit	3k,4k	✓		✓	✓	✓		✓
		Synovation	12.2	Synthesis	Xilinx FPGA Design Kit	3k,4k			✓	✓	✓		✓
		PLDSyn	12.0	Design Entry Synthesis		✓		7k		✓	✓		✓
		VerBest Design Capture	14.x	Design Capture	Xilinx FPGA Design Kit	3k,4k	✓		✓	✓	✓		✓
EMERALD	Accolade Design Automation	Peak FPGA Plus	2.2	HDL, Synthesis, Simulation	Included	✓	✓	✓	✓	✓			
EMERALD	ACEO Technology, Inc.	Asyn	3.3	Synthesis	Included	✓	✓		✓	✓	✓	✓	✓
		Softwire	3.3	Multi-FPGA Partitioning	Included	✓	✓		✓	✓	✓	✓	✓
		Gatran	3.3	ASIC to FPGA Netlist Mapping	Included	✓	✓		✓	✓	✓	✓	✓
EMERALD	Acugen Software, Inc.	Sharpeye	2.60	Testability Analysis	AALCA interface	✓	✓	7k		✓	✓		✓
		ATGEN	2.60	Automatic Test Generation	AALCA interface	✓	✓	7k		✓	✓		✓
EMERALD	ALPS LSI Technologies, Inc.	Edway Design Systems		Synthesis/Simlulation		✓		✓		✓			
EMERALD	Aptix Corporation	System Explorer	2.1	System Emulation	Axess 2.Yes	✓							
EMERALD	Aptix Corporation	ASIC Explorer	2.3	ASIC Emulation	Axess 2.3	4K	✓		✓				
EMERALD	Aster Ingenierie S.A.	XILLAS	4.1	LASAR model generation	Worst Case Simulation	✓		7k		✓	✓		✓
EMERALD	Chronology Corporation	TimingDesigner	3.0	Timing Specification and Analysis	Included	✓	✓	7k,9k	✓	✓	✓		✓
		QuickBench	1.0	Visual Test Bench Generator	Included	✓	✓	7k,9k	✓	✓	✓		✓
EMERALD	CINA-Computer Integrated Network Analysis	SmartViewer	1.0c	Schematic	XNFInterface	✓		7k		✓			
EMERALD	Epsilon Design Systems	Logic Compressor		Synthesis optimization		✓	✓			✓	✓	✓	✓
EMERALD	Flynn Systems	Probe	3.0	Testability Analysis	Xilinx Kit	✓	✓	7k		✓			
		FS-ATG	3.0	Test Vector Generation	Xilinx Kit	✓	✓	7k		✓			
		CKTSIM	3.0	Logic Analysis	Xilinx Kit	✓	✓	7k		✓			
		FS-SIM	3.0	Simulation	Xilinx Kit	✓	✓	7k		✓			
EMERALD	Fujitsu LSI	PROVERD		Top-Down Design System	Included	3k,4k				✓			
EMERALD	Harmonix Corporation	PARTHENON	2.3	Synthesis		4k		7k		✓	✓		
EMERALD	MINC	PLDesigner-XL	3.3	Synthesis	Xilinx Design Module	✓				✓	✓		✓
EMERALD	Teradyne	Lasar	6	Simulation	Xilinx I/F Kit	✓					✓		✓
EMERALD	The Rockland Group	One-Hot State Machine Lib.		Graphic Design for One-Hot State Machines	Xilinx Kit	✓	✓		✓	✓	✓	✓	✓
EMERALD	Tokyo Electron Limited	ViewCAD	1.2	FLDL to XNF translator	XNFGEN	✓							
EMERALD	Trans EDA Limited	TransPRO	1.2	Synthesis	Xilinx Library	✓					✓		✓
EMERALD	Zuken	Tsutsuji		Synthesis/Simulation	XNFInterface	3k,4k					✓	✓	✓
EMERALD	Zycad	Paradigm RP		Rapid Prototyping		✓					✓		✓
		Paradigm XP		Gate-level Sim		✓					✓		✓

Alliance Program Categories:

Diamond: These partners have strong strategic relationships with Xilinx and have a direct impact on our releases. Typically, Xilinx is directly involved in the development and testing of the interface to XACT*step* software for these products.

Ruby: These partners have a high degree of compatibility and have repeatedly shown themselves to be significant contributors to our users' development solutions.

Emerald: Proven Xilinx compatibility

XILINX ALLIANCE-EDA CONTACTS-AUGUST 1996

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XCell 3Q96 Reader Survey

Dear Reader,

XCell is intended to provide you, our users, with the latest information about Xilinx products and their applications. In this issue, we'd like to get your feedback on the effectiveness of this publication. By answering the following questions, you'll help us determine which articles are the most useful to you. In addition, we'd like your suggestions on how to improve the distribution of the *XCell* newsletter. Our goal is to make *XCell* a source of information to help you get the most out of Xilinx products and services.

After marking your choices, please tear off or copy the page and send it to:

Of course, any additional comments are welcome.

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Fax: 408-879-4676

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Guest editorial: *Xilinx senior staff members highlight the companies strategies and directions.*	1	2	3	4	5
Customer success story: *Applications that currently use Xilinx products.*	1	2	3	4	5
General interest features: *Updates on new product literature, technical conferences, financial status*	1	2	3	4	5

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Development systems: *Additions to our development system product line.*	1	2	3	4	5
Design hints and issues	1	2	3	4	5
Recurring, informational charts *Current availability of components, development systems and third-party programmers and software.*	1	2	3	4	5

COMMENTS: _____

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Please use this form to FAX in your comments and suggestions, or to request an addition to the XCELL mailing list. Please feel free to make copies of this form for your colleagues.

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