Part 1 of 2

PLDs, Pins and PCBs

By BRADLY FAWCETT ◆ Editor

Change is inevitable. The best system designers recognize this axiom and incorporate tolerance for change into their schedules, design methodologies, and even the physical realizations of their designs.

Changes can occur during all stages of a product's life cycle. Surveys suggest that as much as 50% of the typical product's development time is spent in the debug/modify/re-implement cycle that occurs after the first prototype is created. Even if the designer is skilled (and lucky) enough to create a working prototype on the first try, the product specification can change in the meantime in response to changing market conditions. In some cases, products that already have been produced and sold for months or even years have been modified to extend the product's life (or, heaven forbid, to correct some previously undetected flaw).

Tolerance of change is one of the prime attractions of programmable logic devices. With PLDs, design changes can be implemented quickly and easily, especially as compared to custom and semicustom IC technology. However, when it comes to tolerating changes, printed circuit boards (PCBs) are more like custom ICs than PLDs. To modify a PCB, new drawings (masks) must be created, and new prototypes must be manufactured, with all the associated expenses and delays.

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Thus, to garner the true benefits of the adaptability of programmable logic, programmable logic device architectures should isolate the PCB design from logic changes that occur within the device. As a result, two concepts that should be of primary concern to PLD users are pin-locking and footprint compatibility.

Pin-locking refers to the ability to establish a fixed pin location for all the signals entering and leaving a PLD so that the PCB layout, in turn, can be fixed. Since PCB design and production is often a critical path in product development, most designers would prefer to lock PLD pin locations early in the design cycle. However, with some PLDs, this can be a risky proposition; the chosen pinout may prove to be less than optimal after the implementation of the inevitable design changes, leading to decreased performance, or, in the worse case, a design that cannot be implemented at all due to routing limitations within the PLD. Designers that used the earliest generations of CPLDs and FPGAs may recall that PLD manufacturers routinely warned their users not to begin their PCB design until the PLD design was completed and debugged. This reputation, established in the early days of high-density PLDs — that is, that design changes can be difficult or impossible to implement without changing the device pinout — lingers on today (and deservedly so, for some of our competitors' offerings!).

However, those days have long passed for Xilinx FPGA and CPLD devices.

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Pin-locking is not an issue with Xilinx CPLDs. The XC9500 CPLD family offers the ultimate in pin-locking capability, with 100% connectivity through the CPLD's internal switch matrix. Thus, any I/O pin can be connected to any function block input or output, regardless of utilization levels. Design changes internal to the CPLD will seldom force pinout changes.

While the Xilinx FPGA families cannot provide the same guarantee of full connectivity offered by the Xilinx CPLDs, the latest generations do provide a high degree of flexibility in their I/O connections. All recent Xilinx FPGA architectures, including the XC5200, XC4000E, XC4000X, and XC6200 families, embrace the VersaRing™ concept introduced in the XC5200 family. Simply put, these FPGAs include an extra layer of routing resources along the perimeter of the logic array to increase routing flexibility between the internal array and the I/O blocks. User feedback is confirming that these devices deliver on the promise of allowing last-minute design changes without changes to the I/O pin locations.

Actually, this capability also is present to a large degree in the "older" XC4000 series FPGAs. The popular XC4000 family was the subject of the only independent research study (that I know of) that examined pin-locking in FPGA architectures. As reported at the 3rd Canadian Workshop on Field-Programmable Devices last May, researchers at the University of Toronto implemented sixteen different designs in XC4000 devices. The designs were first routed with no placement constraints, then with "bad" pin constraints (wherein signals that were assigned to adjacent pins in the unconstrained design were now assigned to opposite ends of the device), and, lastly, with a randomly-generated pin placement. In every case, the designs routed to completion, albeit with a slight performance impact; the average signal delay increase was less than 5% for the "bad" constraints and 3% for the random constraints. Significantly, the researchers concluded that "Fixed pin assignment does impact routability significantly, because the amount of routing resources used was increased, but the Xilinx XC4000 series architecture provided sufficient resources to handle the increased demand". Incidentally, a major competitor's FPGA family — the only other device included in the study — did not fare nearly as well; several designs were unroutable with bad or random pin constraints, and the researchers recommended that users of that FPGA "should leave about 20% of the logic elements and I/O pins free to avoid routability problems due to pin constraints."

In conclusion, while "intelligent" placement of I/O pins is still recommended, Xilinx FPGA and CPLD devices are quite tolerant of design changes without forcing the redesign of the PCB layout. This facilitates an early release of the PCB design and eases the debugging process, thereby accelerating time-to-market, and accommodates the inevitable changes that occur throughout a product's total life cycle.

In the next issue, part 2 of this article will examine the benefits of footprint compatibility both within and across Xilinx PLD product families. ◆

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