XNF XC7000 Specification

ADDENDUM TO XILINX XNF SPECIFICATION
September 5, 1995

1.0 Introduction

This document summarizes the distinguishing features of XNF netlists specific to the XC7000 Family of EPLDs. Specifically, it defines the entire set of XNF primitive symbols and parameters supported by 7000. Where 7000 features are supported in an identical manner as in LCA, readers should refer to the Xilinx XNF Specification. In general, the XNF netlist syntax used for 7000 is the same as described in the Xilinx XNF Specification and is not discussed in this document.

2.0 7000 Family Primitive Symbols

All of the primitive symbols supported by the 7000 family for design entry in Version 6.x are listed below. Of these, only a subset are used to support functional and timing simulation, as indicated. The DLAT is used only to support simulation and is not used for design entry.

The XNF netlist used to capture the user's design does not directly support functional simulation. Instead, a Xilinx translator reads the original XNF netlist, resolves all parameters which affect functionality, and generates a functionally equivalent XNF simulation netlist containing explicit logic and flip-flop symbols. The translator also connects the 7000 global master reset signal, MRESET, to the CLR or PRE input of all flip-flop and latch elements in the model, according to any specified initial state parameters (INIT). Therefore, the XNF-to-simulator translators do not need to automatically connect any global initialization signal (such as PRLD, GR or GSR) to the flip-flop and latch symbols in the XNF simulation netlists for 7000.

Some of the descriptions below list prominent interconnection restrictions. All such restrictions are checked by the 7000 implementation software (XEPLD) and do not also need to be checked by any interface translator software. The restrictions listed below do not represent the complete set of restrictions imposed by 7000 design rules.

2.1 Inverters and Buffers

BUF and INV symbols are supported as for all LCA families. Buffers in 7000 can also be used to represent break points for logic path optimization by applying the OPT=OFF 7000-specific parameter. BUF and INV are used in simulation netlists.

Pins: I, O
Invertible pins: all

2.2 Combinational Logic

AND, NAND, OR, NOR, XOR and XNOR symbols are supported as for LCA. The AND, NAND, OR, and NOR gates can have a maximum of 9 inputs. The XOR and XNOR gates can have a maximum of 4 inputs. All combinational gates are used in simulation netlists.

Pins: I0, I1, I2,..., O
Invertible pins: all

Like LCA, the pin names on combinational logic symbols do not need to be preserved; the 7000 restriction described in the XNF 5.0 Specification no longer applies. The functionality of each pin is determined by the direction and inversion fields of the PIN record. All of the pins on combinational gates are invertible.

AND and NAND symbols can accept the OPT=UIM 7000-specific parameter.

2.3 Input/Output Pads

IPAD, OPAD, IOPAD and UPAD symbols are supported as for LCA, and translate into EXT records. In 7000 designs, pad symbols accept the LOC=pin_number and FAST parameters, as for LCA. For the LOC parameter, pin_number must be a single, explicit pin number.

2.4 Input/Output Buffers

IBUF, OBUF and OBUFT symbols are supported as for the 3000 family. The 7000 family does not support the GTS signal. Input/output buffers are used in simulation netlists.

IBUF pins: I (external), O.
OBUF pins: I, O (external).
OBUFT pins: I, T, O (external).
Invertible pins: internal pins (I, T) on output buffers (OBUF, OBUFT).
No pins on IBUF are invertible.

OBUF and OBUFT accept the FAST parameter as an alternative to placing it on a pad symbol.

2.5 Input Flip-Flops

INFF symbols are supported similar to LCA. The 7000 family INFF is an input flip-flop with an active-low clock-enable input pin, CE. INFF corresponds to the 7000 unified library symbol IFDX1. INFF is not used in simulation netlists.

INFF pins: D (external), C, CE, Q.
Invertible pins: none.

Pin CE is an active-low clock-enable input and must be connected to a BUFG symbol (with SCHNM=BUFCE) in the design, if it is used.

INFF can accept the INIT parameter.

2.6 Input Latch

INLAT symbols are supported as for LCA. INLAT corresponds to the 7000 unified library symbol ILD. INLAT is not used in simulation netlists.

INLAT pins: D (external), G, Q.
Invertible pins: none.

INLAT can accept the INIT parameter.

2.7 Flip-Flops

DFF symbols are supported similar to the 2000 family. The 7000 DFF symbol has no GR input. DFF corresponds to the 7000 unified library symbol FDCP. DFF is used in simulation netlists, in which it represents the FDCPX1 simulation model.

DFF pins: D, C, CLR, PRE, Q
Invertible pins: C

DFF can accept the INIT parameter.

A DFF can be used to implement a D-type latch by connecting appropriate logic to its CLR and PRE inputs and connecting its C and D inputs to ground (GND). No other internal latch primitives are supported by 7000.

2.8 Internal 3-State Buffer

TBUF symbols are supported as for LCA. TBUF corresponds to the 7000 unified library symbol BUFT. TBUF is used in simulation netlists.

TBUF pins: I, T, O.
Invertible pins: I, T.

2.9 Global Buffers

BUFG symbols are used to represent any of three global control signals in 7000. The 7000 unified library symbols BUFG, BUFFOE and BUFCE represent the Fast Clock (FCLK), the Fast Output Enable (FOE) and Clock Enable (CE) global control pins of 7000 family devices. The BUFG XNF primitive represents these three schematic library symbols. The SCHNM parameter is required to distinguish between the particular global signal types. BUFG symbols are not used in simulation netlists.

BUFG pins: I (optionally external), O.
Invertible pins: none.

When SCHNM=BUFG, the O pin may connect only to the C input of flip-flop symbols (DFF, INFF, FBMC or FFBMC) or the G input of the INFF symbol.

When SCHNM=BUFFOE, the O pin may connect only to the T input of the OBUFT symbol through an inverter.

When SCHNM=BUFCE, the O pin may connect only to the CE input of the INFF symbol.

2.10 Timing Specification Symbols

TIMESPEC and TIMEGRP symbols are supported as for LCA.

2.11 7000 Family High-Density Function Block

FBMC symbols represent the configurable macrocell logic contained in a 7000 family High-Density Function Block. FBMC is not used in simulation netlists.

Input pins: D1, D2, FBK, C, CLR, PRE, CI
Output pins: Q, CO
Invertible pins: none.

The CI and CO pins represent the arithmetic or shift carry chain between adjacent 7000 macrocells. The CI input may connect only to the CO output of one other FBMC symbol (or to ground if not used), and vise-versa. (Exception: CI may connect to the Q output of one other FBMC if parameter ADD=SHIFT is specified.)

FBMC accepts the INIT parameter, as used on DFF for LCA.

The FBMC also accepts the following 7000-specific parameters:

ALU = op_code
ADD = OFF | ON | SHIFT
FBKINV = OFF | ON
TYPE = DFF | COMB

2.12 7000 Family Fast Function Block

FFBMC symbols represent the configurable macrocell logic contained in a 7000 family Fast Function Block (FFB). FFBMC is not used in simulation netlists.

Input pins: DT, C, CLR, PRE, EXP, CI
Output pins: Q, CO
Invertible pins: none.

The CI and CO pins represent the product-term exporting path between adjacent 7000 FFB macrocells. The CI input may connect only to the CO output of one other FFBMC symbol (or to ground if not used), and vise-versa.

FFBMC accepts the INIT parameter, as used on DFF for LCA.

The FFBMC also accepts the following 7000-specific parameter:

TYPE = DFF | TFF | COMB

2.13 DLAT Simulation Latch

The DLAT symbol is a transparent latch with clear and preset, similar to the 2000 family, used only for functional and timing simulation and not for design entry. A DLAT symbol should not be included in a schematic capture library unless it is required to support simulation. The DLAT is used in XNF simulation netlists generated by the Xilinx translation software to simulate each IOB latch (originally an INLAT symbol in the design entry XNF file). The CLR and PRE pins are used by the software to connect the 7000 Master Reset signal (MRESET) in the simulation netlist. The DLAT symbol represents the LDCPX1 simulation model.

DLAT pins: D, G, CLR, PRE, Q.
Invertible pins: none.

3.0 7000 Family Parameters

All of the parameters supported by the 7000 family for design entry are listed below. The 7000 fitter acknowledges these parameters whether they appear as actual XNF parameters (OPT=OFF) or as user parameters (=OPT=OFF). None of the parameters listed below, except SCHNM, are used in simulation netlists produced by Xilinx software.

3.1 LOC

For 7000 designs, LOC can appear on EXT records to assign an input/output pad to a specific device pin by applying it to a pad symbol (IPAD, OPAD or IOPAD). In this application, the LOC parameter value can only be a single, explicit pin number, such as “P67” (PC or PQ type package) or “K11” (PG or BG type package). Pin ranges, neighborhoods and excluded ranges are not supported for 7000 designs.

LOC can also be applied to functional (non-I/O) symbols, such as gates or flip-flops, to specify a Function Block or macrocell-within-FB destination. “LOC=FBnn” specifies that the designated symbol is to be placed anywhere inside Function Block nn, assuming the symbol is not optimized into a non-macrocell resource (such as the UIM).
“LOC=FBnn_m” specifies that the designated symbol is to be placed into macrocell m of Function Block nn, assuming the symbol is not optimized into a non-macrocell resource.

3.2 FILE

FILE is used to specify the name of an XNF file defining the functionality of a custom symbol, as for LCA. The XNF files referenced by FILE parameters are flattened into the main design before the netlist is read by the fitter, unless the parameter DEF=PLD is specified. Users normally specify both FILE and DEF=PLD on symbols that are behaviorally-defined using PLUSASM equations.

3.3 DEF

For 7000, the parameter DEF=PLD indicates that a symbol should not yet be flattened because there is an associated PLUSASM equation file that must be processed to create its

XNF file. After creating the XNF file for the embedded symbol, the Xilinx translation software removes the DEF=PLD parameter from the symbol in the intermediate XNF file representing the top-level design, allowing the symbol to be flattened. In Version 6.0, all behaviorally-defined modules are translated into XNF and flattened into the main design before the netlist is read by the fitter.

3.4 PLD

To maintain backward-compatibility for existing 7000 designs, the parameter “PLD=filename” should be interpreted the same as DEF=PLD, indicating that a symbol should not yet be flattened because there is an associated PLUSASM equation file that must be processed to create its XNF file. The value of the PLD parameter is the name of the equation file and of the resulting XNF file. After creating the XNF file for the embedded symbol, the Xilinx translation software (xemake6) replaces the PLD=filename parameter with FILE=filename on the symbol in the intermediate XNF file representing the top-level design, allowing the symbol to be flattened. In Version 6.x, all behaviorally-defined modules are translated into XNF and flattened into the main design before the netlist is read by the fitter.

The PLD parameter should not be documented and need not be supported for new design entry interfaces because it is an obsolete parameter.

3.5 INIT

INIT=R|S can be applied to any flip-flop symbol (DFF, INFF, FBMC, FFBMC) or the INLAT symbol to define the initial state after the MRESET pulse is applied, as in LCA designs when the GR/GSR pulse is applied.

3.6 SCHNM and LIBVER

These parameters are used by interface software for library symbol tracking, as for LCA designs. They are required by the fitter only for the BUFG symbol to distinguish the type of global control signal required.

3.7 FAST

FAST can be applied to output or I/O pad symbols (OPAD, IOPAD) or output buffer symbols (OBUF, OBUFT) to control output slew rate (for 7000 devices with slew-rate control), as in LCA. FAST parameters should propagate from macro symbols onto all output pad or output buffer symbols contained in the macro.

3.8 OPT

The 7000-specific OPT=OFF|ON|MERGE parameter can be applied to any non-I/O symbol to control optimization. The OPT=UIM parameter can be applied only to AND or NAND symbols. The OPT parameter should propagate from macro symbols onto all symbols contained in the macro.

3.9 LOWPWR

The 7000-specific LOWPWR=ON|OFF parameter can be placed on any non-I/O symbol to control macrocell low-power operating mode. The LOWPWR parameter should propagate from macro symbols onto all symbols contained in the macro.

3.10 MINIM

The 7000-specific MINIM=ON|OFF parameter can be applied to any non-I/O symbol to control logic minimization. The MINIM parameter should propagate from macro symbols onto all symbols contained in the macro.

3.11 FBMC-Specific Parameters

The ALU=value, ADD=value and FBKINV=value parameters can be applied only to the 7000-specific FBMC symbol to define its functional modes.

The TYPE=value parameter can be applied only to the FBMC or FFBMC symbol to define its register mode.

FBMC-specific parameters are not applied to macro symbols.

3.12 INV

The INV pin parameter inverts the sense of pins, where allowed, as in LCA.

3.13 F and H

The 7000-specific signal parameters, F and H, are used to designate HDFB vs. FFB output signals, as well as Fast-Input signals.

3.14 TIMESPEC Support Parameters

The TNM and TSidentifier parameters are supported as for LCA.

3.15 User Parameters

The following “User Parameters” are useful in 7000 designs to globally control the fitter’s optimization routines from within the user design. (The normal mechanism for controlling these optimizations is the Xilinx Design Manager interface.)

=CLOCK_OPT=OFF
=REG_OPT=OFF
=FOE_OPT=OFF
=PRELOAD_OPT=OFF
=DENSITY_OPT=OFF

=MRINPUT=ON
=LOWPWR=ALL

The following user parameters are also supported, but not encouraged for user designs:

=LOGIC_OPT=OFF
=MINIMIZE=OFF
=UIM_OPT=OFF

3.16 Group and Chip

The 7000-specific GROUP=value and CHIP=value parameters can be applied to any non-I/O symbol to control the new multi-chip partitioning feature. The GROUP and CHIP parameters should propagate from macro symbols onto all non-I/O symbols contained in the macro.

4.0 Unified Library Name Conversion

The following is a list of all 7000 Unified Library symbols implemented as primitives in the CAE-tool library, and the corresponding XNF symbol names that should be used by the schematic-to-XNF translator to represent them:

Unified Library Name	XNF Primitive Name
ANDn[Bm]	AND
NANDn[Bm]	NAND
ORn[Bm]	OR
NORn[Bm]	NOR
XORn	XOR
XNORn	XNOR
BUF	BUF
BUFCE	BUFG
BUFFOE	BUFG
BUFG	BUFG
BUFGP	BUFG
BUFGS	BUFG
BUFT	TBUF
FBMC	FBMC
FFBMC	FFBMC
FDCP	DFF
IBUF	IBUF
IFDX1	INFF
ILD	INLAT
INV	INV
OBUF	OBUF
OBUFT	OBUFT
TIMEGRP	TIMEGRP
TIMESPEC	TIMESPEC
GND, VCC	(PWR record)
IPAD, OPAD, IOPAD, UPAD	(EXT record)