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LIBRARIES SUPPLEMENT GUIDE

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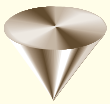

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Trademark Information

Introduction

This supplement documents new library architectures or supersets of existing ones that have been developed since the XACT 5.0 release of the Unified Libraries. It also lists the Configurable Logic Block (CLB) count of elements and which elements are Relationally Placed Modules (RPM) by architecture. The information contained in this supplement will be incorporated in the *Libraries Guide* when that manual is reissued.

Like the *Libraries Guide*, the design elements in this supplement are organized in alphanumeric order by architecture, with all numeric suffixes in ascending order. A graphic symbol, functional description, primitive versus macro table, truth table (when applicable), and schematics for each implementation, generally the 8-bit version, are included for each design element.

Note: XC8000 design elements are not included in this supplement. They are currently documented in the *Series 8000 User Guide*.

Supplement Contents

This supplement consists of the "Introduction," "Selection Guide and Constraints and Attributes," and "New Design Elements (XC4000E and XC5200)" chapters.

CLB Count, RPMs, Constraints and Attributes

CLB count information for the XC2000, XC3000, and XC4000/4000E architecture design elements is provided in alphanumeric order.

Relationally Placed Modules (RPMs) are discussed in the "Attributes, Constraints, and Carry Logic" chapter of the *Libraries Guide*. Existing and new non-carry logic RPMs are listed by architecture in this chapter of the supplement for easy identification.

New Design Elements (XC4000E and XC5200)

This chapter contains information about the XC4000E and XC5200 elements. XC4000E is a superset of the XC4000 architecture. It presents symbols, macro versus primitive tables, truth tables (when applicable), and schematics in the same form as the existing elements in the *Libraries Guide*.

Selection Guide and Constraints and Attributes

This chapter provides the CLB count for XC2000, XC3000, and XC4000 design elements. It also provides a list of the Relationally Placed Modules (RPMs) by family; a functional category selection guide of new XC4000E and XC5200 design elements; and constraints and attributes specific to XC5200 elements.

CLB Count

The "CLB Count" table lists the design elements in alphanumeric order with the CLB count for each applicable architecture.

Table 2-1 CLB Count

Element Name	XC2000	XC3000	XC4000/ 4000E
ACC1	6	-	-
ACC4	-	9	7
ACC8	-	17	12
ACC16	-	33	19
ADD1	1	-	-
ADD4	-	5	4
ADD8	-	9	6
ADD16	-	17	10
ADSU1	2	-	-
ADSU4	-	5	4
ADSU8	-	9	6

Element Name	XC2000	XC3000	XC4000/ 4000E
ADSU16	-	17	10
AND5	2	-	-
AND5B1	2	-	-
AND5B2	2	-	-
AND5B3	2	-	-
AND5B4	2	-	-
AND5B5	2	-	-
AND6	2	2	1
AND7	2	2	1
AND8	3	2	-
AND9	3	2	1
BRLSHFT4	-	4	4
BRLSHFT8	-	12	13
CB2CE	2	3	2
CB2CLE	5	4	3
CB2CLED	5	4	4
CB2RE	3	3	2
CB4CE	5	4	3
CB4CLE	10	8	6
CB4CLED	13	9	7
CB4RE	6	4	5
CB8CE	10	8	6
CB8CLE	21	16	14
CB8CLED	23	17	16
CB8RE	13	9	10
CB16CE	21	15	11
CB16CLE	42	32	26
CB16CLED	47	34	30
CB16RE	26	18	19
CC8CE	-	-	6
CC8CLE	-	-	7

Element Name	XC2000	XC3000	XC4000/ 4000E
CC8CLED	-	-	12
CC8RE	-	-	7
CC16CE	-	-	10
CC16CLE	-	-	11
CC16CLED	-	-	21
CC16RE	-	-	11
CD4CE	6	4	3
CD4CLE	8	6	5
CD4RE	7	5	6
CD4RLE	10	7	6
CJ4CE	4	2	2
CJ4RE	4	2	2
CJ5CE	5	3	3
CJ5RE	5	3	3
CJ8CE	8	4	4
CJ8RE	8	4	4
COMP2	1	1	1
COMP4	5	4	1
COMP8	11	9	2
COMP16	21	17	5
COMPM2	3	3	1
COMPM4	9	8	4
COMPM8	21	19	9
COMPM16	45	39	20
COMPMC8	-	-	6
COMPMC16	-	-	10
CR8CE	8	8	8
CR16CE	16	16	16
D2_4E	2	2	2
D3_8E	8	4	4
D4_16E	17	16	16

Element Name	XC2000	XC3000	XC4000/ 4000E
FD4CE	4	2	2
FD4RE	4	2	2
FD8CE	8	4	4
FD8RE	8	4	4
FD16CE	16	8	8
FD16RE	16	8	8
FDC	1	1	1
FDC_1	1	1	1
FDCE	1	-	-
FDCE_1	1	1	1
FDCPE	2	-	-
FDP	-	-	1
FDP_1	-	-	1
FDPE_1	-	-	1
FDR	1	1	1
FDRE	2	1	1
FDRS	1	1	1
FDRSE	3	1	1
FDS	1	1	1
FDSE	2	1	1
FDSR	1	1	1
FDSRE	3	1	1
FJKC	1	1	1
FJKCE	2	1	1
FJKCP	2	-	-
FJKCPE	2	-	-
FJKP	-	-	1
FJKPE	-	-	1
FJKRSE	3	2	2
FJKSRE	3	2	1
FTC	1	1	1

Element Name	XC2000	XC3000	XC4000/ 4000E
FTCE	1	1	1
FTCLE	3	1	1
FTCP	1	-	-
FTCPE	2	-	-
FTCPLE	3	-	-
FTP	-	-	1
FTPE	-	-	1
FTPLE	-	-	1
FTRSE	3	1	1
FTRSLE	4	3	2
FTSRE	3	1	1
FTSRLE	4	3	2
LD	1	-	-
LD4CE	4	-	-
LD8CE	8	-	-
LD16CE	16	-	-
LD_1	1	-	-
LDC	1	-	-
LDC_1	1	-	-
LDCPE	2	-	-
M2_1	1	1	1
M2_1B1	1	1	1
M2_1B2	1	1	1
M2_1E	1	1	1
M4_1E	3	3	1
M8_1E	7	5	3
M16_1E	14	13	5
NAND5	2	-	-
NAND5B1	2	-	-
NAND5B2	2	-	-
NAND5B3	2	-	-

Element Name	XC2000	XC3000	XC4000/ 4000E
NAND5B4	2	-	-
NAND5B5	2	-	-
NAND6	2	2	1
NAND7	2	2	1
NAND8	3	2	1
NAND9	3	2	1
NOR5	2	-	-
NOR5B1	2	-	-
NOR5B2	2	-	-
NOR5B3	2	-	-
NOR5B4	2	-	-
NOR5B5	2	-	-
NOR6	2	2	1
NOR7	2	2	1
NOR8	3	2	1
NOR9	3	2	1
OR5	2	-	-
OR5B1	2	-	-
OR5B2	2	-	-
OR5B3	2	-	-
OR5B4	2	-	-
OR5B5	2	-	-
OR6	2	2	1
OR7	2	2	1
OR8	3	2	1
OR9	3	2	1
RAM16X2	-	-	1
RAM16X4	-	-	2
RAM16X8	-	-	4
RAM32X2	-	-	2
RAM32X4	-	-	4

Element Name	XC2000	XC3000	XC4000/ 4000E
RAM32X8	-	-	8
SOP3	1	1	1
SOP3B1A	1	1	1
SOP3B1B	1	1	1
SOP3B2A	1	1	1
SOP3B2B	1	1	1
SOP3B3	1	1	1
SOP4	1	1	1
SOP4B1	1	1	1
SOP4B2A	1	1	1
SOP4B2B	1	1	1
SOP4B3	1	1	1
SOP4B4	1	1	1
SR4CE	4	2	2
SR4CLE	8	3	3
SR4CLED	11	5	5
SR4RE	4	2	2
SR4RLE	8	6	5
SR4RLED	12	7	7
SR8CE	8	4	4
SR8CLE	16	5	5
SR8CLED	21	9	10
SR8RE	8	4	4
SR8RLE	16	12	9
SR8RLED	24	13	18
SR16CE	16	8	16
SR16CLE	32	9	9
SR16CLED	41	17	17
SR16RE	16	8	8
SR16RLE	32	24	17
SR16RLED	48	25	25

Element Name	XC2000	XC3000	XC4000/ 4000E
XNOR5	2	-	-
XNOR6	2	2	1
XNOR7	2	2	1
XNOR8	3	2	1
XNOR9	3	2	1
XOR5	2	-	-
XOR6	2	2	1
XOR7	2	2	1
XOR8	3	2	1
XOR9	3	2	1
X74_42	10	5	5
X74_L85	17	14	11
X74_138	9	5	5
X74_139	2	2	2
X74_147	13	8	5
X74_148	15	10	6
X74_150	13	12	5
X74_151	8	5	3
X74_152	6	5	3
X74_153	6	6	2
X74_154	18	17	16
X74_157	4	4	2
X74_158	4	4	2
X74_160	10	9	6
X74_161	11	9	6
X74_162	10	8	8
X74_163	13	9	8
X74_164	8	5	4
X74_165S	16	5	9
X74_168	18	9	7
X74_174	6	4	3

Element Name	XC2000	XC3000	XC4000/ 4000E
X74_194	9	9	5
X74_195	5	4	3
X74_273	8	5	4
X74_280	4	3	3
X74_283	4	4	8
X74_298	4	4	2
X74_352	6	6	2
X74_377	8	5	4
X74_390	4	3	3
X74_518	11	9	3
X74_521	11	9	3

Relationally Placed Modules

This section lists the RPMs by family. RPMs are "soft" macros that contain relative location constraint (RLOC) information. Only non-carry logic (CY4_*) RPMs are listed. See the *Libraries Guide* "Attributes, Constraints, and Carry Logic" chapter for more information on XC4000 carry logic and RPMs.

The "RPMs by Architecture" table lists non-carry logic RPMs by architecture for easy identification.

Table 2-2 RPMs by Architecture

Element Name	XC4000/4000E	XC5000
ACC4	✓	✓
ACC8	✓	✓
ACC16	✓	✓
ADD4	✓	✓
ADD8	✓	✓
ADD16	✓	✓
ADSU4	✓	✓

Element Name	XC4000/4000E	XC5000
ADSU8	✓	✓
ADSU16	✓	✓
AND8		✓
AND9		✓
AND12		✓
AND16		✓
CC8CE	✓	✓
CC8CLE	✓	✓
CC8CLED	✓	✓
CC8RE	✓	✓
CC16CE	✓	✓
CC16CLE	✓	✓
CC16CLED	✓	✓
CC16RE	✓	✓
COMPMC8	✓	✓
COMPMC16	✓	✓
CY_INIT		✓
CY_MUX		✓
DECODE4		✓
DECODE8		✓
DECODE16		✓
DECODE32		✓
DECODE64		✓
DEC_CC4		✓
DEC_CC8		✓
DEC_CC16		✓
NAND8		✓
NAND9		✓
NAND12		✓

Element Name	XC4000/4000E	XC5000
NAND16		✓
NOR8		✓
NOR9		✓
NOR12		✓
NOR16		✓
OR12		✓
OR16		✓

Functional Categories

The tables in this section briefly describe and list the XC4000E and 5200 design element functions by category. Elements are listed in alphanumeric order according to architecture in each applicable architecture column. N/A means the element does not exist in that particular architecture.

Note: Only new design elements are listed. Refer to the "Selection Guide" chapter of the *Libraries Guide* for functional listings of the design elements of existing architectures.

Arithmetic Functions

There are three types of arithmetic functions: accumulators (ACC), adders (ADD), and adder/subtracters (ADSU). With an ADSU, either unsigned binary or twos-complement operations cause an overflow. If the result crosses the overflow boundary, an overflow is generated. Similarly, when the result crosses the carry-out boundary, a carry-out is generated.

XC4000E	XC5200	Description
N/A	CY_MUX	2-to-1 multiplexer for carry logic
N/A	CY_INIT	Initialization stage for carry chain

Decoders

Decoder names indicate the number of inputs and outputs and if an enable is available. Decoders with an enable can be used as

multiplexers. XC4000E decoders are edge decoders or open-drain wired-AND gates. XC5200 decoders are implemented by cascading CY_MUX elements driven from lookup tables (LUTs).

XC4000E	XC5200	Description
DECODE4, DECODE8, DECODE16	DECODE4, DECODE8, DECODE16	4-, 8-, 16-, and 32-bit active-Low decoders
N/A	DECODE32, DECODE64	32- and 64-bit active-Low decoders
N/A	DEC_CC4, DEC_CC8, and DEC_CC16	4-, 8-, and 16-bit active-Low decoders

General

General elements include FPGA configuration functions, oscillators, boundary scan logic, and other functions not classified in other sections.

XC4000E	XC5200	Description
N/A	BSCAN	Boundary scan logic control circuit
N/A	CK_DIV	Internal multiple-frequency clock divider
N/A	CY_INIT	Initialization stage for carry chain
N/A	OSC5	Internal multiple-frequency clock-signal generator
STARTUP	STARTUP	User interface to global clock, reset, and tristate controls

Input/Output Flip-Flops

Input/output flip-flops are configured in IOBs. They include flip-flops whose outputs are enabled by tristate buffers, flip-flops that can be set upon global set/reset rather than reset, and flip-flops with inverted clock inputs.

XC4000E	XC5200	Description
IFDX, IFDX4, IFDX8, and IFDX16	N/A	Single- and multiple-input D flip-flops
IFDX_1	N/A/	Input D flip-flop with inverted clock
IFDXI	N/A/	Input D flip-flop (asynchronous set)
IFDXI_1	N/A	D flip-flop with inverted clock (asynchronous set)
OFDEX, OFDEX4, OFDEX8, and OFDEX16	N/A	D flip-flops with active-High enable output buffers
OFDEX_1	N/A	D flip-flop with active-High enable output buffer and inverted clock
OFDEXI	N/A	D flip-flop with active-High enable output buffer (asynchronous set)
OFDEXI_1	N/A	D flip-flop with active-High enable output buffer and inverted clock (asynchronous set)
OFDTX, OFDTX4, OFDTX8, and OFDTX16	N/A	Single and multiple D flip-flops with active-High tristate and active-Low output enable buffers
OFDTX_1	N/A	D flip-flop with active-High tristate and active-Low output buffer and inverted clock
OFDTXI	N/A	D flip-flop with active-High tristate and active-Low output buffer (asynchronous set)

XC4000E	XC5200	Description
OFDTXI_1	N/A	D flip-flop with active-High tristate, active-Low output buffer and inverted clock
OFDX, OFDX4, OFDX8, and OFDX16	N/A	Single- and multiple-output D flip-flops
OFDX_1	N/A	Output D flip-flop with inverted clock
OFDXI	N/A	Output D flip-flop (asynchronous set)
OFDXI_1	N/A	Output D flip-flop with inverted clock (asynchronous set)

Input Latches

Single and multiple input latches can hold transient data entering a chip.

XC4000E	XC5200	Description
ILDX, ILDX4, ILDX8, and ILDX16	N/A	Input transparent data latches
ILDX_1	N/A	Transparent input data latch with inverted gate
ILDXI	N/A	Input transparent data latch (asynchronous set)
ILDXI_1	N/A	Transparent input data latch with inverted gate (asynchronous set)

Latches

Latches are two-state buffers fed by two inputs: D and L. When the L input is Low, it acts as a transparent input; in this case, the latch acts

as a buffer and outputs the value input by D. When the L input is High, it ignores the D input value.

XC4000E	XC5200	Description
N/A	LDCE	Transparent data latch with asynchronous clear and gate enable
N/A	LDCE_1	Transparent data latch with asynchronous clear, gate enable, and inverted gate input
N/A	LD4CE, LD8CE, and LD16CE	Transparent data latches with asynchronous clear and clock enable

Logic Primitives

New combinatorial logic gates that implement the basic Boolean functions are available in the XC5200 architecture.

XC4000E	XC5200	Description
N/A	AND12, AND16	2- to 9-input AND gates with inverted and non-inverted inputs
N/A	NAND12, NAND16	2- to 9-input NAND gates with inverted and non-inverted inputs
N/A	NOR12, NOR16	2- to 9-input NOR gates with inverted and non-inverted inputs
N/A	OR12, OR16	2- to 9-input OR gates with inverted and non-inverted inputs

Map Elements

Map elements are used in conjunction with logic symbols to constrain the logic to particular CLBs or particular F or H function generators.

XC4000E	XC5200	Description
N/A	F5MAP	5-input function partitioning control symbol

Memory Elements

The XC4000/4000E architecture has a number of static-RAM configurations defined as macros. These 16- or 32-word RAMs are 1, 2, 4, and 8 bits wide.

XC4000E	XC5200	Description
RAM16X1D	N/A	16-deep by 1-wide static dual port synchronous RAM
RAM16X2D	N/A	16-deep by 2-wide static dual port synchronous RAM
RAM16X4D	N/A	16-deep by 4-wide static dual port synchronous RAM
RAM16X8D	N/A	16-deep by 8-wide static dual port synchronous RAM
RAM16X1S	N/A	16-deep by 1-wide static synchronous RAM
RAM16X2S	N/A	16-deep by 2-wide static synchronous RAM
RAM16X4S	N/A	16-deep by 4-wide static synchronous RAM
RAM16X8S	N/A	16-deep by 8-wide static synchronous RAM
RAM32X1S	N/A	32-deep by 1-wide static synchronous RAM
RAM32X2S	N/A	32-deep by 2-wide static synchronous RAM
RAM32X4S	N/A	32-deep by 4-wide static synchronous RAM
RAM32X8S	N/A	32-deep by 8-wide static synchronous RAM

Multiplexers

Reprogrammable routing control. This component selects one input wire as output from a selection of wires.

XC4000E	XC5200	Description
N/A	CY_MUX	2-to-1 multiplexer for carry logic
N/A	F5_MUX	2-to-1 lookup table multiplexer

XC5200 Constraints and Attributes

Attributes are instructions placed on symbols or nets in an FPGA or EPLD schematic to indicate their placement, implementation, naming, directionality, and so forth. Constraints are a type, or subset, of attributes that are only used to indicate where an element should be placed.

The constraints and attributes described in this section are specific to the XC5200 architecture. XC5200 does support the constraints and attributes supported by the XC4000/4000E architectures which are described in detail in the "Attributes, Constraints, and Carry Logic" chapter of the *Libraries Guide*.

These are the XC5200-specific attributes and constraints.

- DIVIDE1_BY
- DIVIDE2_BY

DIVIDE1_BY and DIVIDE2_BY are new attributes.

- NODELAY
- RLOC

NODELAY and RLOC are existing attributes that have been modified to support XC5200.

DIVIDE1_BY and DIVIDE2_BY

DIVIDE1_BY=*value* and DIVIDE2_BY=*value* attributes are user-defined parameters added to the schematic for the OSC5 and CK_DIV symbols. These attributes have the following syntax.

```
DIVIDE1_BY={4|16|64|256}
```

DIVIDE2_BY={2|8|32|128|1024|4096|16384|65536}

For the OSC5 symbol, these attributes define the amount by which the internal 16-MHz clock is to be divided for the OSC1 and/or OSC2 outputs. The DIVIDE1_BY attribute applies to the OSC1 output and the DIVIDE2_BY attribute applies to the OSC2 output.

For the CK_DIV symbol, the attributes define the amount by which the user-specified clock input (C) is to be divided.

NODELAY

The default configuration of input buffers that directly source flip-flops and data latches includes an input delay that results in no external hold time on the input data path. However, this delay can be removed by placing the NODELAY attribute on input buffers (IBUFs), resulting in a smaller setup time but a positive hold time. This is the syntax of the NODELAY attribute.

NODELAY

RLOC

RLOC=*value* is a parameter added to schematic symbols to control relative placement of the elements contained in the schematic. This is the RLOC parameter syntax.

RLOC=R*row#*C*column#*[.*extension*]

The row and column numbers of the LCA grid array can be any positive integer or zero.

The optional *.extension* further denotes positioning of FMAPs, flip-flops, latches, and CY_MUX symbols within the appropriate logic cell of the CLB. Its value can be LC0, LC1, LC2, or LC3.

The RLOC value cannot specify a range or a list of several locations; it must specify a single location.

For more details on the RLOC constraints, refer to the *Libraries Guide*.

Chapter 3

New Design Elements (XC4000E and XC5200)

This chapter contains design elements for the XC4000E and XC5200 architectures. The elements are organized in alphanumeric order, with all numeric suffixes in ascending order. A graphic symbol; functional description; primitive versus macro table; truth table (when applicable); and schematics for each implementation, generally the 8-bit version, are included for each design element.

The XC4000E architecture is a superset of the XC4000 architecture. The design elements in this section are variations of those included in the XC4000 architecture but can be used with them.

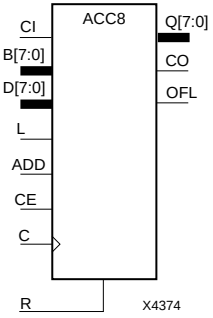
Note: Some of the design elements in this chapter are also in the *Libraries Guide*; they are repeated in this supplement to show how those elements are implemented for the XC5200 architecture.

ACC8

8-Bit Loadable Cascadable Accumulator with Carry-In, Carry-Out, and Synchronous Reset

XC3000	XC4000	XC4000E	XC5200	XC7000[a]
Macro	Macro	Macro	Macro	Macro

a. not supported for XC7272 or XC7336 designs



ACC8 can add or subtract an 8-bit unsigned-binary or twos-complement word to or from the contents of an 8-bit data register and store the results in the register. The register can be loaded with an 8-bit word.

In the XC4000/4000E family, the accumulator is implemented using carry logic and relative location constraints to ensure efficient placement of logic. The synchronous reset (R) has priority over all other inputs, and when High, causes all outputs to go to logic level zero. Clock (C) transitions are ignored when clock enable (CE) is Low.

The accumulator is asynchronously reset, with Low outputs, when power is applied or when global reset (GR) for XC3000 and 5200 or global set/reset (GSR) for XC4000/4000E is active. GR is active Low; the GSR active level is programmable.

Load

When the load input (L) is High, CE is ignored and the data on inputs D7 – D0 is loaded into the 8-bit register.

Unsigned Binary Versus Twos-Complement

ACC8 can operate on either 8-bit unsigned binary numbers or 8-bit twos-complement numbers. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as twos complement, the output can be interpreted as twos complement. The only functional difference between an unsigned binary operation and a twos-complement operation is how they determine when “overflow” (OFL) occurs. Unsigned binary uses carry-out (CO) to determine when “overflow” occurs, while twos complement uses OFL.

For the XC7000 EPLD architecture, the CO output is not valid during load (L=High), during reset (R=High), or while CE is inactive (Low). Also, the CI and CO pins are not implemented using the EPLD arithmetic carry path and should be used to cascade accumulators. Refer to "ACC8X1" and "ACC8X2" for descriptions of cascadable EPLD accumulators. The OFL output is not provided on the ACC8 symbol in XC7000.

Unsigned Binary Operation

For unsigned binary operation, ACC8 can represent numbers between 0 and 255, inclusive. In add mode, CO is active (High) when the sum exceeds the bounds of the adder/subtracter. In subtract mode, CO is an active-Low borrow-out and goes Low when the difference exceeds the bounds. The (CO) is not registered synchronously with the data outputs. CO always reflects the accumulation of inputs B7 – B0 and the contents of the register, which allows cascading of ACC8s by connecting CO of one stage to CI of the next stage. An unsigned binary "overflow" that is always active-High can be generated by gating the ADD signal and CO as follows.

```
unsigned overflow = CO XOR ADD
```

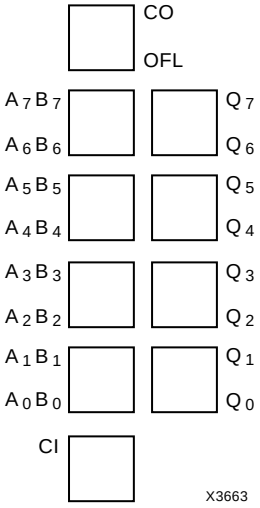
OFL should be ignored in unsigned binary operation.

Twos-Complement Operation

For twos-complement operation, ACC8 can represent numbers between -128 and +127, inclusive. If an addition or subtraction operation result exceeds this range, the OFL output goes High. The overflow is not registered synchronously with the data outputs. OFL always reflects the accumulation of inputs B7 – B0 and the contents of the register, which allows cascading of ACC8s by connecting OFL of one stage to CI of the next stage.

CO should be ignored in twos-complement operation.

XC4000/4000E Topology



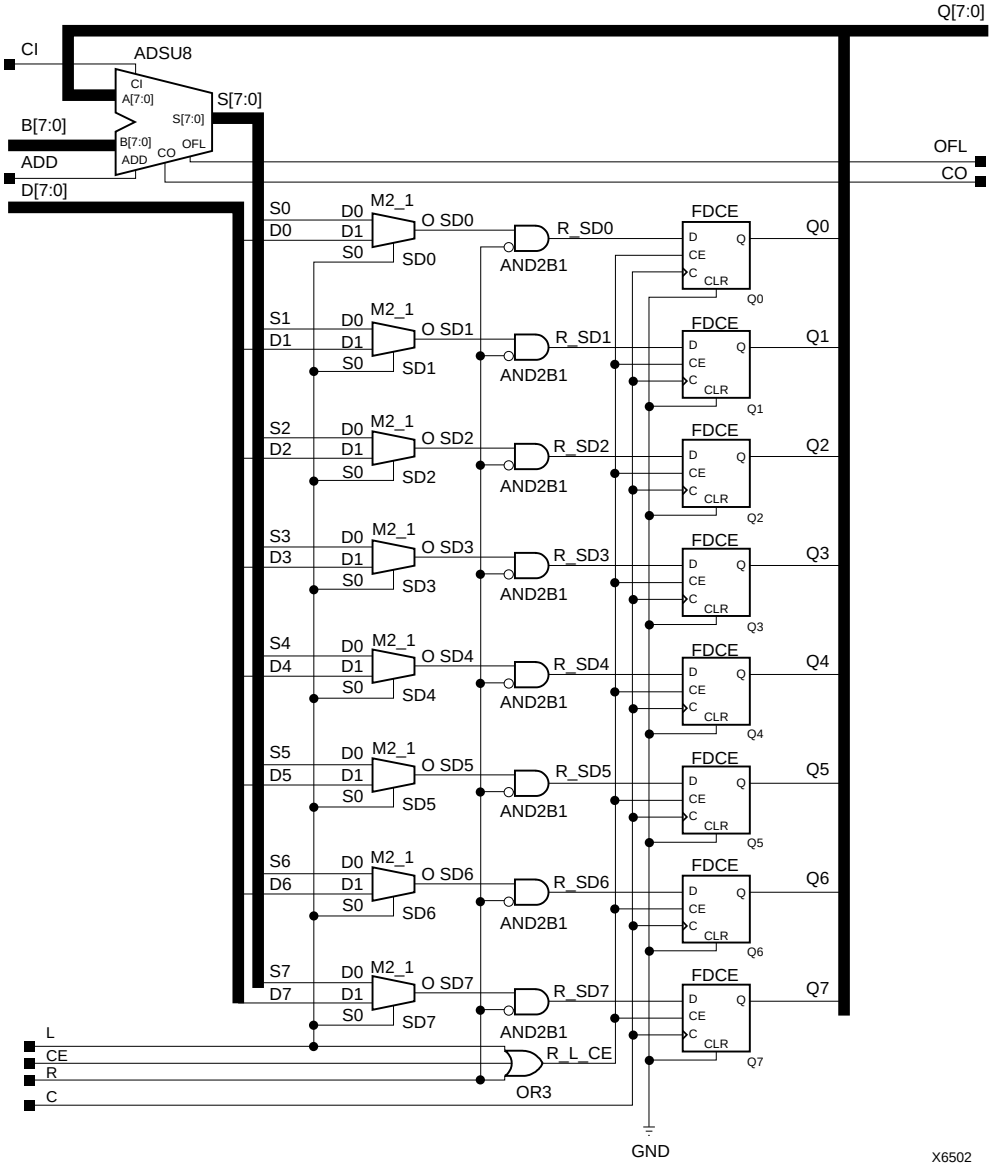


Figure 3-1 ACC8 XC3000 Implementation

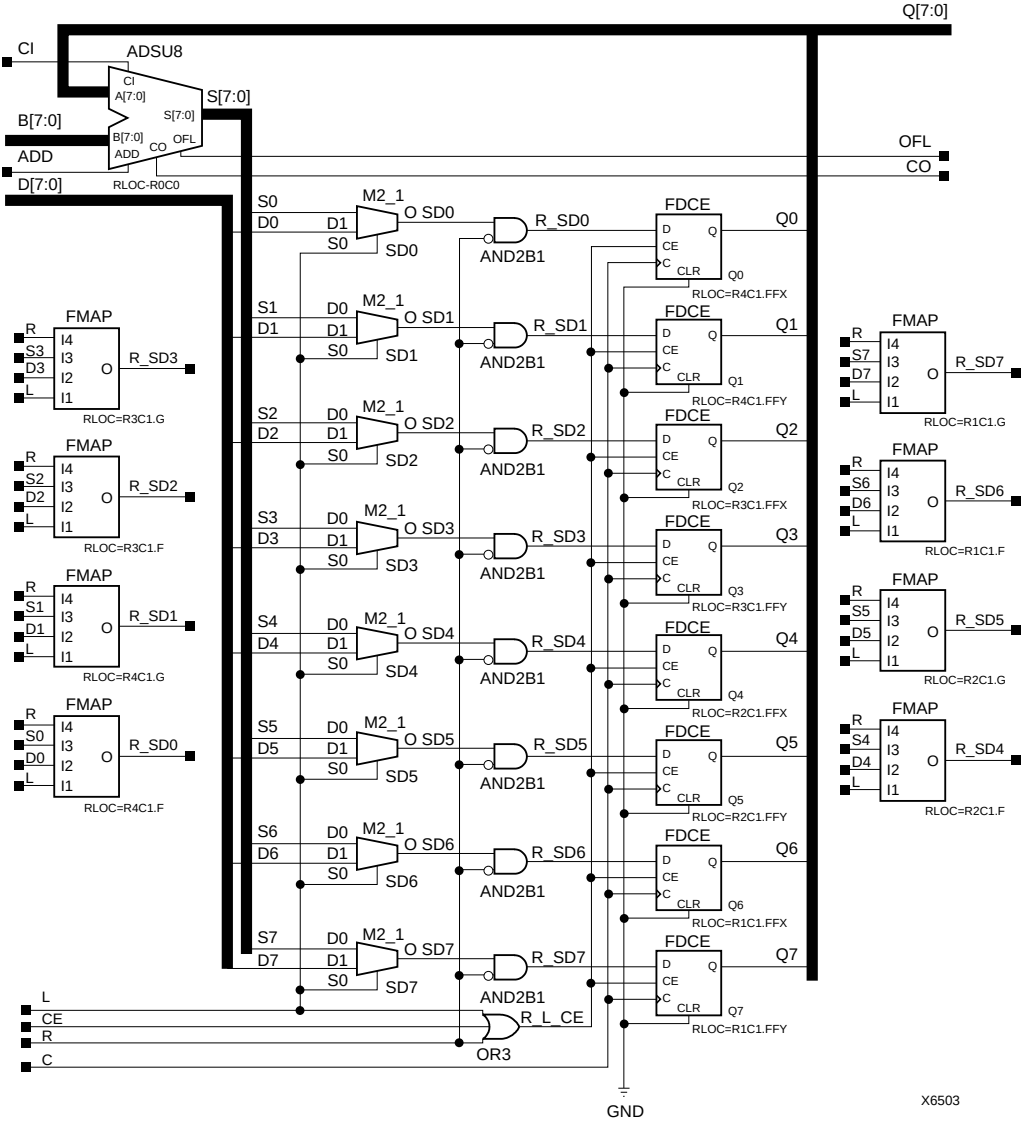


Figure 3-2 ACC8 XC4000/4000E Implementation

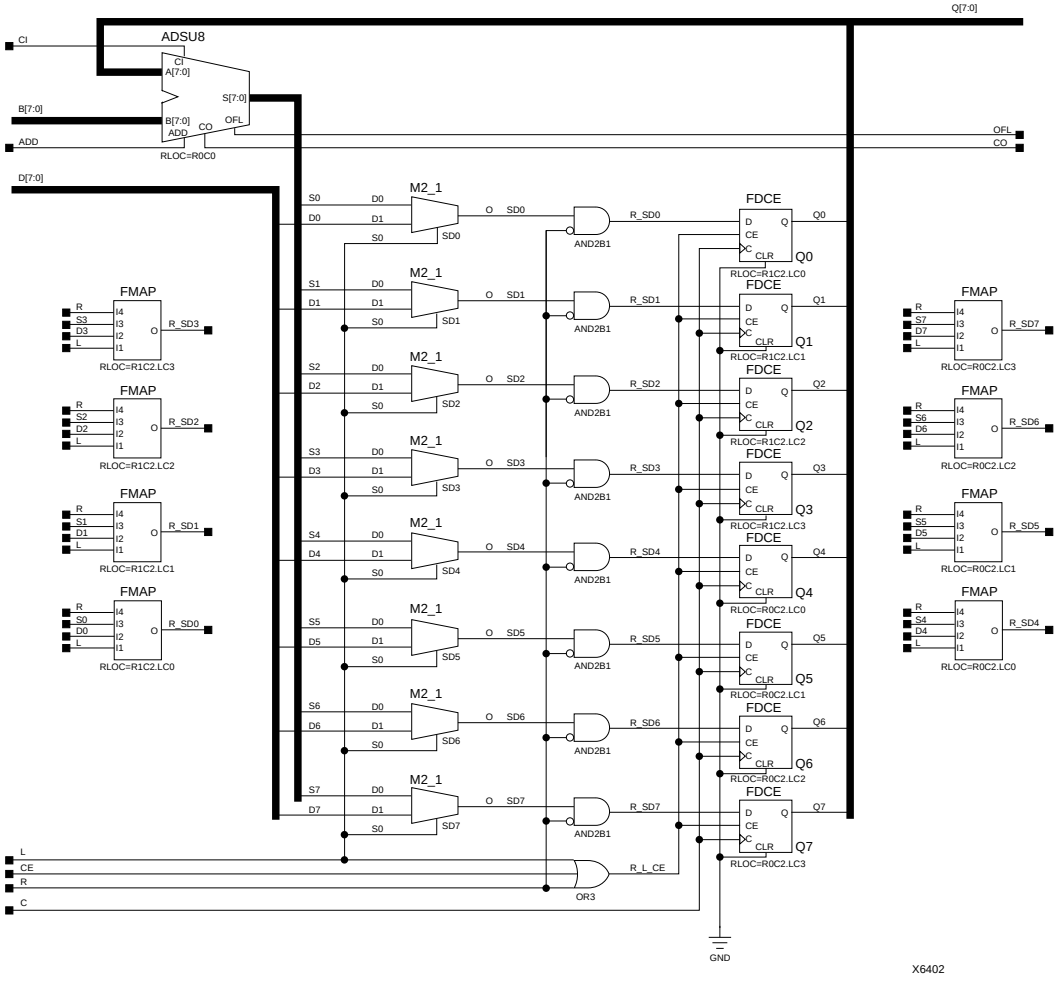


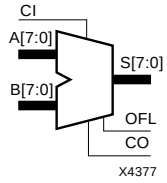
Figure 3-3 ACC8 XC5200 Implementation

ADD8

8-Bit Cascadable Full Adder with Carry-In, Carry-Out, and Overflow

XC3000	XC4000	XC4000E	XC5200	XC7000[a]
Macro	Macro	Macro	Macro	Macro

a. not supported for XC7336 designs



ADD8 is implemented in the XC4000/4000E family using carry logic and relative location constraints to ensure efficient placement of logic. ADD8 adds two words (A7 – A0 and B7 – B0) and a carry-in (CI), producing a sum output (S7 – S0) and carry-out (CO) or overflow (OFL). For XC7000 cascadable adders, refer to the "ADD8X1" and "ADD8X2" descriptions in the *Libraries Guide*. The ADD8 CI and CO pins do not use the EPLD carry chain.

Unsigned Binary Versus Twos Complement

ADD8 can operate on either 8-bit unsigned binary numbers or 8-bit twos-complement numbers. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as twos complement, the output can be interpreted as twos complement. The only functional difference between an unsigned binary operation and a twos-complement operation is how they determine when "overflow" occurs. Unsigned binary uses CO, while twos complement uses OFL to determine when "overflow" occurs.

Unsigned Binary Operation

For unsigned binary operation, ADD8 can represent numbers between 0 and 255, inclusive. CO is active (High) when the sum exceeds the bounds of the adder.

An unsigned binary "overflow" that is always active-High can be generated by gating the ADD signal and CO as follows.

```
unsigned overflow = CO XOR ADD
```

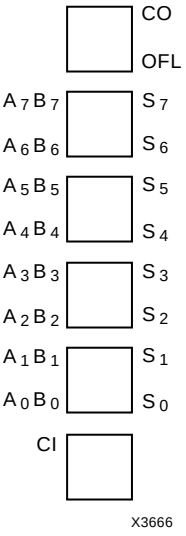
OFL is ignored in unsigned binary operation.

Twos-Complement Operation

For twos-complement operation, ADD8 can represent numbers between -128 and +127, inclusive. OFL is active (High) when the sum exceeds the bounds of the adder.

CO is ignored in twos-complement operation.

XC4000/4000E Topology



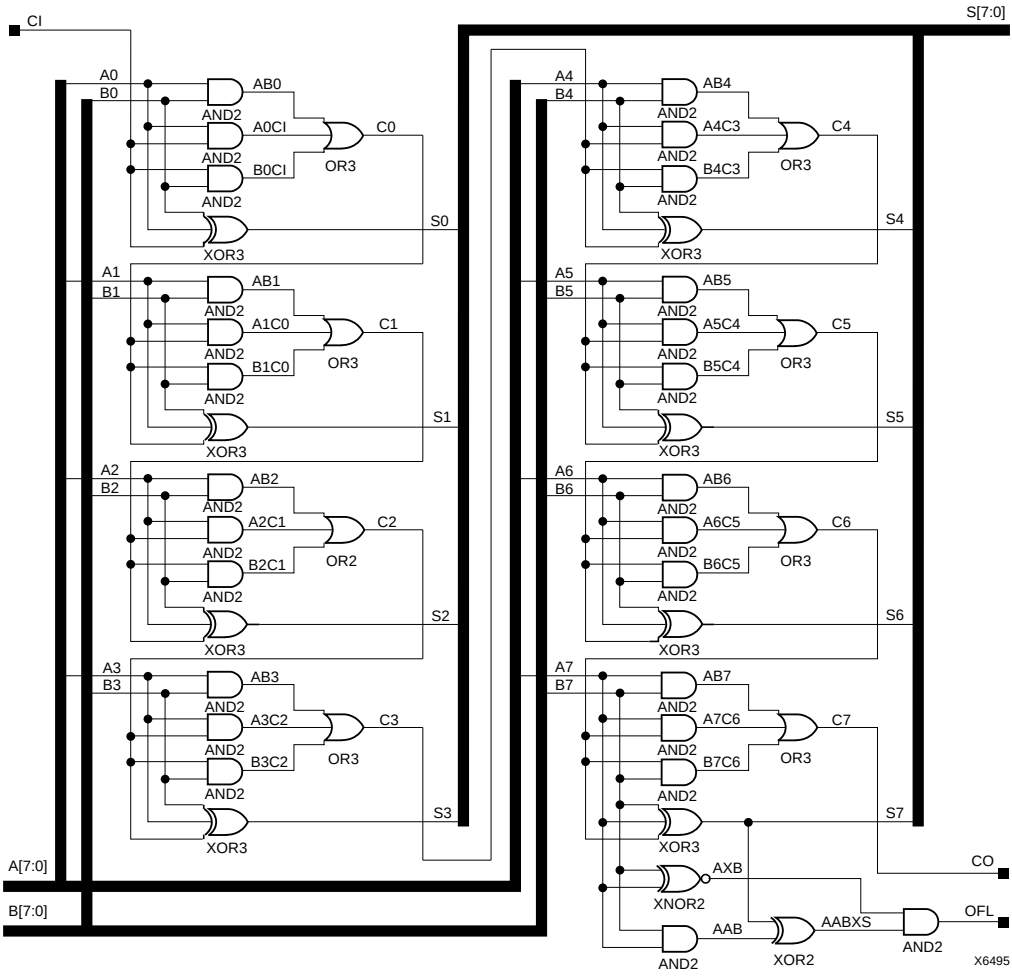


Figure 3-4 ADD8 XC3000 Implementation

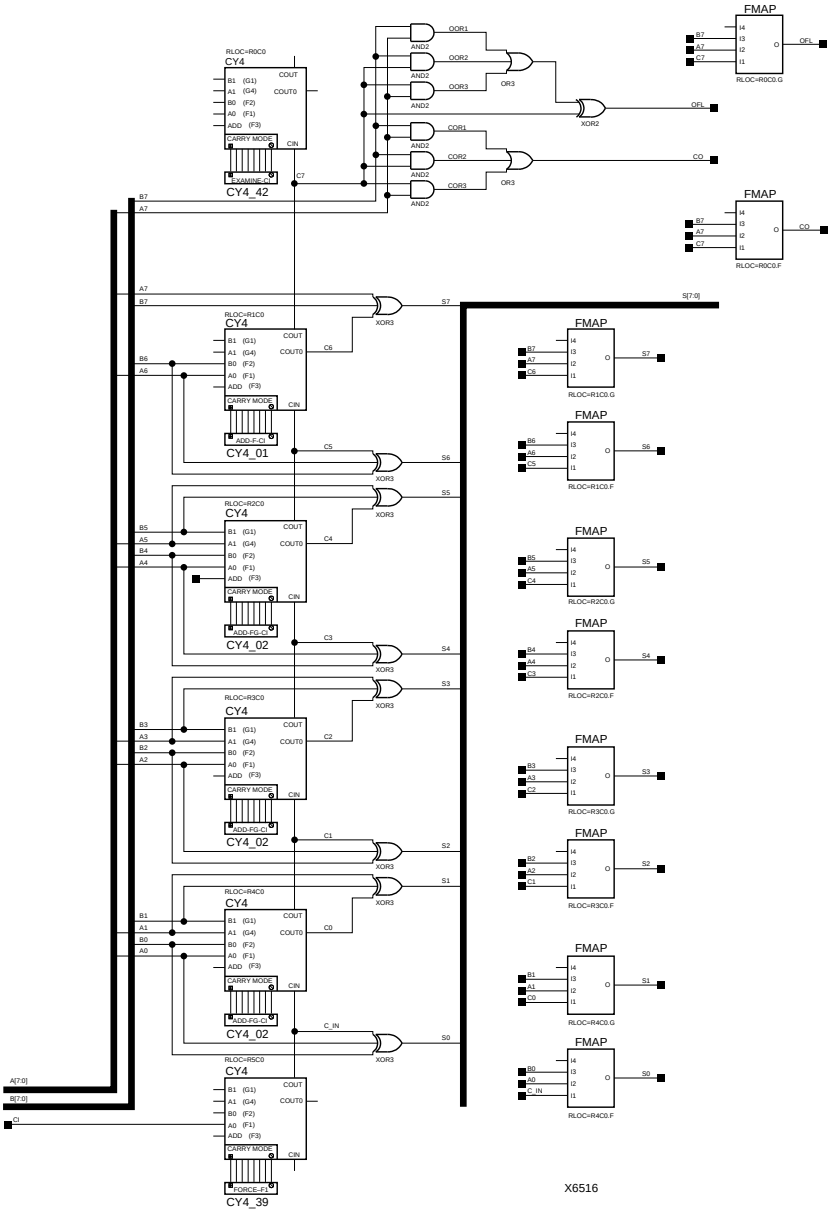


Figure 3-5 ADD8 XC4000/4000E Implementation

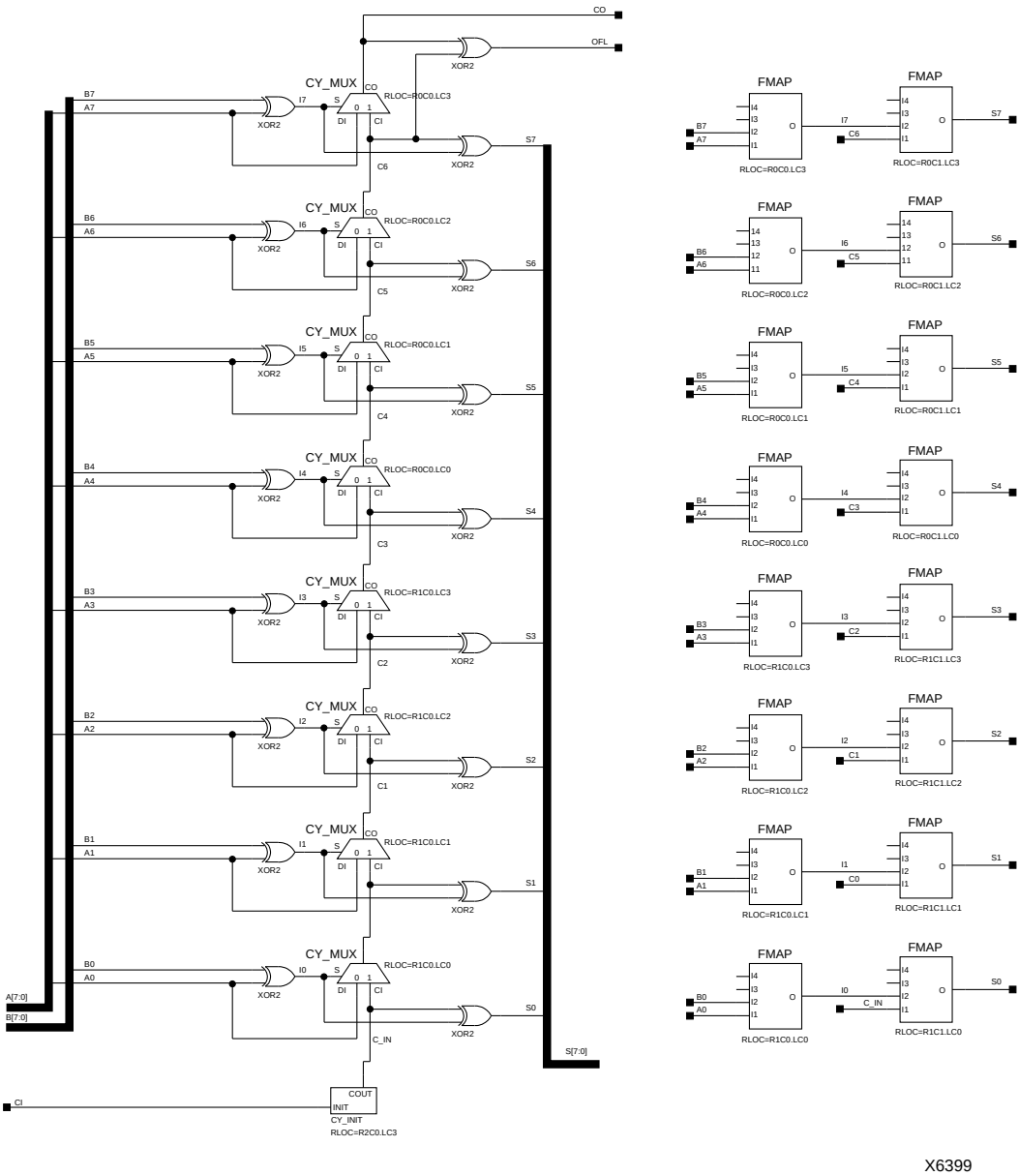


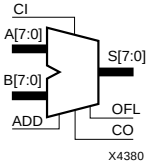
Figure 3-6 ADD8 XC5200 Implementation

ADSU8

8-Bit Cascadable Adder/Subtracter with Carry-In, Carry-Out, and Overflow

XC3000	XC4000	XC4000E	XC5200	XC7000[a]
Macro	Macro	Macro	Macro	Macro

a. not supported for XC7336 designs



ADSU8 is implemented in the XC4000/4000E family using carry logic and relative location constraints, which assure most efficient logic placement.

When the ADD input is High, two 8-bit words (A7 – A0 and B7 – B0) are added with a carry-in (CI), producing an 8-bit sum (S7 – S0) and carry-out (CO) or overflow (OFL). When the ADD input is Low, B7 – B0 is subtracted from A7 – A0, producing an 8-bit difference (S7 – S0) and CO or OFL. In add mode, CO and CI are active-High. In subtract mode, CO and CI are active-Low. OFL is active-High in add and subtract modes. For cascadable EPLD symbols, refer to the "ADSU8X1" and "ADSU8X2" descriptions in the *Libraries Guide*. ADSU8 CI and CO pins do not use the EPLD carry chain.

Unsigned Binary Versus Twos Complement

ADSU8 can operate on either 8-bit unsigned binary numbers or 8-bit twos-complement numbers. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as twos complement, the output can be interpreted as twos complement. The only functional difference between an unsigned binary operation and a twos-complement operation is how they determine when "overflow" occurs. Unsigned binary uses CO to determine when "overflow" occurs, while twos complement uses OFL.

With adder/subtracters, either unsigned binary or twos-complement operations cause an overflow. If the result crosses the overflow boundary, an overflow is generated. Similarly, when the result crosses the carry-out boundary, a carry-out is generated.

This figure shows carry-out and overflow boundaries.

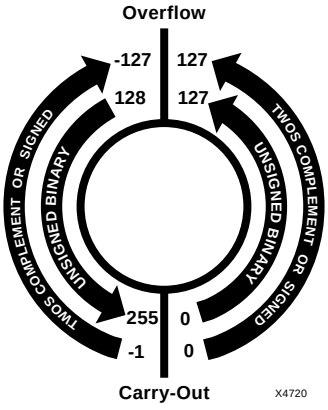


Figure 3-7 ADSU Carry-Out and Overflow Boundaries

Unsigned Binary Operation

For unsigned binary operation, ADSU8 can represent numbers between 0 and 255, inclusive. In add mode, CO is active (High) when the sum exceeds the bounds of the adder/subtracter. In subtract mode, CO is an active-Low borrow-out and goes Low when the difference exceeds the bounds.

An unsigned binary "overflow" that is always active-High can be generated by gating the ADD signal and CO as follows.

```
unsigned overflow = CO XOR ADD
```

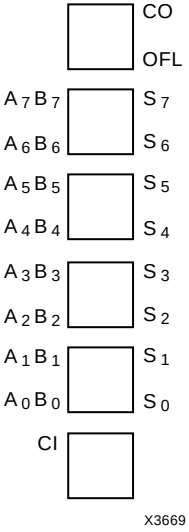
OFL is ignored in unsigned binary operation.

Twos-Complement Operation

For twos-complement operation, ADSU8 can represent numbers between -128 and +127, inclusive. If an addition or subtraction operation result exceeds this range, the OFL output goes High.

CO is ignored in twos-complement operation.

XC4000/4000E Topology



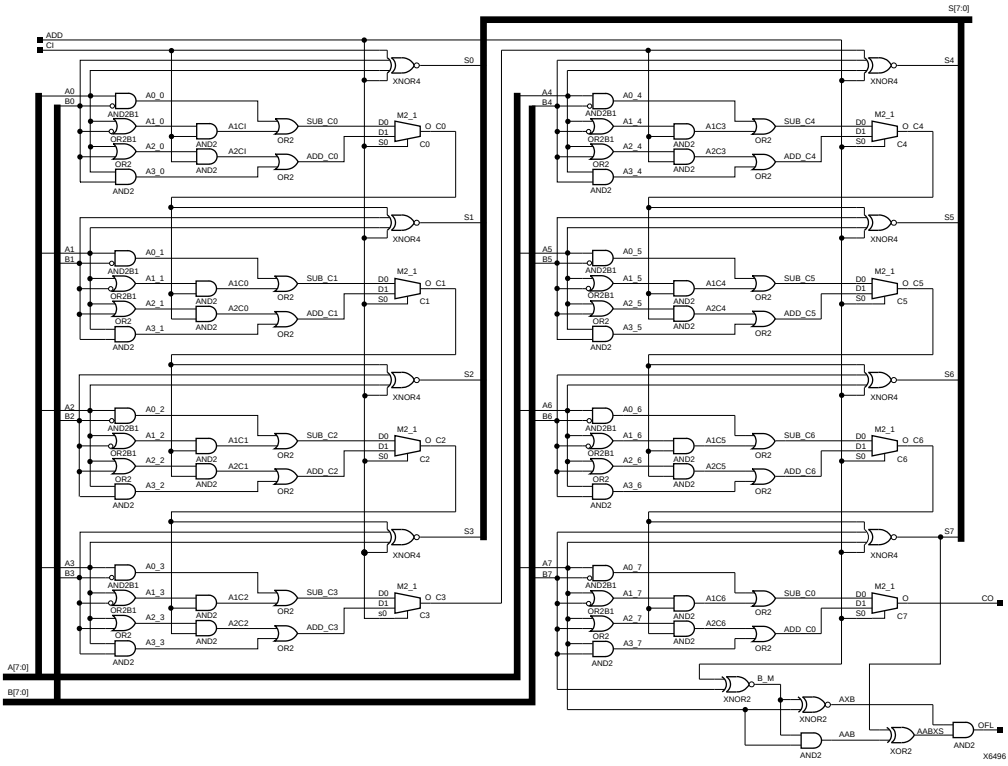


Figure 3-8 ADSU8 XC3000 Implementation

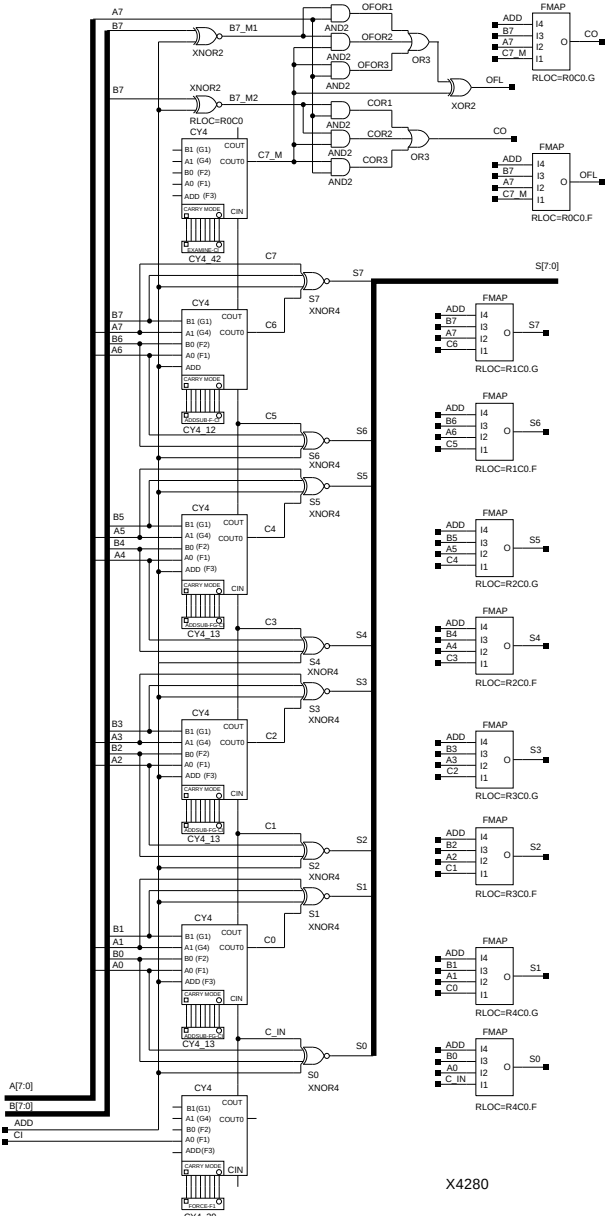


Figure 3-9 ADSU8 XC4000/4000E Implementation

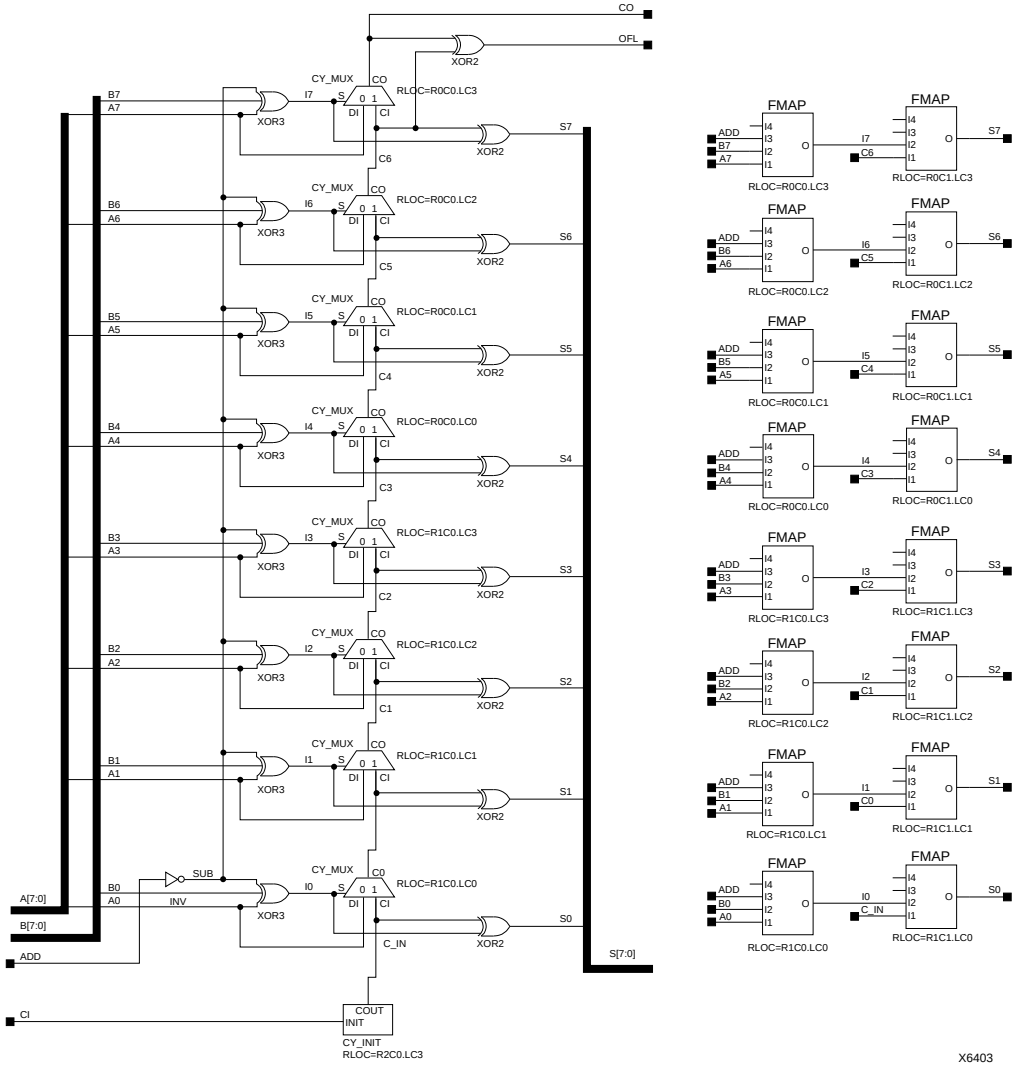


Figure 3-10 ADSU8 XC5200 Implementation

AND

2- to 9-Input AND Gates with Inverted and Non-Inverted Inputs

Element	XC2000	XC3000	XC4000	XC4000E	XC5200	XC7000
AND2, AND2B1, AND2B2, AND3B1, AND3B2, AND3B3, AND4B1, AND4B2, AND4B3, AND4B4	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
AND5, AND5B1, AND5B2, AND5B3, AND5B4, AND5B5	Macro	Primitive	Primitive	Primitive	Macro	Primitive
AND6, AND7, AND8	Macro	Macro	Macro	Macro	Macro	Primitive
AND9	Macro	Macro	Macro	Macro	Macro	Primitive
AND12, AND16	N/A	N/A	N/A	N/A	Macro	N/A

The AND function is performed in the Configurable Logic Block (CLB) function generators for XC2000, XC3000, XC4000/4000E, and XC5200 architectures.

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs are available with only non-inverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource in FPGAs, replace functions with unused inputs with functions having the appropriate number of inputs.

The 12- and 16-input AND functions are available only with non-inverting inputs. To invert some or all inputs, use external inverters.

Refer to the “Overview” chapter of the *Libraries Guide* for the combinatorial/AND gate naming convention.

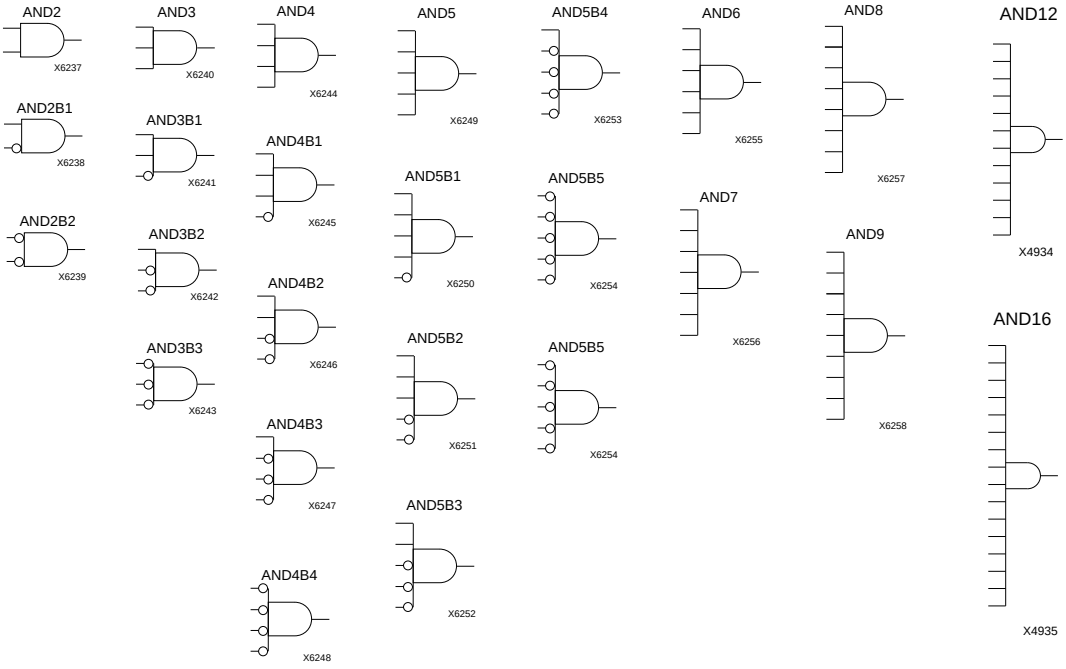


Figure 3-11 AND Gate Representations

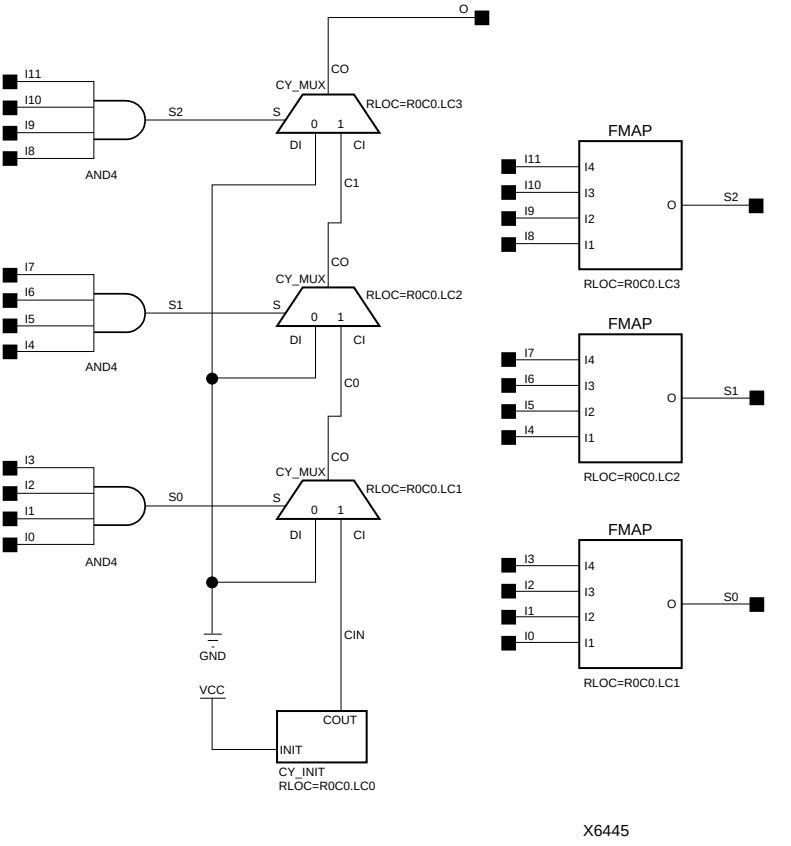


Figure 3-12 AND12 XC5200 Implementation

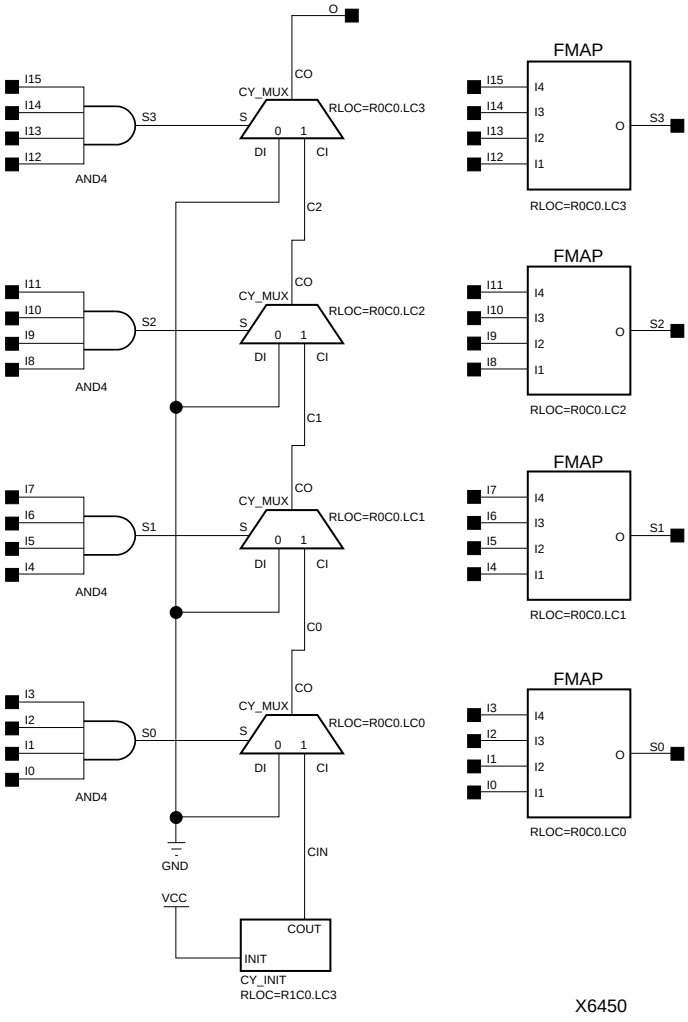
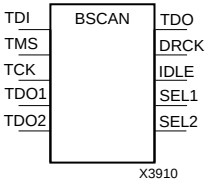


Figure 3-13 AND16 XC5200 Implementation

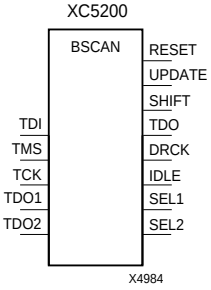
BSCAN

Boundary Scan Logic Control Circuit

XC4000, XC4000E



XC5200



XC4000	XC4000E	XC5200
Primitive	Primitive	Primitive

The BSCAN symbol indicates that boundary scan logic should be enabled after the programmable logic device (PLD) configuration is complete. It also provides optional access to some special features of the XC5200 boundary scan logic.

Note: For more information on boundary scan, refer to the application note "Boundary Scan in XC4000 Devices" in *The Programmable Logic Data Book*.

To indicate that boundary scan remains enabled after configuration, connect the BSCAN symbol to the TDI, TMS, TCK, and TDO pads shown in the "Boundary Scan XC4000/4000E Representation" illustration and the "Boundary Scan XC5200 Representation" illustration. The other pins on BSCAN do not need to be connected, unless those special functions are needed. A signal on the TDO1 input is passed to the external TDO output when the USER1 instruction is executed; the SEL1 output goes High to indicate that the USER1 instruction is active. The TDO2 and SEL2 pins perform a similar function for the USER2 instruction. The DRCK output provides access to the data register clock (generated by the TAP controller). The IDLE output provides access to a version of the TCK input, which is only active while the TAP controller is in the Run-Test-Idle state. The RESET, UPDATE, and SHIFT pins of the XC5200 BSCAN symbol represent the decoding of the corresponding state of the boundary scan internal state machine. These functions are not available in the XC4000/4000E architecture.

If boundary scan is used only before configuration is complete, do not include the BSCAN symbol in the design. The TDI, TMS, TCK, and TDO pins can be reserved for user functions.

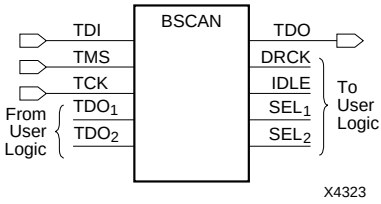


Figure 3-14 Boundary Scan XC4000/4000E Representation

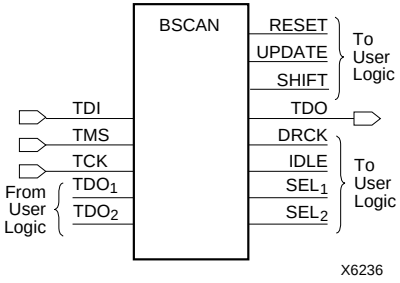
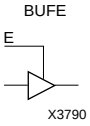


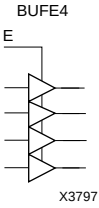
Figure 3-15 Boundary Scan XC5200 Representation

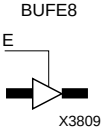
BUFE

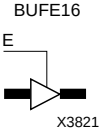
Internal Tristate Buffers

XC3000	XC4000	XC4000E	XC5200	XC7000
Macro	Macro	Macro	Macro	Primitive









BUFE, BUFE4, BUFE8, and BUFE16 are single or multiple tristate buffers with inputs I, I3 – I0, I7 – I0, and so forth; outputs O, O3 – O0, O7 – O0, and so forth; and active-High output enable (E). When E is High, data on the inputs of the buffers is transferred to the corresponding outputs. When E is Low, the output is high impedance (Z state or Off). The outputs of the buffers are connected to horizontal longlines in FPGA architectures.

The outputs of separate BUFE symbols can be tied together to form a bus or a multiplexer. Make sure that only one E is High at any one time. If none of the E inputs is active-High, a "weak-keeper" circuit (XC2000, 3000, 4000/4000E, and 5200) keeps the output bus from floating, but does not guarantee that the bus remains at the last value driven onto it.

The E signal in XC3000/4000/4000E BUFE macros is implemented by using a BUFT with an inverter on the active-Low enable (T) pin. This inverter can add an extra level of logic to the data path. Pull-up resistors can be used to establish a High logic level if all BUFE elements are Off in XC3000 and XC4000/4000E. Pull-ups cannot be used in conjunction with BUFT or BUFE macros in the XC5200 architecture, because there are no pull-ups available at the ends of the horizontal longlines. Pull-up resistors are always used for EPLD designs. This figure shows BUFE XC3000/4000/4000E implementation.

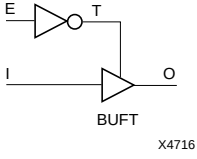


Figure 3-16 BUFE XC3000/XC4000/4000E Implementation

Inputs		Outputs
E	**I**	**O**
0	X	Z
1	1	1
1	0	0

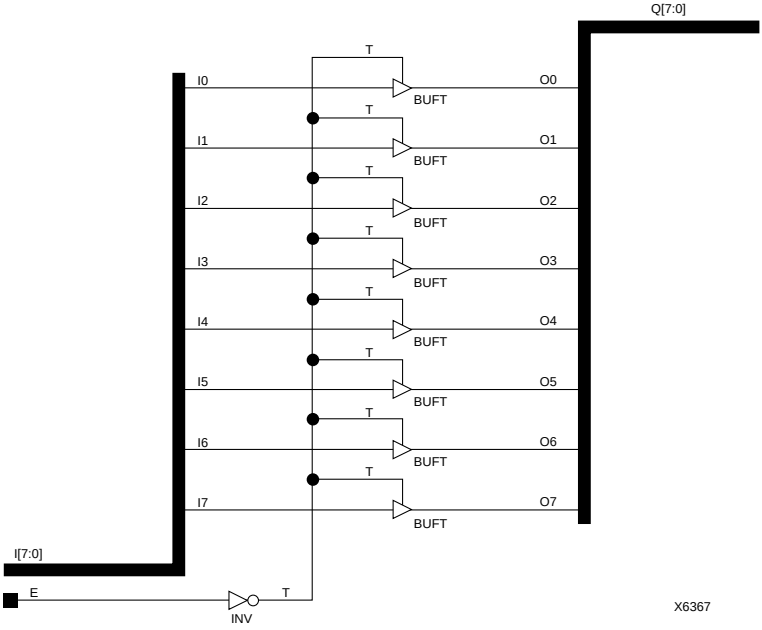
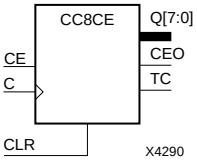


Figure 3-17 BUFE8 XC3000/4000/4000E/5200 Implementation

CC8CE

8-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear



XC4000	XC4000E	XC5200
Macro	Macro	Macro

CC8CE is an 8-stage, 8-bit, synchronous, clearable, cascadable binary counter. The counter is implemented using carry logic with relative location constraints to ensure efficient placement of logic. The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored and data (Q7 – Q0) and terminal count (TC) outputs go to logic level zero, independent of clock transitions. The outputs (Q7 – Q0) increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

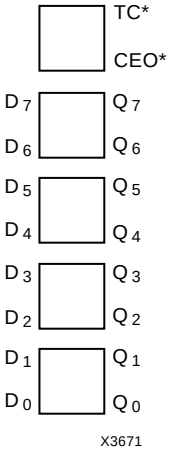
Larger counters are created by connecting the count enable out (CEO) output of the first stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than *n*(tCE-TC), where *n* is the number of stages and "tCE-TC" is the CE-to-TC propagation delay of each stage.

The counter is asynchronously reset, with Low outputs, when power is applied or when global set/reset (GSR) for XC4000/4000E or global reset (GR) for XC5200 is active. The GSR active level is programmable. When cascading counters, use the CEO output if the counter uses the CE input; otherwise, use the TC output.

Inputs			Outputs		
CLR	CE	C	Q7 – Q0	TC[a]	CEO[b]
1	X	X	0	0	0
0	0	X	No Chg	No Chg	0
0	1	↑	Inc	TC	CEO

a. TC = (Q7•Q6•Q5•Q4•...•Q0)
b. CEO = (TC•CE)

XC4000/4000E Topology[1]



1. In the process of combining the logic that loads CEO and TC, the place and route software might map the logic that generates CEO and TC to different function generators. If this mapping occurs, the CEO and TC logic cannot be placed in the uppermost CLB as indicated in the illustration.

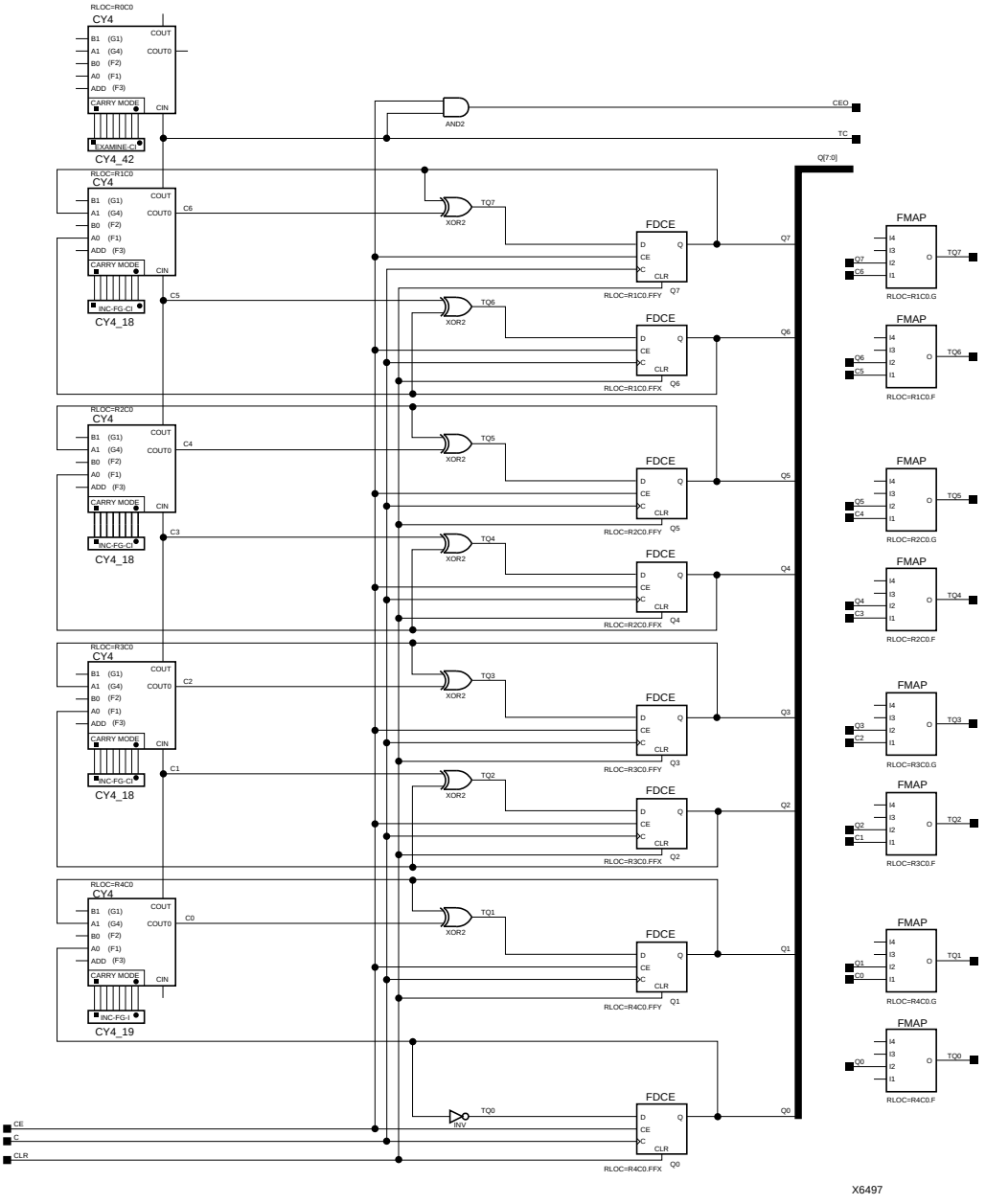


Figure 3-18 CC8CE XC4000/4000E Implementation

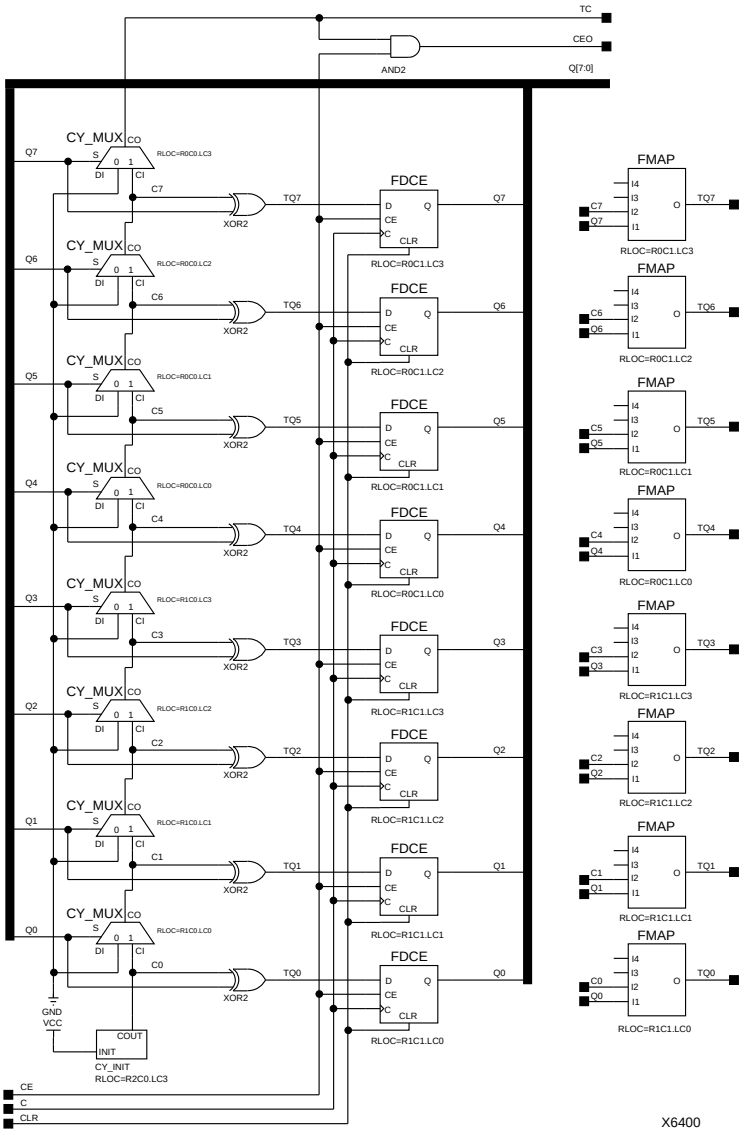
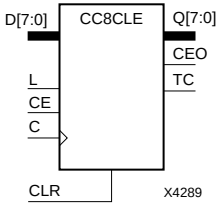


Figure 3-19 CC8CE XC5200 Implementation

CC8CLE

8-Bit Loadable Cascadable Binary Counter with Clock Enable and Asynchronous Clear



XC4000	XC4000E	XC5200
Macro	Macro	Macro

CC8CLE is an 8-stage, 8-bit, synchronous, loadable, clearable, cascadable binary counter. The counter is implemented using carry logic with relative location constraints to ensure efficient placement of logic.

The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored and data (Q7 – Q0) and terminal count (TC) outputs go to logic level zero, independent of clock transitions. The data on the D7 – D0 inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The outputs (Q7 – Q0) increment when CE is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

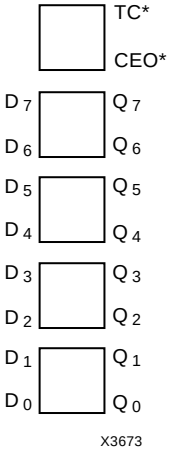
Larger counters are created by connecting the count enable out (CEO) output of the first stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n(tCE-TC), where “n” is the number of stages and “tCE-TC” is the CE-to-TC propagation delay of each stage.

The counter is asynchronously reset, with Low output, when power is applied or when global set/reset (GSR) for XC4000/4000E or global reset (GR) for XC5200 is active. The GSR active level is programmable. When cascading counters, use the CEO output if the counter uses the CE input; otherwise, use the TC output.

Inputs					Outputs		
CLR	L	CE	C	D7 – D0[a]	Q7 – Q0	TC[b]	CEO[c]
1	X	X	X	X	0	0	0
0	1	X	X	D	d7 – d0	TC	CEO
0	0	0	X	X	No Chg	No Chg	0
0	0	1	↑	X	Inc	TC	CEO

a. dn = state of referenced input one set-up time prior to active clock transition
b. TC = (Q7•Q6•Q5•Q4•...•Q0)
c. CEO = (TC•CE)

XC4000 Topology[1]



1. In the process of combining the logic that loads CEO and TC, the place and route software might map the logic that generates CEO and TC to different function generators. If this mapping occurs, the CEO and TC logic cannot be placed in the uppermost CLB as indicated in the illustration.

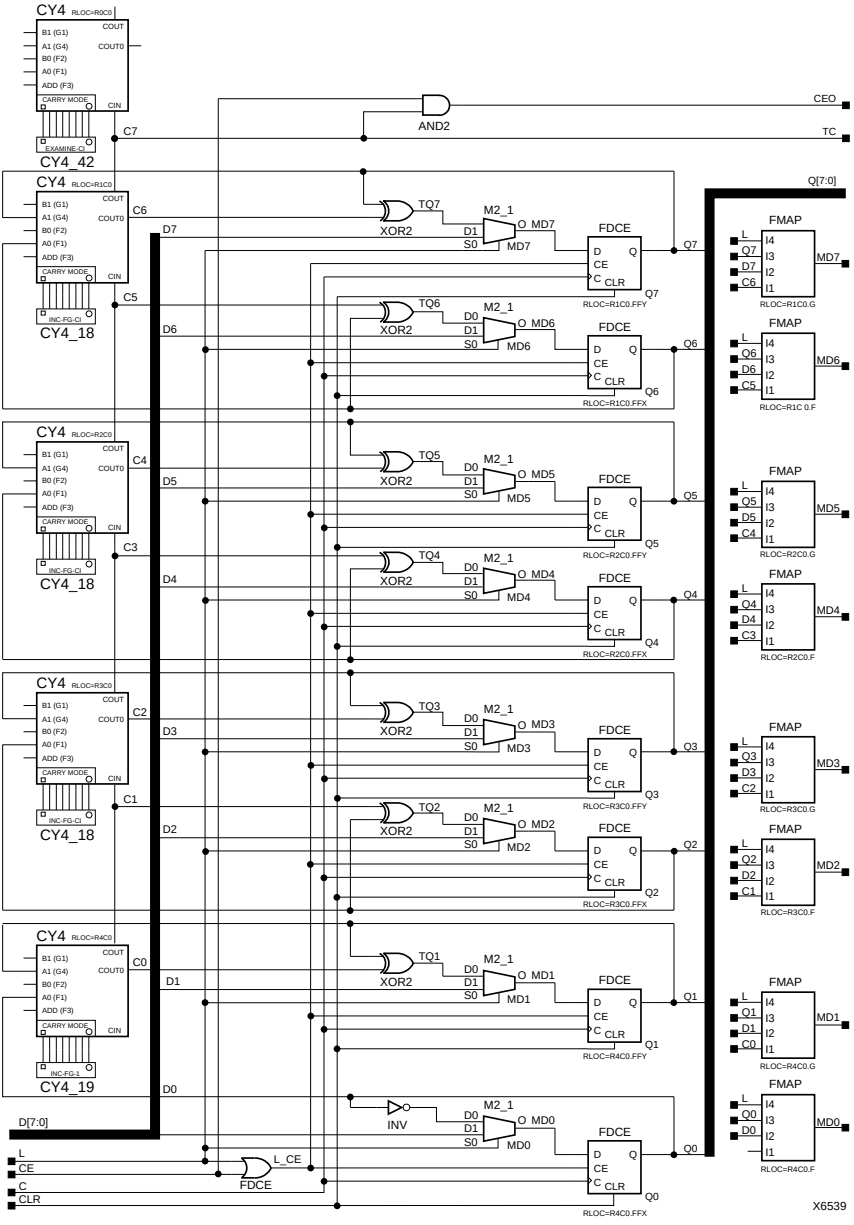


Figure 3-20 CC8CLE XC4000 Implementation

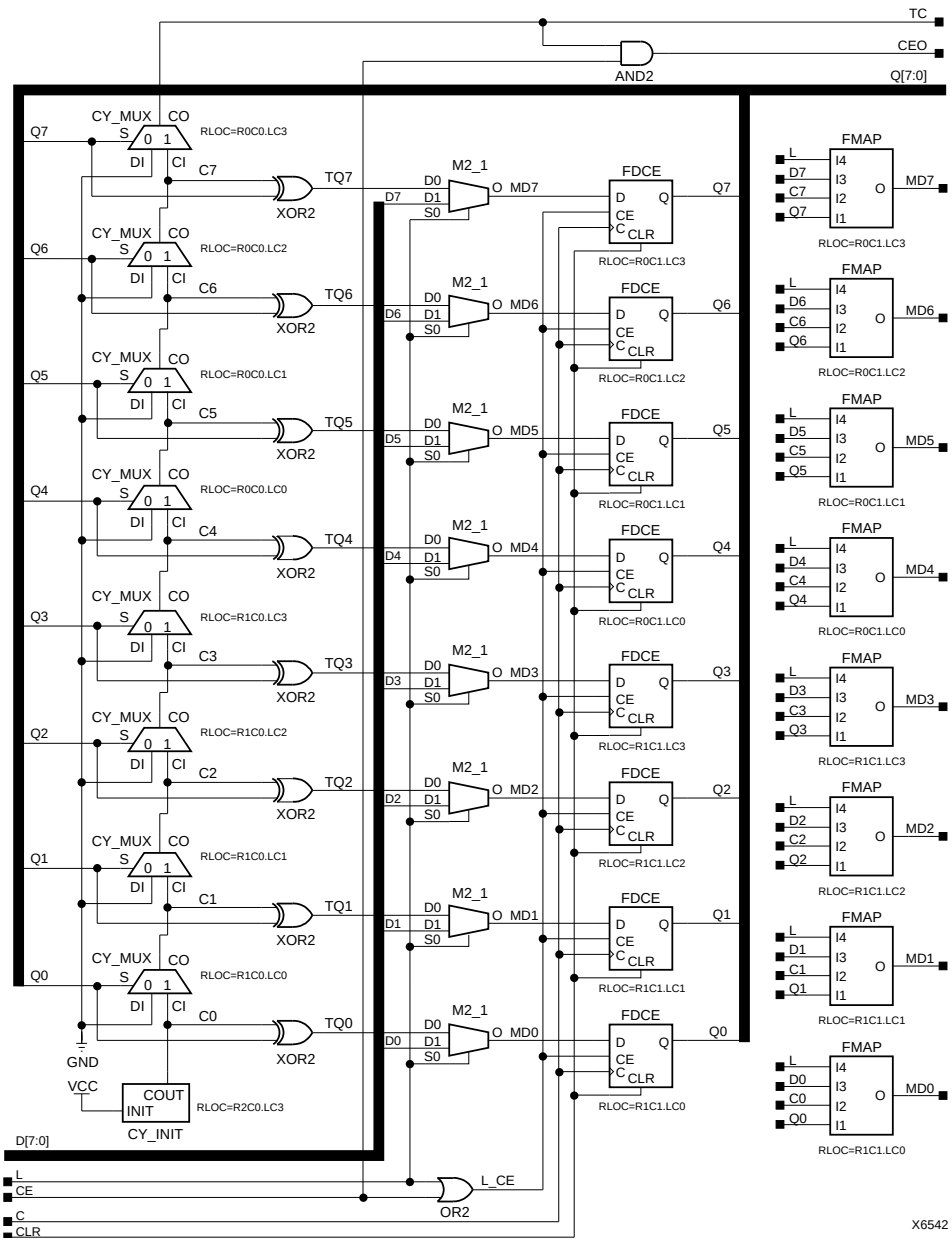
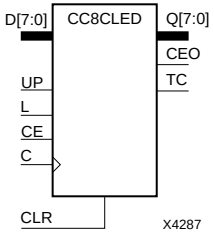


Figure 3-21 CC8CLE XC5200 Implementation

CC8CLED

8-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Asynchronous Clear



XC4000	XC4000E	XC5200
Macro	Macro	Macro

CC8CLED is an 8-stage, 8-bit, synchronous, loadable, clearable, cascadable, bidirectional binary counter. The counter is implemented using carry logic with relative location constraints to ensure efficient placement of logic.

The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored and data (Q7 – Q0) and terminal count (TC) outputs go to logic level zero, independent of clock transitions. The data on the D7 – D0 inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The outputs (Q7 – Q0) decrement when CE is High and UP is Low during the Low-to-High clock transition. The outputs (Q7 – Q0) increment when CE and UP are High. The counter ignores clock transitions when CE is Low.

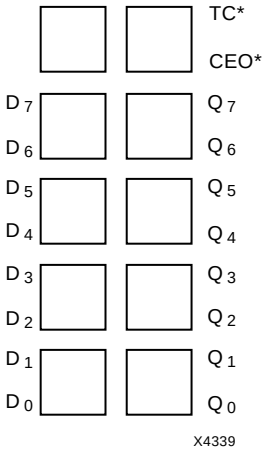
For counting up, the TC output is High when all Q outputs and UP are High. For counting down, the TC output is High when all Q outputs and UP are Low. To cascade counters, the count enable out (CEO) output of each counter is connected to the CE pin of the next stage. The clock, UP, L, and CLR inputs are connected in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than n(tCE-TC), where “n” is the number of stages and “tCE-TC” is the CE-to-TC propagation delay of each stage.

The counter is asynchronously reset, output Low, when power is applied or when global set/reset (GSR) for XC4000/4000E or global reset (GR) for XC5200 is active. The GSR active level is programmable. When cascading counters, use the CEO output if the counter uses the CE input; otherwise, use the TC output.

Inputs						Outputs		
CLR	**L**	**CE**	**C**	**UP**	**D7 – D0[a]**	**Q7 – Q0**	**TC[b]**	**CEO[c]**
1	X	X	X	X	X	0	0	0
0	1	X	X	X	D	d7 – d0	TC	CEO
0	0	0	X	X	X	No Chg	No Chg	0
0	0	1	↑	1	X	Inc	TC	CEO
0	0	1	↑	0	X	Dec	TC	CEO

a. dn = state of referenced clock one set-up time prior to active clock transition
b. TC = (Q7•Q6•Q5•...•Q0•UP) + ($\overline{Q7}$•$\overline{Q6}$•$\overline{Q5}$•...•$\overline{Q0}$•$\overline{UP}$)
c. CEO = (TC•CE)

XC4000 Topology[1]



1. In the process of combining the logic that loads CEO and TC, the place and route software might map the logic that generates CEO and TC to different function generators. If this mapping occurs, the CEO and TC logic cannot be placed in the uppermost CLB as indicated in the illustration.

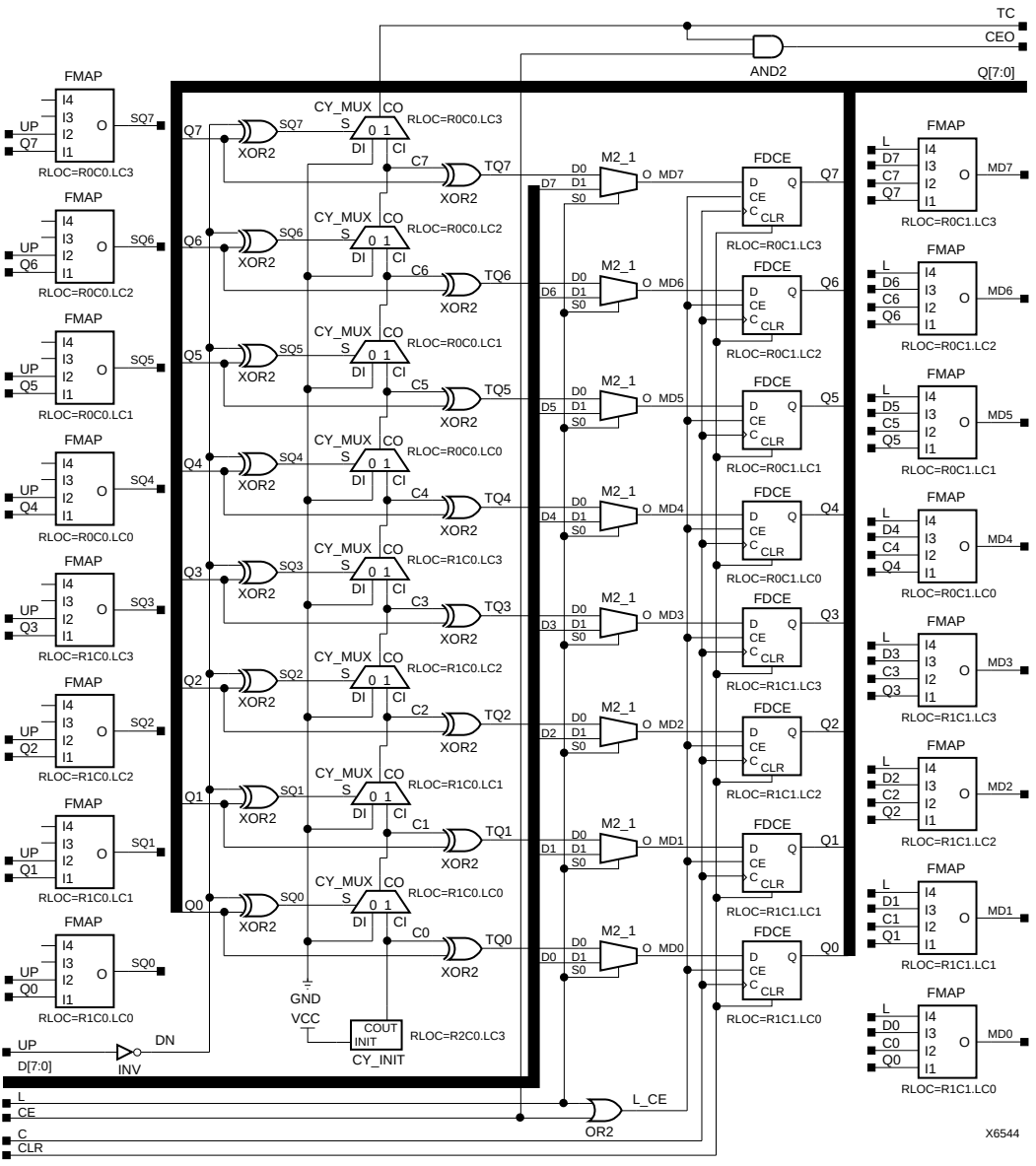
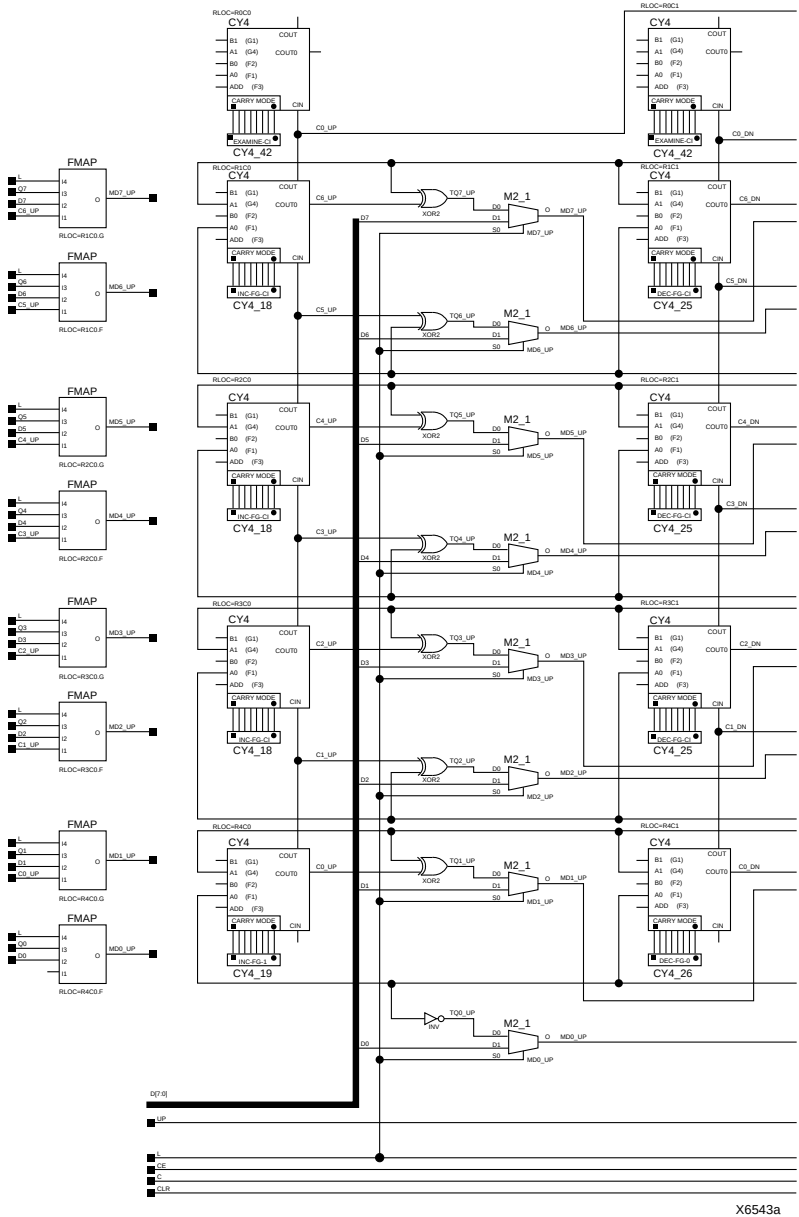


Figure 3-22 CC8CLED XC5200 Implementation


RLOC=R0C0
RLOC=R0C1
CY4
CY4_42
EXAMINE-CI
CARRY MODE
C0_UP
C0_DN
RLOC=R1C0
RLOC=R1C1
CY4_18
CY4_25
INC-FG-CI
DEC-FG-CI
C5_UP
C5_DN
RLOC=R2C0
RLOC=R2C1
C4_UP
C4_DN
C3_UP
C3_DN
RLOC=R3C0
RLOC=R3C1
C2_UP
C2_DN
C1_UP
C1_DN
RLOC=R4C0
RLOC=R4C1
CY4_19
CY4_26
INC-FG-1
DEC-FG-0
FMAP
RLOC=R1C0.G
RLOC=R1C0.F
RLOC=R2C0.G
RLOC=R2C0.F
RLOC=R3C0.G
RLOC=R3C0.F
RLOC=R4C0.G
RLOC=R4C0.F
XOR2
INV
M2_1
MD7_UP
MD6_UP
MD5_UP
MD4_UP
MD3_UP
MD2_UP
MD1_UP
MD0_UP
D[7:5]
UP
CE
C
CLR

X6543a

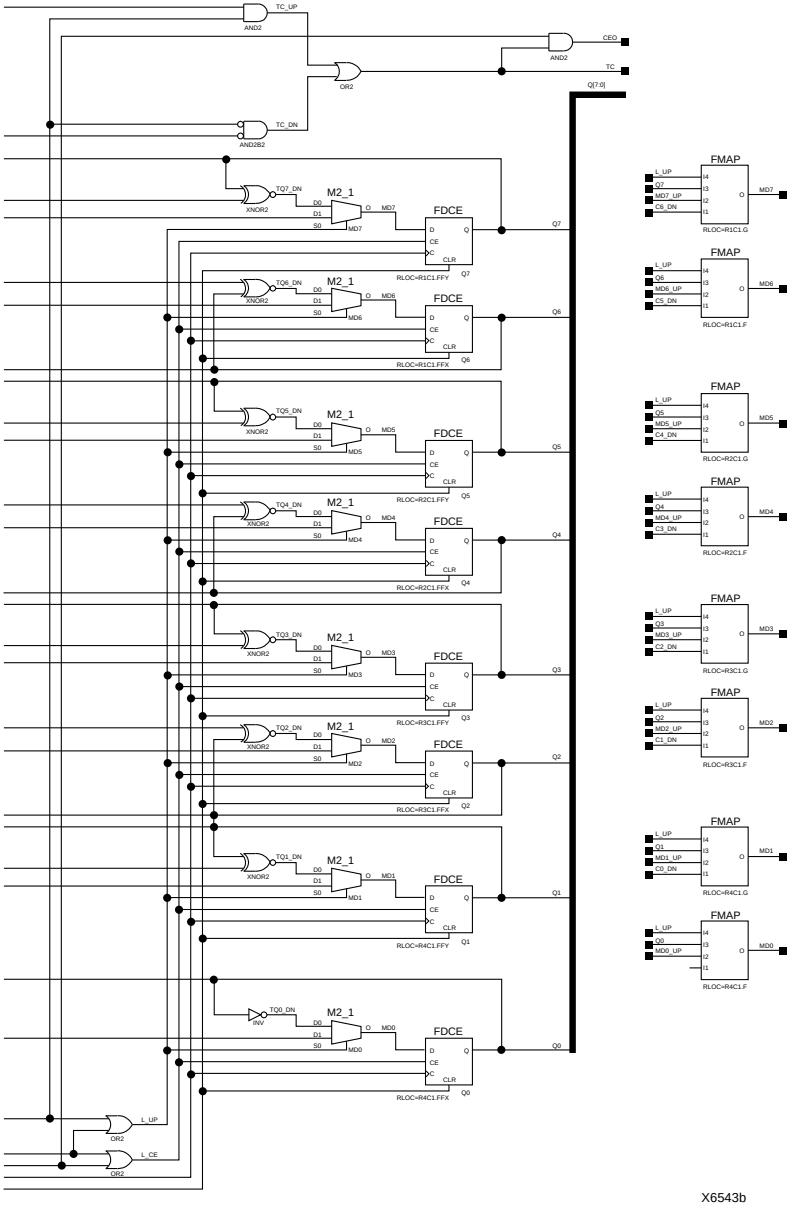
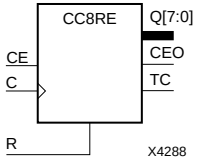


Figure 3-23 CC8CLED XC4000/4000E Implementation

CC8RE

8-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset



XC4000	XC4000E	XC5200
Macro	Macro	Macro

CC8RE is an 8-stage, 8-bit, synchronous, resettable, cascadable binary counter. The counter is implemented using carry logic with relative location constraints to ensure efficient placement of logic. The synchronous reset (R) is the highest priority input. When R is High, all other inputs are ignored and data (Q7 – Q0) and terminal count (TC) outputs go to logic level zero on the Low-to-High clock (C) transition. The outputs (Q7 – Q0) increment when the clock enable input (CE) is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs and CE are High.

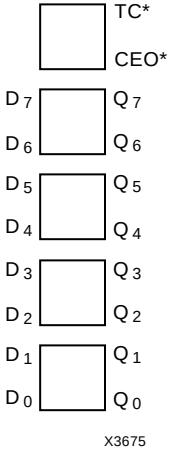
Larger counters are created by connecting the count enable out (CEO) output of the first stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than *n*(tCE-TC), where *n* is the number of stages and "tCE-TC" is the CE-to-TC propagation delay of each stage.

The counter is asynchronously reset, with Low outputs, when power is applied or when global set/reset (GSR) for XC4000/4000E or global reset (GR) for XC5200 is active. The GSR active level is programmable. When cascading counters, use the CEO output if the counter uses the CE input; use the TC output if it does not.

Inputs			Outputs		
R	**CE**	**C**	**Q7 – Q0**	**TC[a]**	**CEO[b]**
1	X	↑	0	0	0
0	0	X	No Chg	No Chg	0
0	1	↑	Inc	TC	CEO

a. TC = (Q7•Q6•Q5•...•Q0•CE)
b. CEO = (TC•CE)

XC4000/4000E Topology[1]



1. In the process of combining the logic that loads CEO and TC, the place and route software might map the logic that generates CEO and TC to different function generators. If this mapping occurs, the CEO and TC logic cannot be placed in the uppermost CLB as indicated in the illustration.

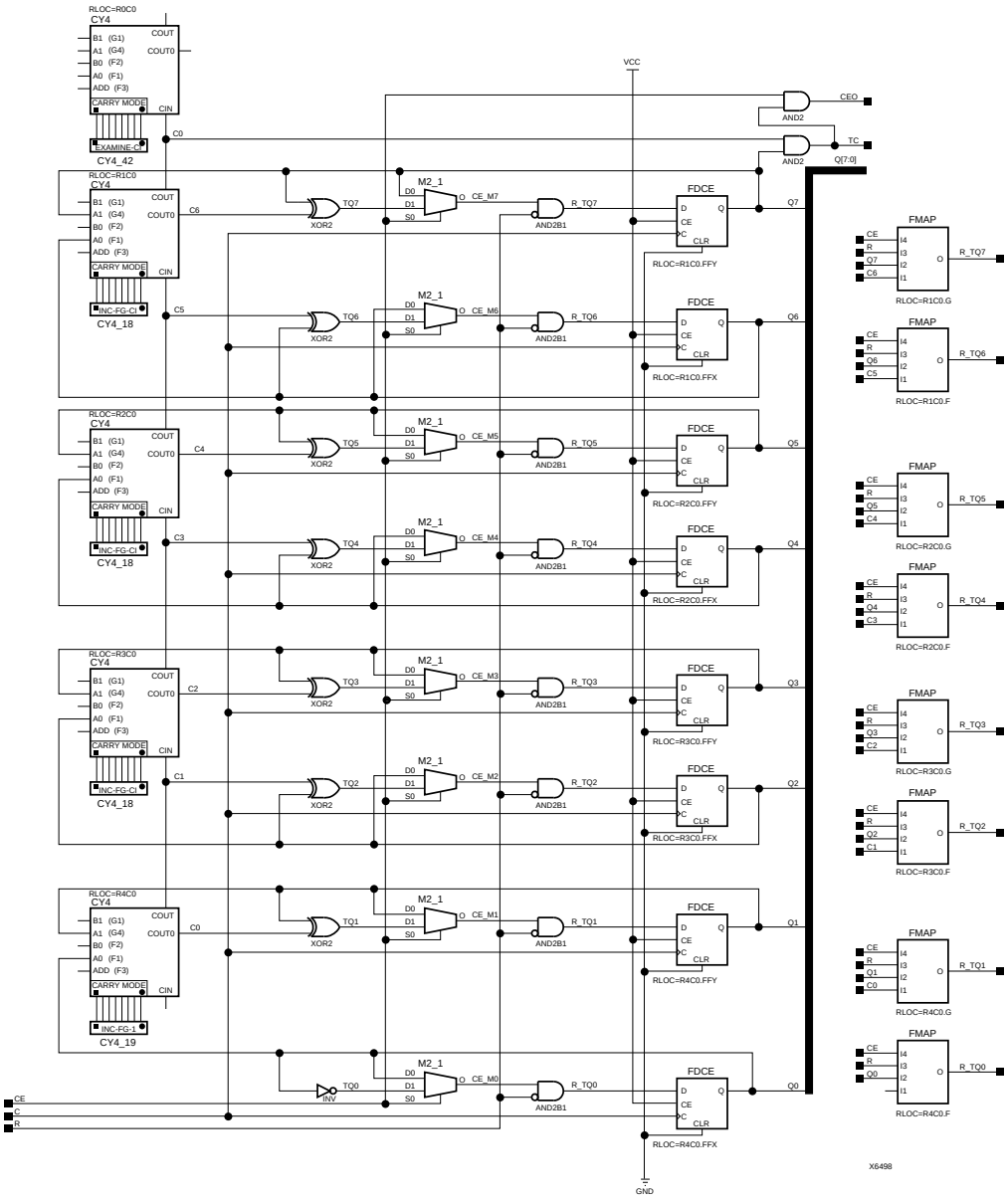


Figure 3-24 CC8RE XC4000/4000E Implementation

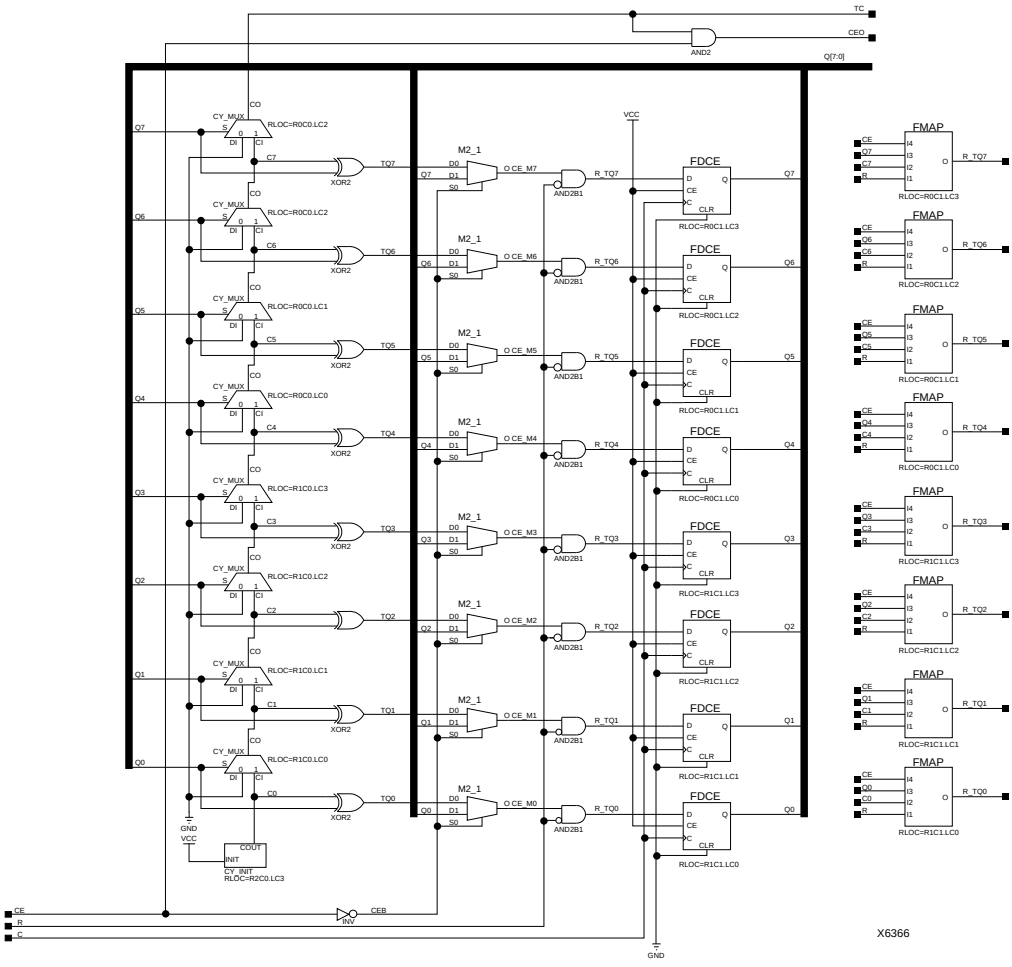
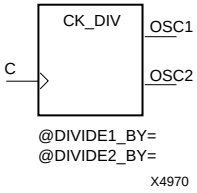


Figure 3-25 CC8RE XC5200 Implementation

CK_DIV

Internal Multiple-Frequency Clock Divider



XC4000E	XC5200
N/A	Macro

CK_DIV divides a user-provided external clock signal with different divide factors on either or both of the outputs. Only one CK_DIV may be used per design. The CK_DIV is not available if the OSC5 element is used.

The clock frequencies of the OSC1 and OSC2 outputs are determined by specifying the DIVIDE1_BY=n_1 attribute for the OSC1 output, and the DIVIDE2_BY=n_2 attribute for the OSC2 output. n_1 and n_2 are integer numbers by which the clock input (C) is divided to produce the desired output clock frequency. The available values of n_1 and n_2 are shown in the table.

n_1	n_2
4	2
16	8
64	32
256	128
	1,024
	4,096
	16,384
	65,536

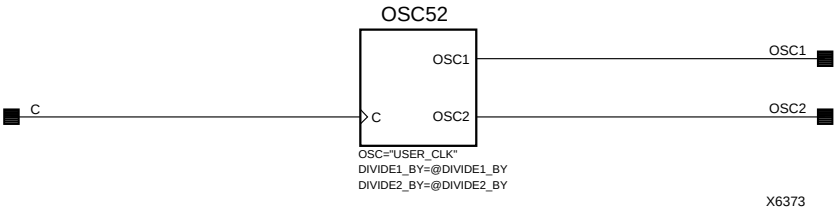
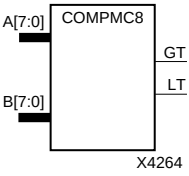


Figure 3-26 CK_DIV XC5200 Implementation

COMPMC8

8-Bit Magnitude Comparator

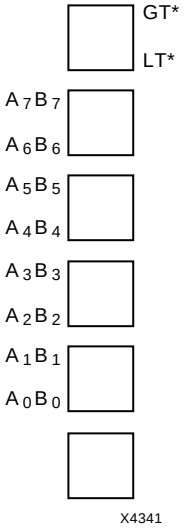


XC4000	XC4000E	XC5200
Macro	Macro	Macro

COMPMC8 is an 8-bit, magnitude comparator that compares two positive binary-weighted words A7 – A0 and B7 – B0, where A7 and B7 are the most significant bits. The comparator is implemented using carry logic with relative location constraints to ensure efficient logic placement. The greater-than output (GT) is High when A>B, and the less-than output (LT) is High when A<B. When the two words are equal, both GT and LT are Low. Equality can be flagged with this macro by connecting both outputs to a NOR gate, as shown in the table.

Inputs				Outputs	
A3, B3	**A2, B2**	**A1, B1**	**A0, B0**	**GT**	**LT**
A3>B3	X	X	X	1	0
A3<B3	X	X	X	0	1
A3=B3	A2>B2	X	X	1	0
A3=B3	A2<B2	X	X	0	1
A3=B3	A2=B2	A1>B1	X	1	0
A3=B3	A2=B2	A1<B1	X	0	1
A3=B3	A2=A2	A1=B1	A0>B0	1	0
A3=B3	A2=B2	A1=B1	A0<B0	0	1
A3=B3	A2=B2	A1=B1	A0=B0	0	0

XC4000/4000E Topology[1]



1. In the process of combining the logic that loads GT and LT, the place and route software might map the logic that generates GT and LT to different function generators. If this mapping occurs, the GT and LT logic cannot be placed in the uppermost CLB, as indicated in the illustration.

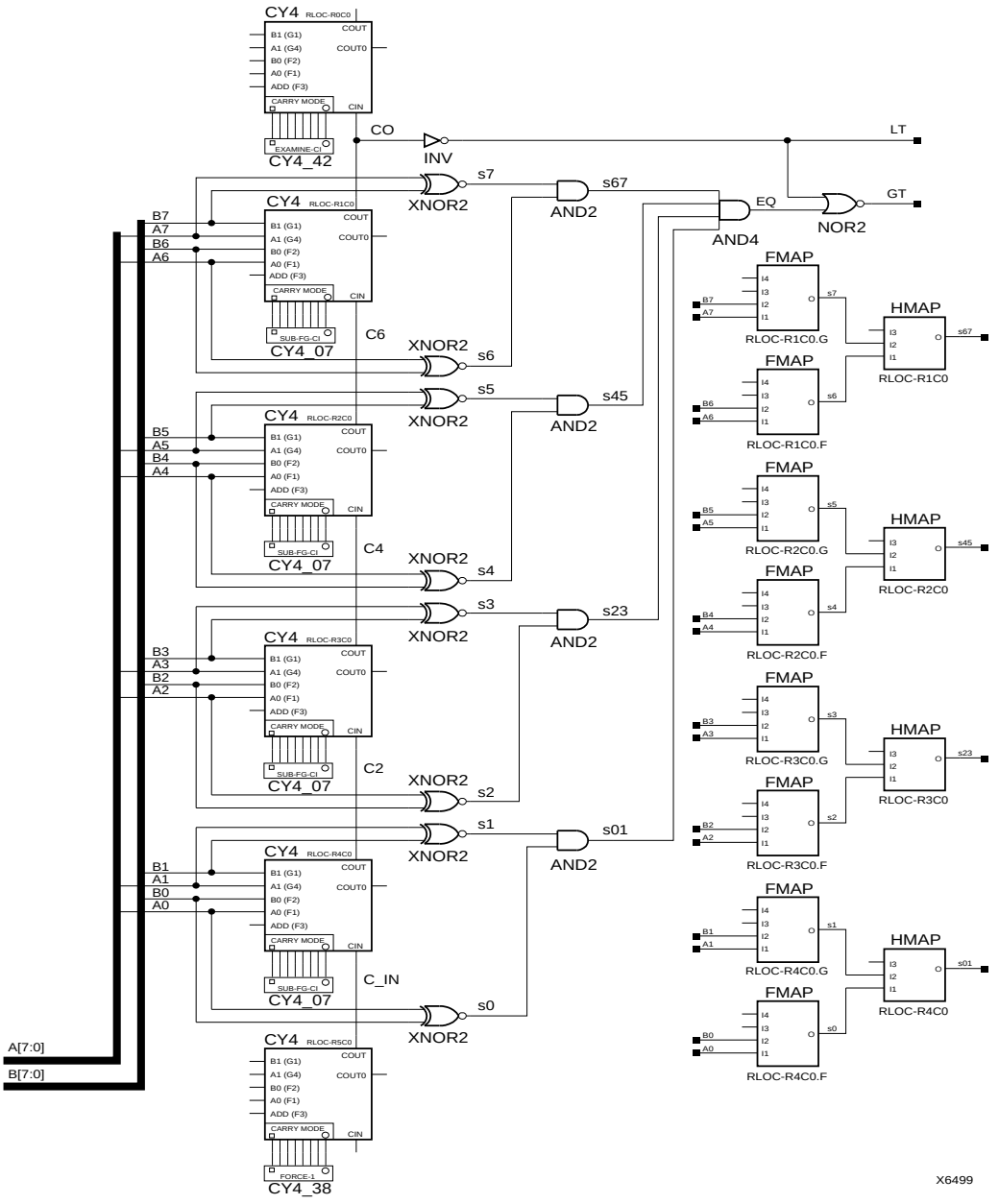


Figure 3-27 COMPMC8 XC4000/4000E Implementation

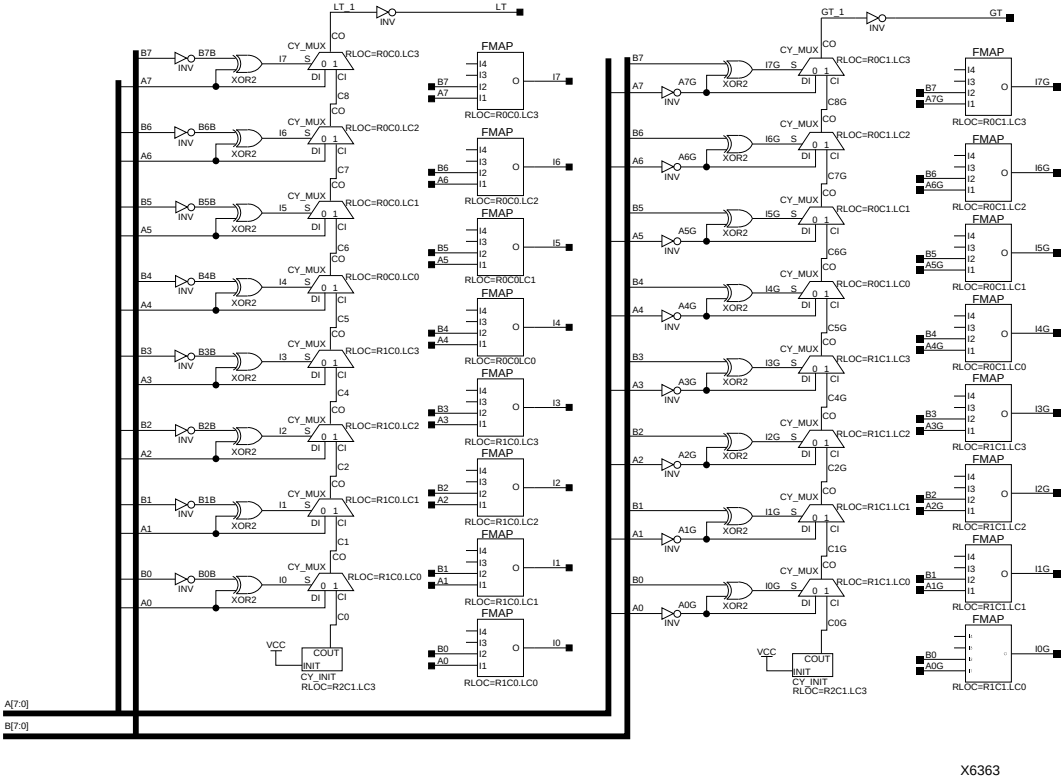
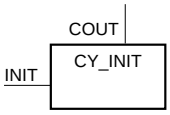


Figure 3-28 COMPMC8 XC5200 Implementation

CY_INIT

Initialization Stage for Carry Chain



XC4000E	XC5200
N/A	Macro

CY_INIT is used to initialize the carry chain in the XC5200 architecture. It is used in conjunction with multiple CY_MUX elements to implement high speed carry-propagate or high speed cascade logic. CY_INIT must be placed in the logic cell (LC) immediately below the least-significant carry element (CY_MUX) in the carry/cascade chain. The INIT input is driven from the direct input (DI) to LC. The CY_INIT carry-out (COUT) drives the C_{in} input of the first LC in the carry chain. The COUT output reflects the state of the DI input. This figure represents the schematic implementation of CY_INIT.

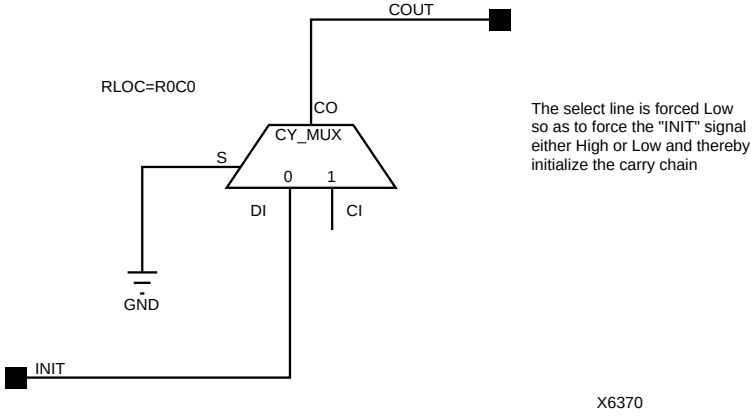
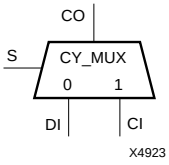


Figure 3-29 CY_INIT XC5200 4-Bit Adder Implementation

CY_MUX

2-to-1 Multiplexer for Carry Logic



XC4000E	XC5200
N/A	Primitive

CY_MUX is used to implement a 1-bit high-speed carry propagate function. One such function can be implemented per logic cell (LC), for a total of 4-bits per configurable logic block (CLB). The direct input (DI) of an LC is connected to the DI input of the CY_MUX. The carry in (CI) input of an LC is connected to the CI input of the CY_MUX. The select input (S) of the CY_MUX is driven by the output of the lookup table (LUT), and configured as an XOR function. The carry-out (CO) of the CY_MUX reflects the state of the selected input and implements the carry out function of each LC. When Low, S selects DI; when High, S selects CI.

Inputs			Outputs
S	DI	CI	CO
0	1	X	1
0	0	X	0
1	X	1	1
1	X	0	0

The "CY_MUX XC5200 4-Bit Adder Schematic" illustration depicts the application of the CY_MUX for a 4-bit adder. Also shown are the associated FMAP symbols and the CY_INIT function.

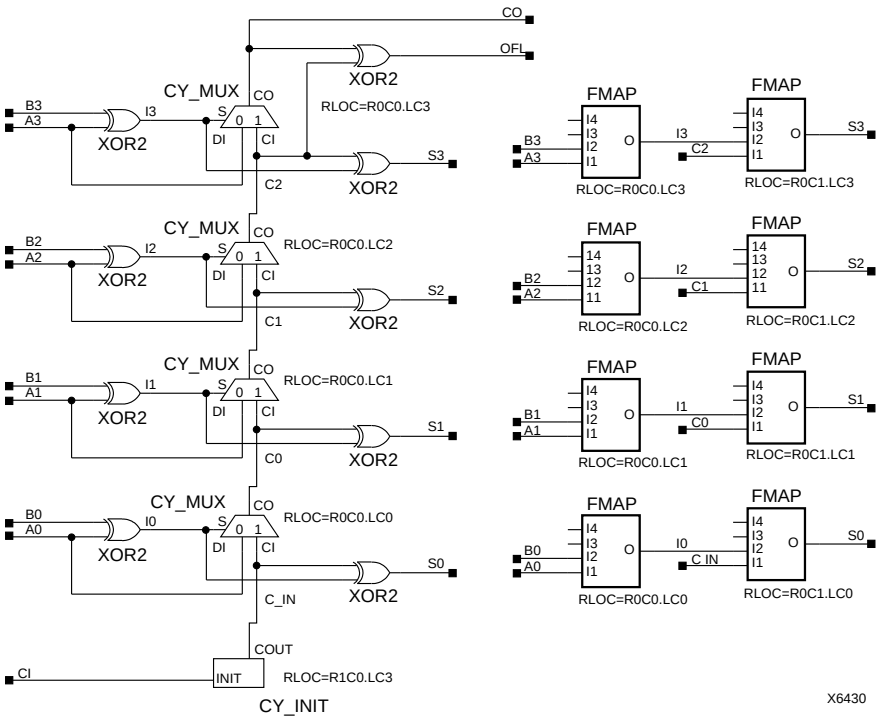


Figure 3-30 CY_MUX XC5200 4-Bit Adder Schematic

DECODE4, DECODE8, DECODE16, DECODE32, and DECODE64

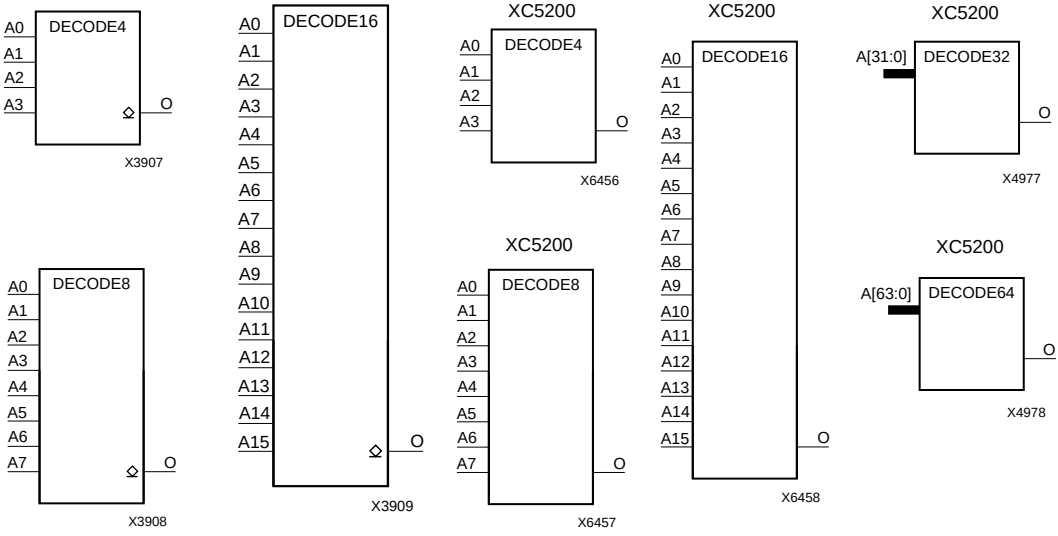
4-, 8-, 16-, 32-, and 64-Bit Active-Low Decoders

Element	XC4000	XC4000E	XC5200
DECODE4, DECODE8, DECODE16	Macro	Macro	Macro
DECODE32, DECODE64	N/A	N/A	Macro

In the XC4000/4000E architectures, decoders are open-drain wired-AND gates. When one or more of the inputs (A) are Low, output (O) is Low. When all the inputs are High, the output is High or Off. A pull-up resistor must be connected to the output node to achieve a true logic High. A double pull-up resistor can be used to achieve faster performance; however, it uses more power. The XACT software implements these macros using the open-drain AND gates around the periphery of the XC4000/4000E devices.

In XC5200, decoders are implemented by cascading CY_MUX elements driven by lookup tables (LUTs). When one or more of the inputs are Low, the output is Low. When all the inputs are High, the output is High. You can decode patterns by adding inverters to inputs.

Note: Pull-ups cannot be used on XC5200 longlines. Diamonds in library symbols indicate an open-drain output.



Inputs				Outputs[a]
A0	**A1**	**...**	**A(n-1)**	**O**
1	1	1	1	1
0	X	X	X	0
X	0	X	X	0
X	X	X	0	0

a. A pull-up resistor must be connected to the output to establish High-level drive current.

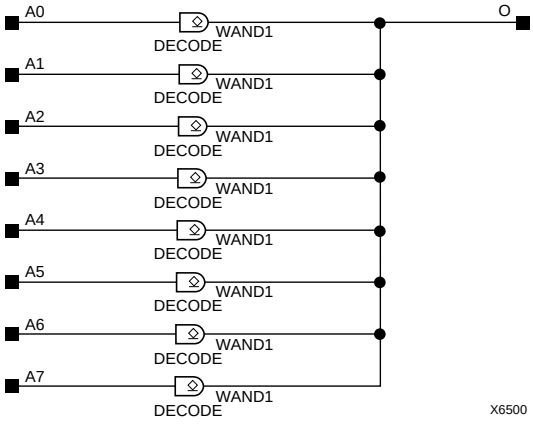


Figure 3-31 DECODE8 XC4000/XC4000E Implementation

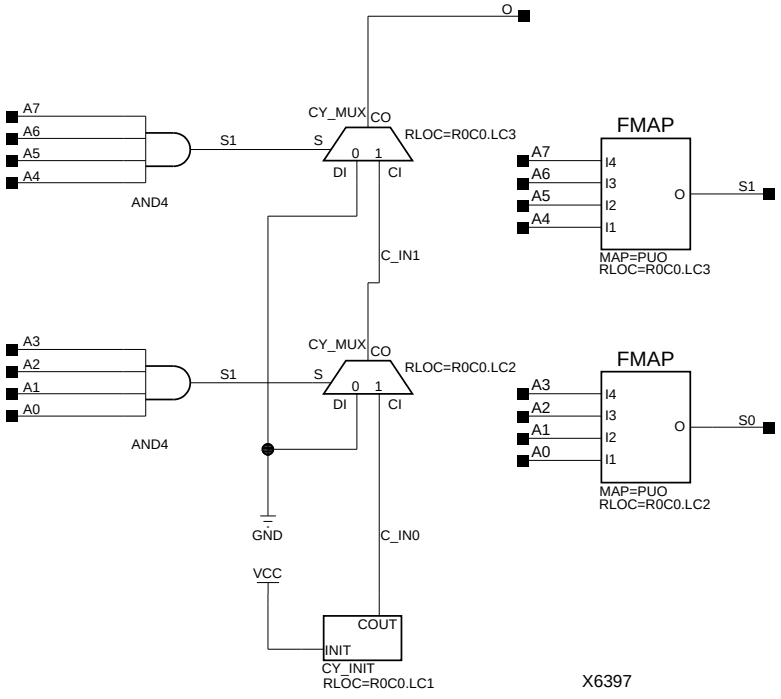
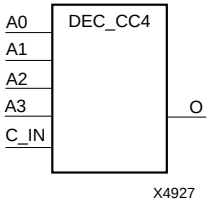
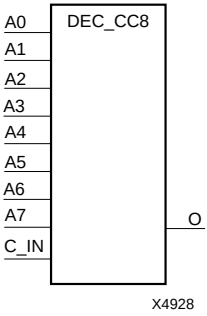


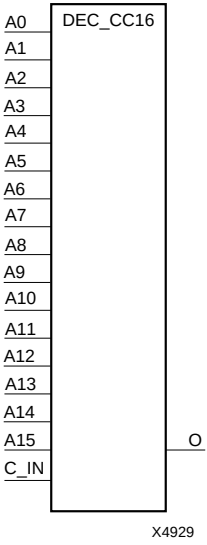
Figure 3-32 DECODE8 XC5200 Implementation

DEC_CC4, DEC_CC8, and DEC_CC16

4-, 8-, and 16-Bit Active Low Decoders







Element	XC4000E	XC5200
DEC_CC4, DEC_CC8, DEC_CC16	N/A	Macro

These decoders are used to build wide-decoder functions. They are implemented by cascading CY_MUX elements driven by lookup tables (LUTs). The C_IN pin can only be driven by a CY_INIT or by the output (O) of a previous decode stage. When one or more of the inputs (A) are Low, the output is Low. When all the inputs are High and the C_IN input is High, the output is High. You can decode patterns by adding inverters to inputs.

Inputs					Outputs
A0	**A1**	**…**	**A(n-1)**	**C_IN**	**O**
1	1	1	1	1	1
X	X	X	X	0	0
0	X	X	X	X	0
X	0	X	X	X	0
X	X	X	0	X	0

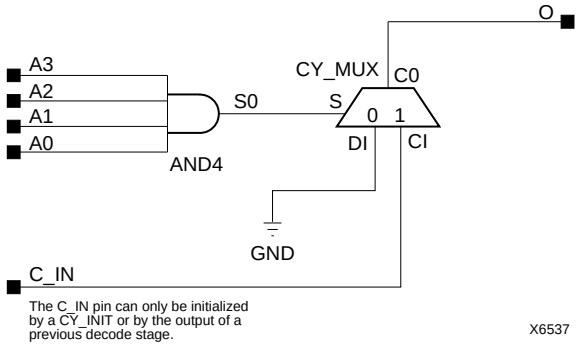


Figure 3-33 DEC_CC4 XC5200 Implementation

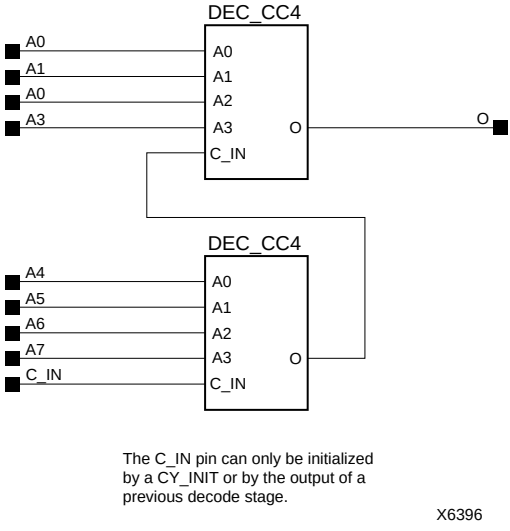
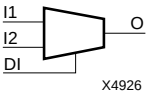


Figure 3-34 DEC_CC8 XC5200 Implementation

F5_MUX

2-to-1 Lookup Table Multiplexer



XC4000E	XC5200
N/A	Primitive

F5_MUX provides a multiplexer function in one half of a CLB. The output from the lookup table (LUT) in LC1 is connected to the I1 input of the F5_MUX and the output from the LUT in LC0 is connected to the I2 input. The direct input (DI) of LC0 is connected to the DI input of the F5_MUX. The output (O) reflects the state of the selected input. When Low, DI selects I1; when High, DI selects I2. Similarly, the F5_MUX can connect to the LUTs in LC2 and LC3. The F5_MUX can also implement any 5-input function in the top or bottom half of a CLB when the mapping of the function is controlled by F5MAP.

Inputs			Outputs
DI	**I1**	**I2**	**O**
0	1	X	1
0	0	X	0
1	X	1	1
1	X	0	0

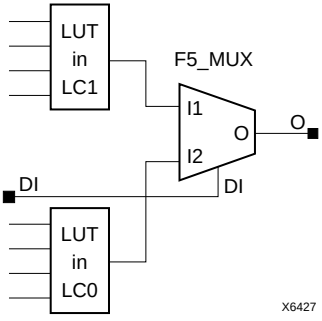
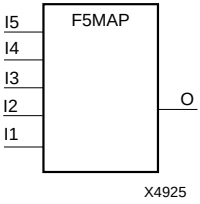


Figure 3-35 F5_MUX Representation

F5MAP

5-Input Function Partitioning Control Symbol



XC4000E	XC5200
N/A	Primitive

The F5MAP symbol is used to control the logic partitioning of 5-input functions into the top or bottom half of a CLB. The F5MAP symbol is not a substitute for logic. It is used in addition to combinatorial gates for mapping control.

At the schematic level, any 5-input logic function can be implemented using gates, and mapped into half of a single CLB by using the F5MAP symbol. The signals that are the inputs and outputs of the 5-input function must be labelled and connected to appropriate pins of the F5MAP symbol, or the F5MAP signals and logic signals must have identical labels. The symbol can have unconnected pins, but all signals on the logic group to be mapped must be specified on a symbol pin.

Using F5MAP forces any 5-input function to be implemented by two lookup tables (LUTs), the direct input (DI), and the F5_MUX primitive, which are contained within adjacent CLB logic cells LC0 and LC1 or LC2 and LC3.

This figure illustrates the connections within a CLB.

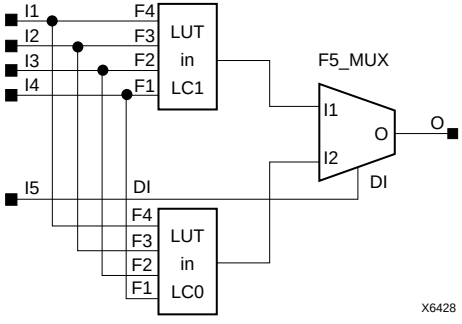


Figure 3-36 Two LUTs in Parallel Combined to Create a 5-Input Function

An F5MAP primitive example is shown in this figure.

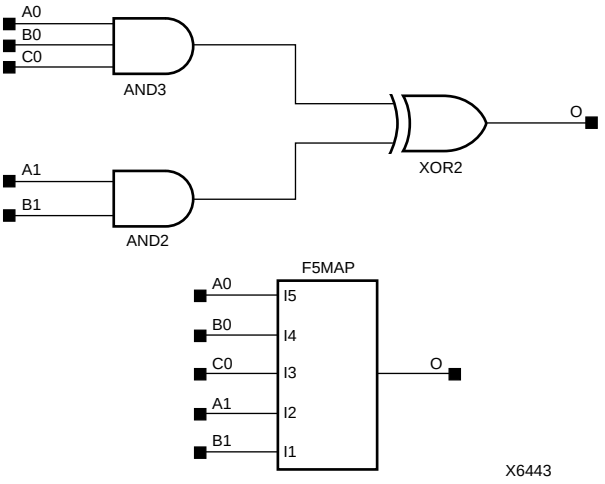
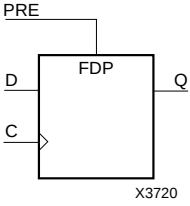


Figure 3-37 F5MAP Primitive Example

FDP

D Flip-Flop with Asynchronous Preset



XC4000	XC4000E	XC5200	XC7000
Macro	Macro	Macro	Primitive

FDP is a single D-type flip-flop with data (D) and asynchronous preset (PRE) inputs, and data output (Q). The asynchronous PRE, when High, overrides all other inputs and presets the Q output High. The data on the D input is loaded into the flip-flop when PRE is Low on the Low-to-High clock (C) transition. The flip-flop is asynchronously set, output High, when global set/reset (GSR) for XC4000/4000E or global reset (GR) for XC5200 is active. The GSR/GR active level is programmable.

Inputs			Outputs
PRE	D	C	Q
1	X	X	1
0	1	↑	1
0	0	↑	0

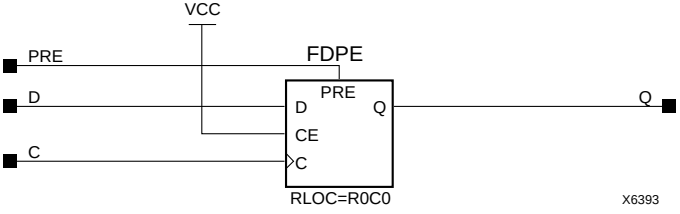
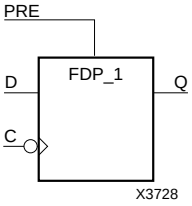


Figure 3-38 FDP XC4000/4000E/5200 Implementation

FDP_1

D Flip-Flop with Negative-Edge Clock and Asynchronous Preset



XC4000	XC4000E	XC5200
Macro	Macro	Macro

FDP_1 is a single D-type flip-flop with data (D) and asynchronous preset (PRE) inputs, and data output (Q). The asynchronous PRE, when High, overrides all other inputs and presets the Q output High. The data on the D input is loaded into the flip-flop when PRE is Low on the High-to-Low clock (C) transition. The flip-flop is asynchronously set, output High, when global set/reset (GSR) for XC4000/4000E or global reset (GR) for XC5200 is active. The GSR/GR active level is programmable.

Inputs			Outputs
PRE	D	C	Q
1	X	X	1
0	1	↓	1
0	0	↓	0

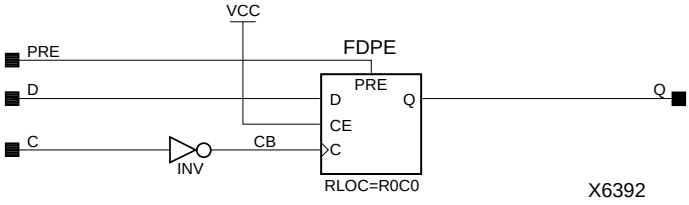
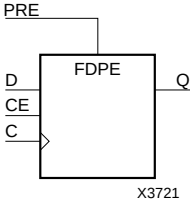


Figure 3-39 FDP_1 XC4000/4000E/5200 Implementation

FDPE

D Flip-Flop with Clock Enable and Asynchronous Preset



XC4000	XC4000E	XC5200	XC7000
Primitive	Primitive	Macro	Primitive

FDPE is a single D-type flip-flop with data (D), clock enable (CE), and asynchronous preset (PRE) inputs and data output (Q). The asynchronous PRE, when High, overrides all other inputs and sets the Q output High. Data on the D input is loaded into the flip-flop when PRE is Low and CE is High on the Low-to-High clock (C) transition. When CE is Low, the clock transitions are ignored. The flip-flop is asynchronously set, output High, when global set/reset (GSR) for XC4000/4000E or global reset (GR) for XC5200 is active. The GSR/GR active level is programmable.

Inputs				Outputs
PRE	CE	D	C	Q
1	X	X	X	1
0	0	X	X	No Chg
0	1	0	↑	0
0	1	1	↑	1

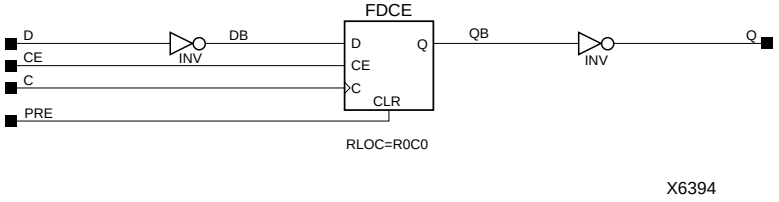
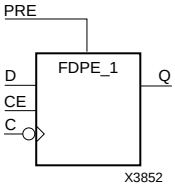


Figure 3-40 FDPE XC5200 Implementation

FDPE_1

D FLip-Flop with Negative-Edge Clock, Clock Enable, and Asynchronous Preset



XC4000	XC4000E	XC5200
Macro	Macro	Macro

FDPE_1 is a single D-type flip-flop with data (D), clock enable (CE), and asynchronous preset (PRE) inputs and data output (Q). The asynchronous PRE, when High, overrides all other inputs and sets the Q output High. Data on the D input is loaded into the flip-flop when PRE is Low and CE is High on the High-to-Low clock (C) transition. When CE is Low, the clock transitions are ignored. The flip-flop is asynchronously set, output High, when global set/reset (GSR) for XC4000/4000E or global reset (GR) for XC200 is active. The GSR/GR active level is programmable.

Inputs				Outputs
PRE	CE	D	C	Q
1	X	X	X	1
0	0	X	X	No Chg
0	1	1	↓	1
0	1	0	↓	0

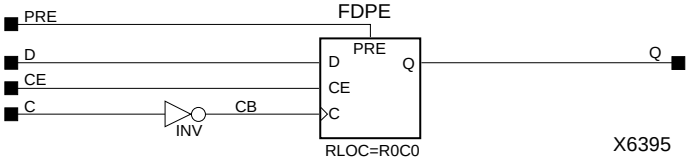
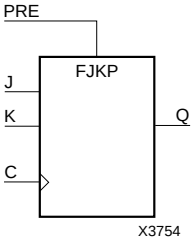


Figure 3-41 FDPE_1 XC4000/4000E/5200 Implementation

FJKP

J-K Flip-Flop with Asynchronous Preset



XC4000	XC4000E	XC5200	XC7000
Macro	Macro	Macro	Primitive

FJKP is a single J-K-type flip-flop with J, K, and asynchronous preset (PRE) inputs and data output (Q). The asynchronous preset (PRE) input, when High, overrides all other inputs and sets the Q output High on the Low-to-High clock (C) transition. When PRE is Low, the Q output responds to the state of the J and K inputs, as shown in the following truth table, during the Low-to-High clock transition. The flip-flop is asynchronously set, output High, when global set/reset (GSR) for XC4000/4000E or global reset (GR) for XC5200 is active; the GSR/GR active level is programmable.

Inputs				Outputs
PRE	J	K	C	Q
1	X	X	X	1
0	0	0	X	No Chg
0	0	1	↑	0
0	1	0	↑	1
0	1	1	↑	Toggle

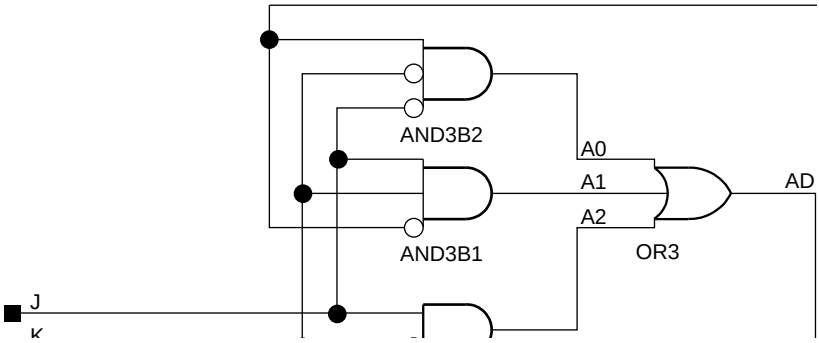
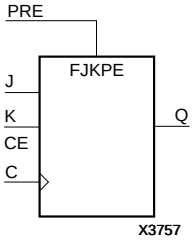


Figure 3-42 FJKP XC4000/4000E/5200 Implementation

FJKPE

J-K Flip-Flop with Clock Enable and Asynchronous Preset



XC4000	XC4000E	XC5200	XC7000
Macro	Macro	Macro	Primitive

FJKPE is a single J-K-type flip-flop with J, K, clock enable (CE), and asynchronous preset (PRE) inputs and data output (Q). The asynchronous preset (PRE), when High, overrides all other inputs and sets the Q output High. When PRE is Low and CE is High, the Q output responds to the state of the J and K inputs, as shown in the truth table, during the Low-to-High clock (C) transition. When CE is Low, clock transitions are ignored. The flip-flop is asynchronously set, output High, when global set/reset (GSR) for XC4000/4000E or global reset (GR) for XC5200 is active; the GSR/GR active level is programmable.

Inputs					Outputs
PRE	CE	J	K	C	Q
1	X	X	X	X	1
0	0	X	X	X	No Chg
0	1	0	0	X	No Chg
0	1	0	1	↑	0
0	1	1	0	↑	1
0	1	1	1	↑	Toggle

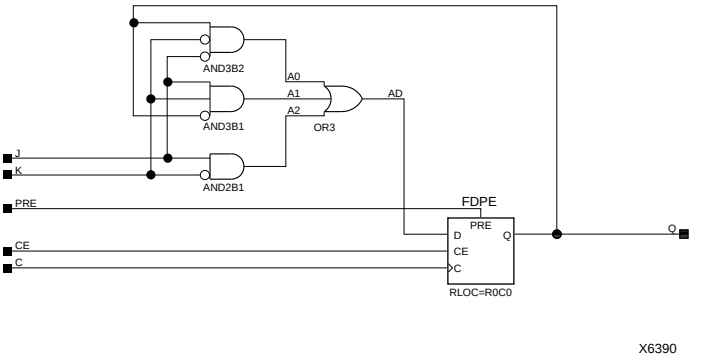
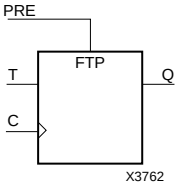


Figure 3-43 FJKPE XC4000/4000E/5200 Implementation

FTP

Toggle Flip-Flop with Toggle Enable and Asynchronous Preset



XC4000	XC4000E	XC5200	XC7000
Macro	Macro	Macro	Primitive

When the asynchronous preset (PRE) input is High, all other inputs are ignored and output Q is set High. When toggle-enable input (T) is High and PRE is Low, output Q toggles, or changes state, during the Low-to-High clock (C) transition. The flip-flop is asynchronously set, output High, when global set/reset (GSR) for XC4000/4000E or global reset (GR) for XC5200 is active; the GSR/GR level is programmable.

Inputs			Outputs
PRE	T	C	Q
1	X	X	1
0	0	X	No Chg
0	1	↑	Toggle

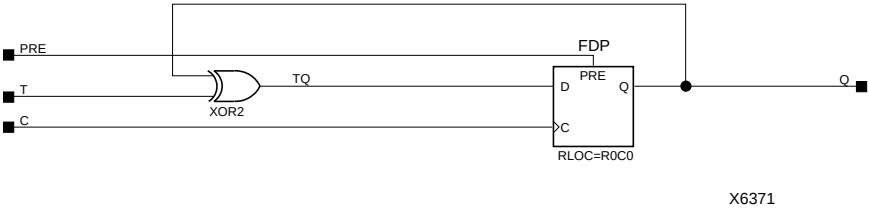
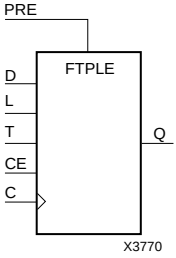


Figure 3-44 FTP XC4000/4000E/5200 Implementation

FTPLE

Toggle/Loadable Flip-Flop with Toggle and Clock Enable and Asynchronous Preset



XC4000	XC4000E	XC5200	XC7000
Macro	Macro	Macro	Primitive

When the asynchronous preset input (PRE) is High, all other inputs are ignored and output Q is set High during the Low-to-High clock (C) transition. When the load enable input (L) is High and PRE is Low, the clock enable (CE) is overridden and the data (D) is loaded into the flip-flop during the Low-to-High clock transition. When L and PRE are Low and toggle-enable input (T) and CE are High, output Q toggles, or changes state, during the Low-to-High clock transition. When CE is Low, clock transitions are ignored. The flip-flop is asynchronously set, output High, when global set/reset (GSR) for XC4000/4000E or global reset (GR) for XC5200 is active; the GSR/GR active level is programmable.

Inputs						Outputs
PRE	L	CE	T	D	C	Q
1	X	X	X	X	X	1
0	1	X	X	1	↑	1
0	1	X	X	0	↑	0
0	0	0	X	X	X	No Chg
0	0	1	0	X	X	No Chg
0	0	1	1	X	↑	Toggle

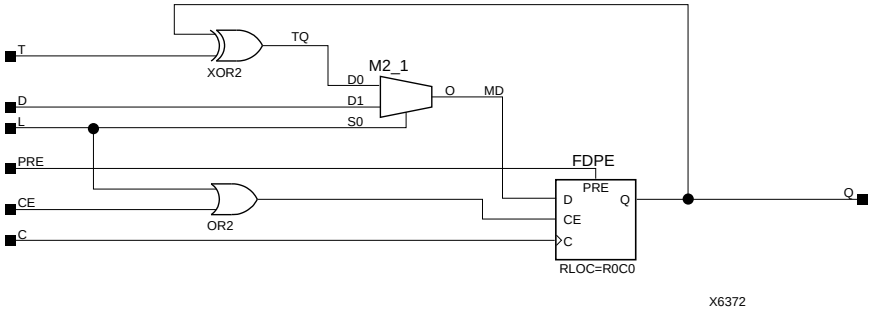


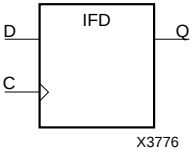
Figure 3-45 FTPLE XC4000/4000E/5200 Implementation

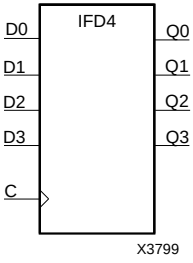
IFD, IFD4, IFD8, and IFD16

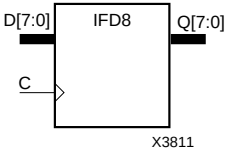
Single- and Multiple-Input D Flip-Flops

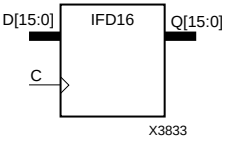
Element	XC2000	XC3000	XC4000	XC4000E	XC5200	XC7000[a]
IFD	Primitive	Primitive	Primitive	Macro	Macro	Primitive
IFD4, IFD8, IFD16	Macro	Macro	Macro	Macro	Macro	Macro

a. not supported for XC7336 designs









The IFD D-type flip-flop is contained in an input/output block (IOB), except for XC5200. The input (D) of the flip-flop is connected to an IPAD or an IOPAD (without using an IBUF). The D input provides data input for the flip-flop, which synchronizes data entering the chip. The data on input D is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). The clock input is controlled by the internal circuit. For XC7000 EPLDs, the clock (C) can only be driven by a FastCLK represented by the BUFG symbol.

The flip-flops are asynchronously reset with Low outputs, when power is applied or when global reset (GR) for XC2000, 3000, and 5200 or global set/reset (GSR) for XC4000/4000E is active. GR is active-Low for XC2000 and 3000. The GR active level is programmable for XC5200. The GSR active level is programmable for XC4000/4000E. For XC7000 EPLDs (except XC7272), the flip-flops are set High when power is applied.

These figures illustrate legal IFD/ILD combinations for XC3000 and XC4000/4000E respectively.

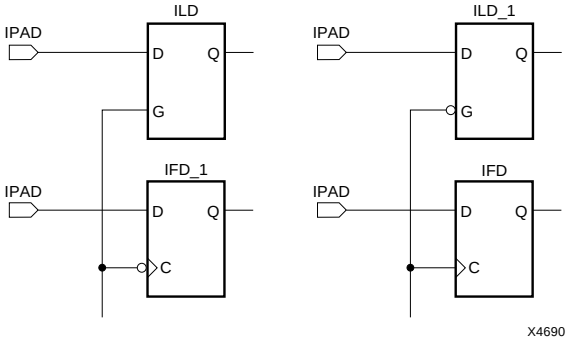


Figure 3-46 Legal Combinations of IFD and ILD for a Single Device Edge of XC3000 IOB

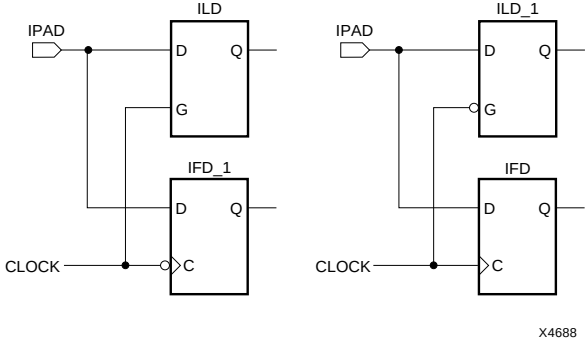


Figure 3-47 Legal Combinations of IFD and ILD for a Single XC4000/4000E IOB

Inputs		Outputs
Dn	**C**	**Qn**
Dn	↑	dn[a]

a. dn = state of referenced input one set-up time prior to active clock transition

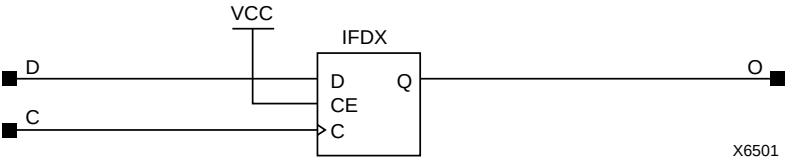


Figure 3-48 IFD XC4000E Implementation

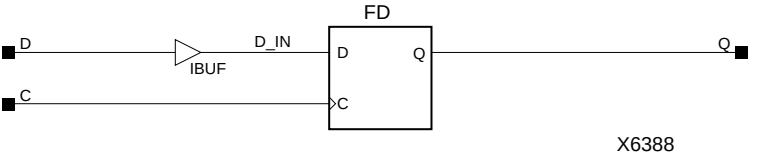


Figure 3-49 IFD XC5200 Implementation

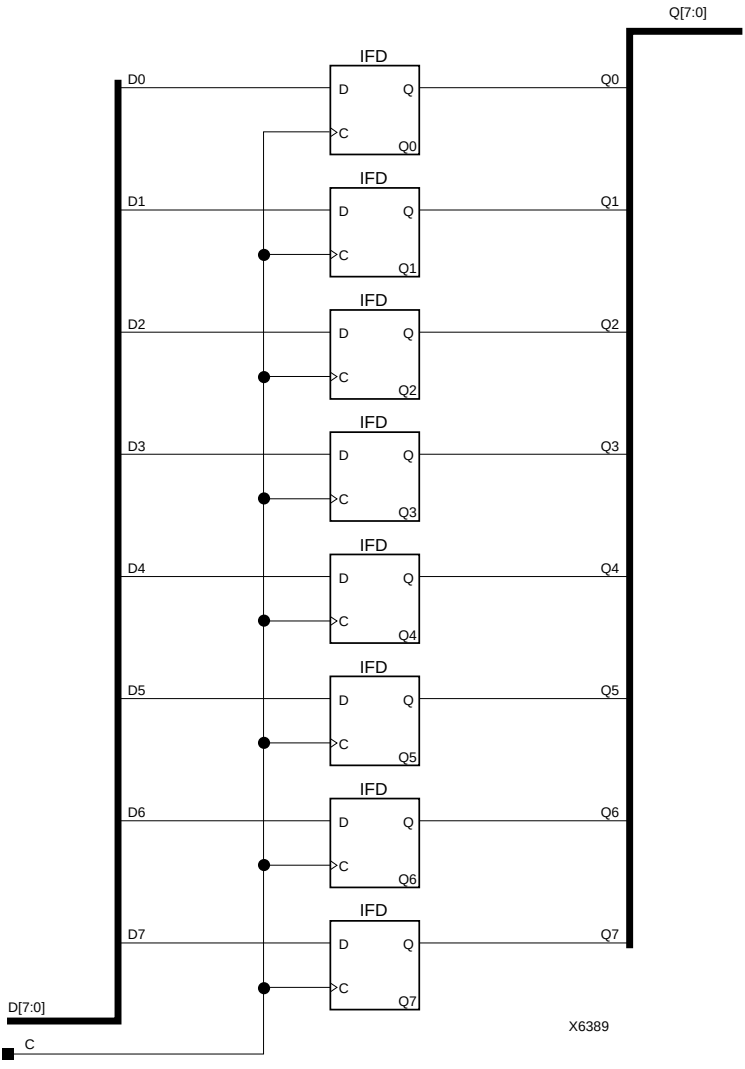
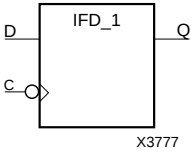


Figure 3-50 IFD8 XC2000/3000/4000/4000E/5200 Implementation

IFD_1

Input D Flip-Flop with Inverted Clock



XC2000	XC3000	XC4000	XC4000E	XC5200
Macro	Macro	Macro	Macro	Macro

The IFD_1 D-type flip-flop is contained in an input/output block (IOB) except for XC5200. The input (D) of the flip-flop is connected to an IPAD or an IOPAD. The D input also provides data input for the flip-flop, which synchronizes data entering the chip. The D input data is loaded into the flip-flop during the High-to-Low clock (C) transition and appears at the output (Q). The clock input is controlled by the internal circuit.

The flip-flop is asynchronously reset with Low output, when power is applied or when global reset (GR) for XC2000, 3000, and 5200 or global set/reset (GSR) for XC4000/4000E is active. GR is active-Low for XC2000 and 3000. The GR active level is programmable for XC5200. The GSR active level is programmable for XC4000/4000E.

These figures illustrate legal IFD/ILD combinations for XC3000 and XC4000/4000E, respectively.

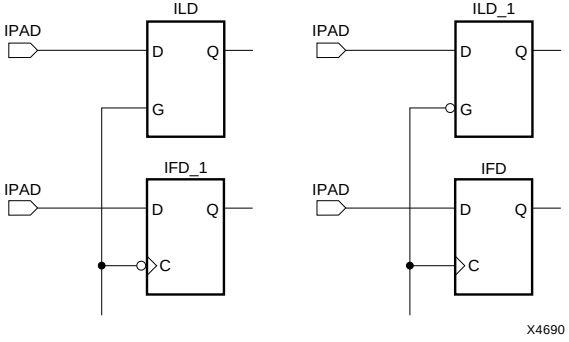


Figure 3-51 Legal Combinations of IFD and ILD for a Single Device Edge of XC3000 IOB

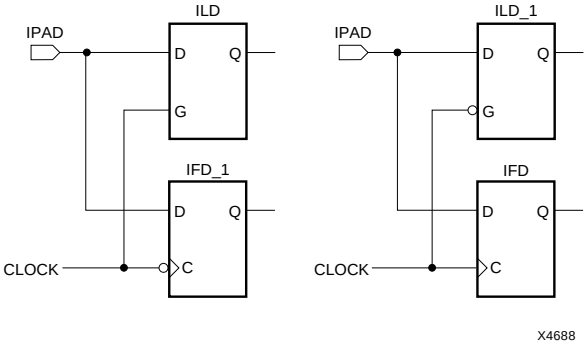


Figure 3-52 Legal Combinations of IFD and ILD for a Single XC4000/4000E IOB

Inputs		Outputs
D	**C**	**Q**
D	↓	d^a

a. d = state of referenced input one set-up time prior to active clock transition

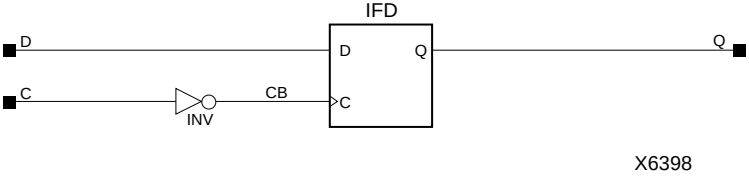
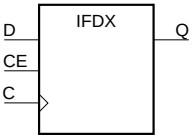


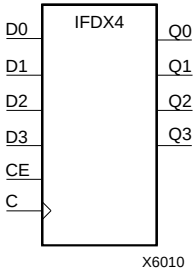
Figure 3-53 XC2000/3000/4000/4000E/5200 Implementation

IFDX, IFDX4, IFDX8, and IFDX16

Single- and Multiple-Input D Flip-Flops with Clock Enable



Element	XC4000E	XC5200
IFDX	Primitive	N/A
IFDX4, IFDX8, IFDX16	Macro	N/A



The IFDX D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD (without using an IBUF). The D input provides data input for the flip-flop, which synchronizes data entering the chip. The data on input D is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). The clock input is controlled by the internal circuit. When CE is Low, flip-flop outputs do not change.

The flip-flops are asynchronously reset with Low outputs, when power is applied or when global set/reset (GSR) is active. The GSR active level is programmable.

This figure illustrates legal IFDX/ILDX combinations for XC4000E.

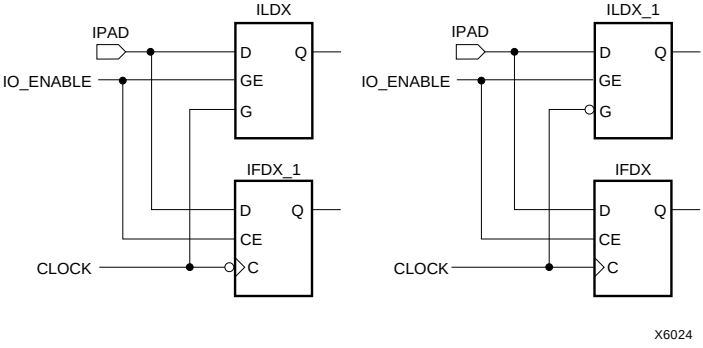


Figure 3-54 Legal Combinations of IFDX and ILDX for a Single XC4000E IOB

Inputs			Outputs
CE	**Dn**	**C**	**Qn**
1	Dn	↑	dn[a]
0	X	X	No Chg

a. dn = state of referenced input one set-up time prior to active clock transition

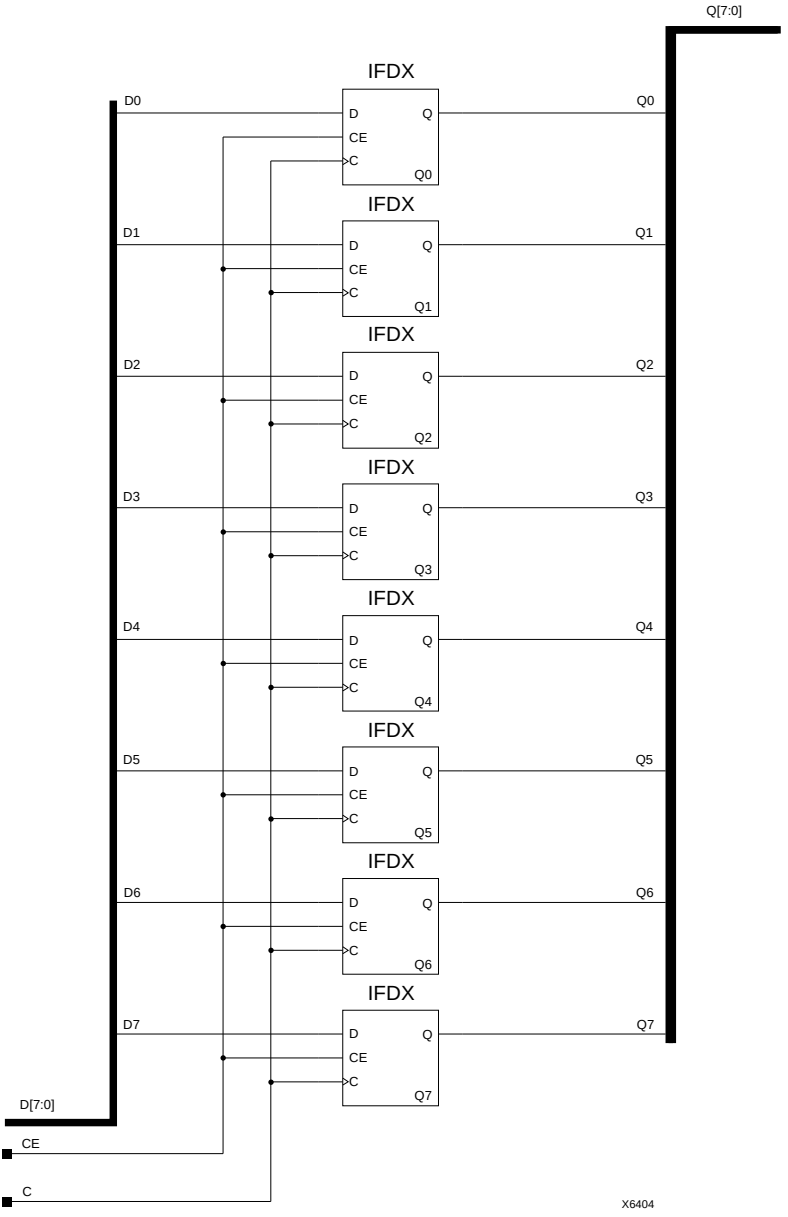
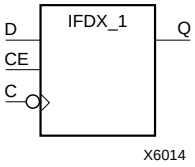


Figure 3-55 IFDX8 XC4000E Implementation

IFDX_1

Input D Flip-Flop with Inverted Clock



XC4000E	XC5200
Macro	N/A

The IFDX_1 D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD. The D input also provides data input for the flip-flop, which synchronizes data entering the chip. The data on input D is loaded into the flip-flop during the High-to-Low clock (C) transition and appears at the output (Q). The clock input is controlled by the internal circuit. When the CE pin is Low, the output (Q) does not change.

The flip-flop is asynchronously reset with Low output, when power is applied or when global set/reset (GSR) is active. The GSR active level is programmable.

This figure illustrates legal IFDX/ILDX combinations for XC4000E.

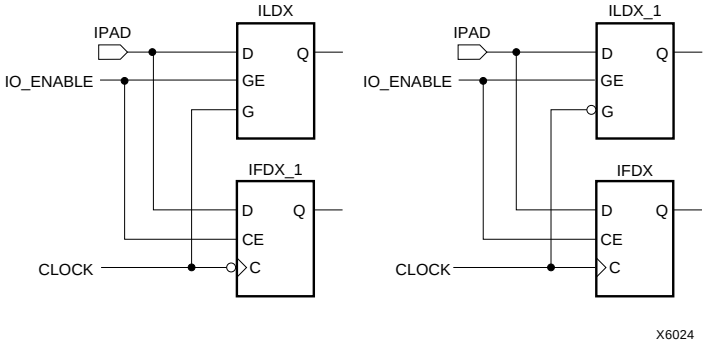


Figure 3-56 Legal Combinations of IFDX and ILDX for a Single XC4000E IOB

Inputs			Outputs
CE	**D**	**C**	**Q**
1	D	↓	d^a
0	X	X	No Chg

a. d = state of referenced input one set-up time prior to active clock transition

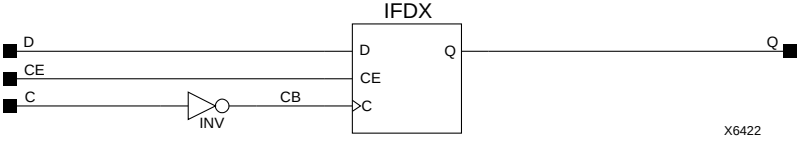
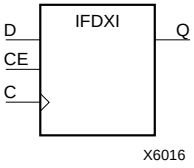


Figure 3-57 IFDX_1 XC4000E Implementation

IFDXI

Input D Flip-Flop (Asynchronous Set)



XC4000E	XC5200
Primitive	N/A

The IFDXI D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD. The D input provides data input for the flip-flop, which synchronizes data entering the chip. The data on input D is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). The clock input is controlled by the internal circuit. The flip-flop is asynchronously set with High output, when power is applied or when global set/reset (GSR) is active. The GSR active level is programmable. When the CE pin is Low, the output (Q) does not change.

This figure illustrates legal IFDXI/ILDXI combinations for XC4000E.

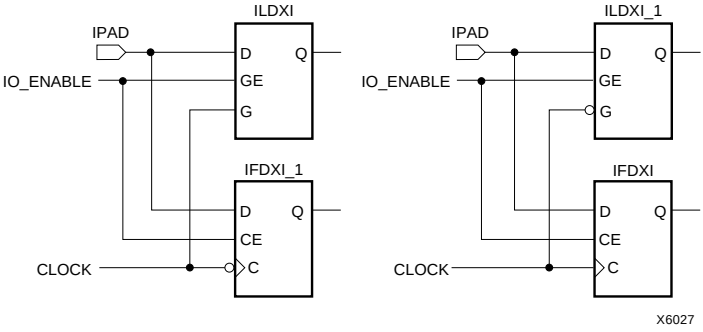


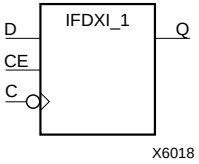
Figure 3-58 Legal Combinations of IFDXI and ILDXI for a Single XC4000E IOB

Inputs			Outputs
CE	**D**	**C**	**Q**
1	D	↑	d^a
0	X	X	No Chg

a. d = state of referenced input one set-up time prior to active clock transition

IFDXI_1

D Flip-Flop with Inverted Clock (Asynchronous Set)



XC4000E	XC5200
Macro	N/A

The IFDXI_1 D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD. The D input provides data input for the flip-flop, which synchronizes data entering the chip. The data on input D is loaded into the flip-flop during the High-to-Low clock (C) transition and appears at the output (Q). The clock input is controlled by the internal circuit. The flip-flop is asynchronously set with High output, when power is applied or when global set/reset (GSR) is active. The GSR active level is programmable. When the CE pin is Low, the output (Q) does not change.

This figure illustrates legal IFDXI/ILDXI combinations for XC4000E.

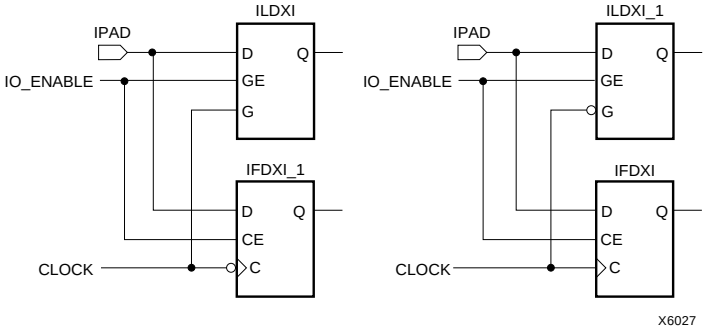


Figure 3-59 Legal Combinations of IFDXI and ILDXI for a Single XC4000E IOB

Inputs			Outputs
CE	**D**	**C**	**Q**
1	D	↓	d[a]
0	X	X	No Chg

a. d = state of referenced input one set-up time prior to active clock transition

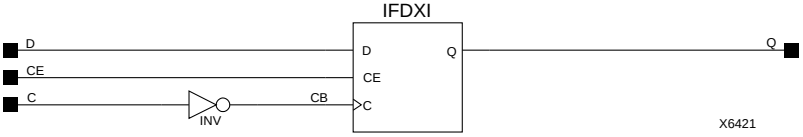


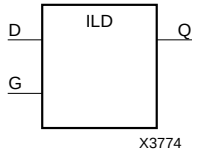
Figure 3-60 IFDXI_1 XC4000E Implementation

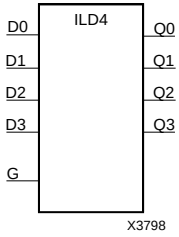
ILD, ILD4, ILD8, and ILD16

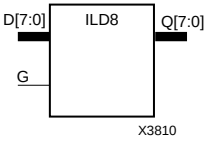
Input Transparent Data Latches

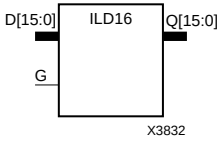
Element	XC3000	XC4000	XC4000E	XC5200	XC7000[a]
ILD	Primitive	Macro	Macro	Macro	Primitive
ILD4, ILD8, ILD16	Macro	Macro	Macro	Macro	Macro

a. not supported for XC7336 designs









ILD, ILD4, ILD8, and ILD16 are single or multiple transparent data latches, which can be used to hold transient data entering a chip. The latch input (D) is connected to an IPAD or an IOPAD (without using an IBUF). When the gate input (G) is High, data on the inputs (D) appears on the outputs (Q). Data on the D inputs during the High-to-Low G transition is stored in the latch. For XC7000 EPLDs, the gate input (G) must be driven by a FastCLK, represented by the BUFG symbol.

The latch is reset with Low output, when power is applied or when global reset (GR) for XC3000 and 5200 or global set/reset (GSR) for XC4000/4000E is active. GR is active-Low; the GSR active level is programmable. For XC7000 EPLDs (except XC7272), the latches are set High when power is applied.

XC4000/4000E ILD

The XC4000/4000E ILD is actually the input flip-flop master latch. It is possible to access two different outputs from the input flip-flop: one that responds to the level of the clock signal and another that responds to an edge of the clock signal. When using both outputs from the same input flip-flop, a transparent High latch (ILD) corresponds to a falling edge-triggered flip-flop (IFD_1). Similarly, a transparent Low latch (ILD_1) corresponds to a rising edge-triggered flip-flop (IFD).

This figure illustrates XC4000/4000E legal IFD/ILD combinations.

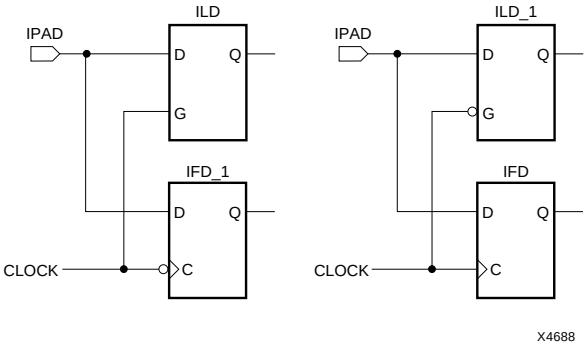


Figure 3-61 Legal Combinations of IFD and ILD for a Single XC4000/4000E IOB

XC3000 ILD

The XC3000 ILD is actually the input flip-flop master latch. If both ILD and IFD elements are controlled by the same clock signal, the relationship between the transparent sense of the latch and the active edge of the flip-flop is fixed as follows: a transparent High latch (ILD) corresponds to a falling edge-triggered flip-flop (IFD_1), and a transparent Low latch (ILD_1) corresponds to a rising edge-triggered flip-flop (IFD). Because the place and route software does not support using both phases of a clock for IOBs on a single edge of the device, certain combinations of ILD and IFD elements are not allowed. Refer to the "Legal Combinations of IFD and ILD for a Single Device Edge of XC3000 IOB" illustration for XC3000 legal IFD/ILD combinations.

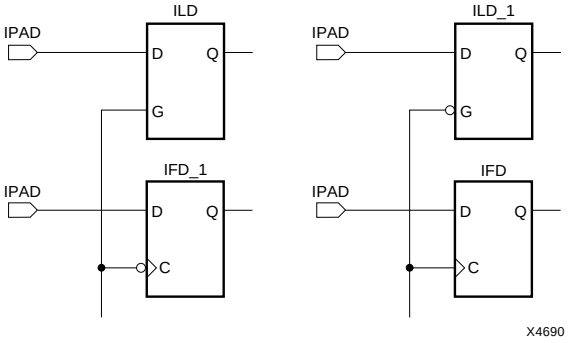


Figure 3-62 Legal Combinations of IFD and ILD for a Single Device Edge of XC3000 IOB

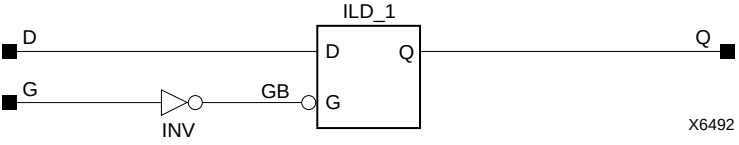


Figure 3-63 ILD XC4000/4000E Implementation

Inputs		Outputs
G	**D**	**Q**
1	1	1
1	0	0
↓	D	d[a]

a. d = state of referenced input one set-up time prior to High-to-Low gate transition

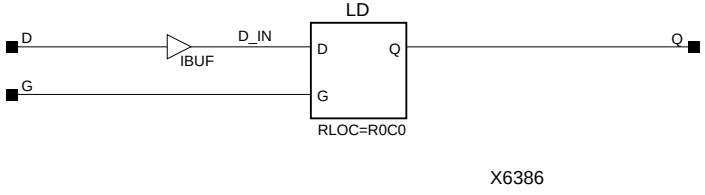
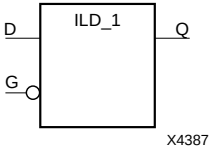


Figure 3-64 ILD XC5200 Implementation

ILD_1

Transparent Input Data Latch with Inverted Gate



XC3000	XC4000	XC4000E	XC5200
Macro	Primitive	Macro	Macro

ILD_1 is a transparent data latch, which can be used to hold transient data entering a chip. When the gate input (G) is Low, data on the data input (D) appears on the data output (Q). Data on D during the Low-to-High G transition is stored in the latch. For implementation details, refer to the "ILD, ILD4, ILD8, and ILD16" section.

The latch is reset with Low output, when power is applied or when global reset (GR) for XC3000 and 5200 or global set/reset (GSR) for XC4000/4000E is active. GR is active-Low; the GSR active level is programmable.

These figures illustrate legal IFD/ILD combinations for XC3000 and XC4000/4000E, respectively.

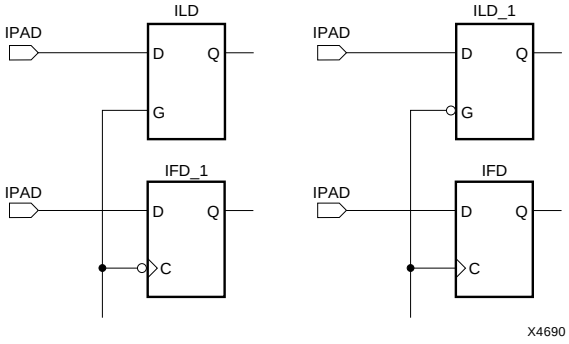


Figure 3-65 Legal Combinations of IFD and ILD for a Single Device Edge of XC3000 IOB

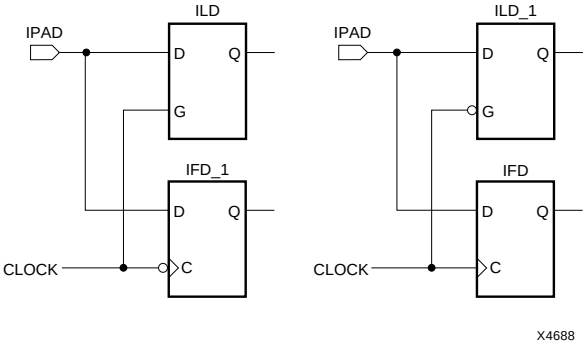


Figure 3-66 Legal Combinations of IFD and ILD for a Single XC4000/4000E IOB

Inputs		Outputs
G	**D**	**Q**
0	1	1
0	0	0
↑	D	d[a]

a. d = state of referenced input one set-up time prior to Low-to-High gate transition

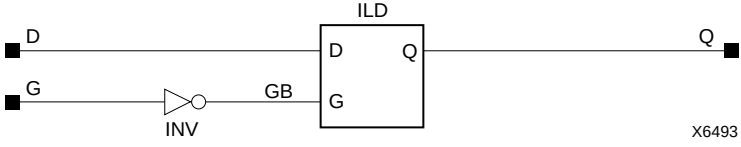


Figure 3-67 ILD_1 XC3000 Implementation

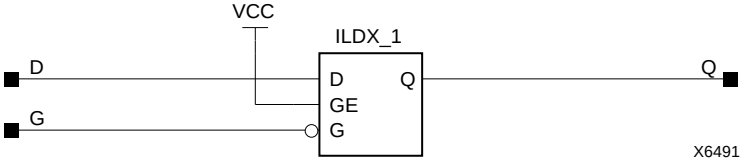


Figure 3-68 ILD_1 XC4000/4000E Implementation

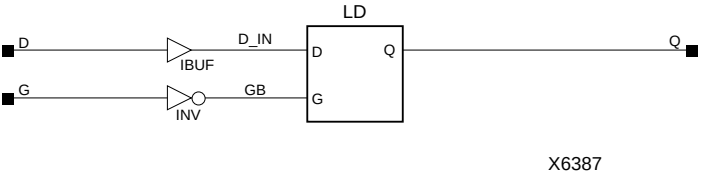
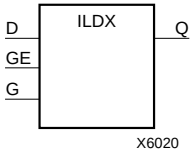
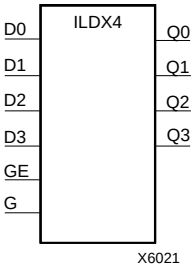


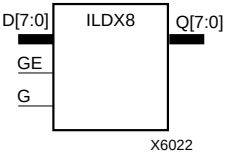
Figure 3-69 ILD_1 XC5200 Implementation

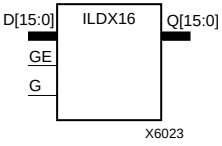
ILDX, ILDX4, ILDX8, and ILDX16

Input Transparent Data Latches









Element	XC4000E	XC5200
ILDX, ILDX4, ILDX8, ILDX16	Macro	N/A

ILDX, ILDX4, ILDX8, and ILDX16 are single or multiple transparent data latches, which can be used to hold transient data entering a chip. The latch input (D) is connected to an IPAD or an IOPAD (without using an IBUF). When the gate input (G) is High, data on the inputs (D) appears on the outputs (Q). Data on the D inputs during the High-to-Low G transition is stored in the latch.

The latch is reset, output Low, when power is applied or when global set/reset (GSR) is active. The GSR active level is programmable.

XC4000E ILDX

The XC4000E ILDX is actually the input flip-flop master latch. Two different outputs can be accessed from the input flip-flop: one that responds to the level of the clock signal and another that responds to an edge of the clock signal. When using both outputs from the same input flip-flop, a transparent High latch (ILDX) corresponds to a falling edge-triggered flip-flop (IFDX_1). Similarly, a transparent Low latch (ILDX_1) corresponds to a rising edge-triggered flip-flop (IFDX).

This figure illustrates XC4000E legal IFDX/ILDX combinations.

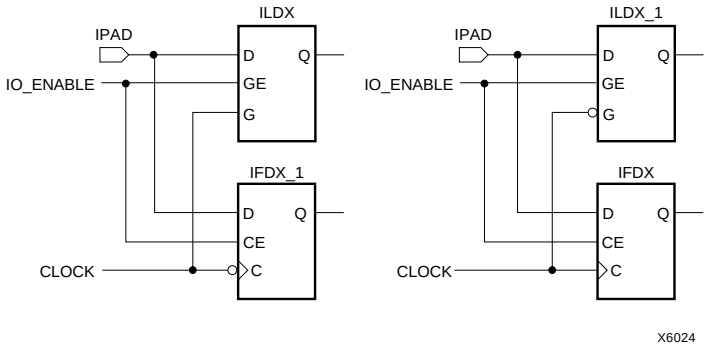


Figure 3-70 Legal Combinations of IFDX and ILDX for a Single XC4000E IOB

Inputs		Outputs
GE	**G**	**Q**
1	1	D
1	0	D
0	1	No Chg
0	0	No Chg

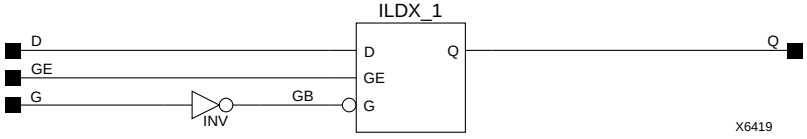


Figure 3-71 ILDX XC4000E Implementation

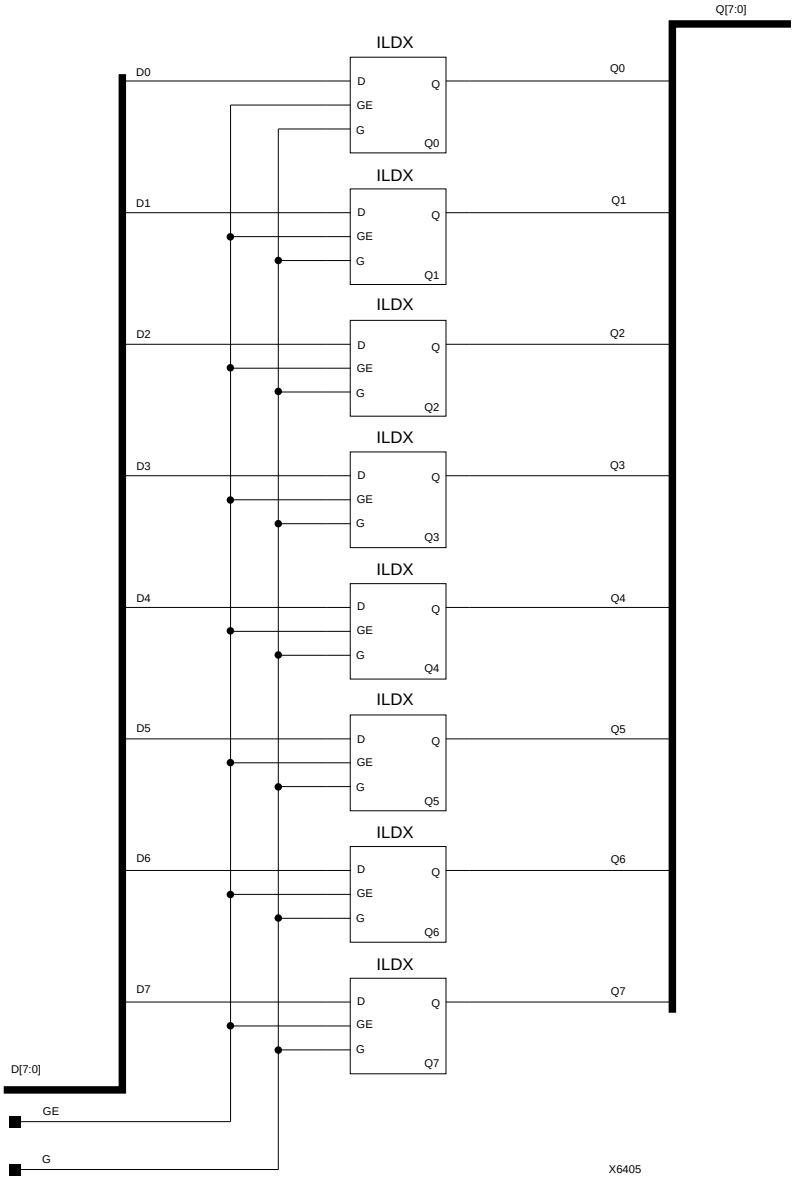
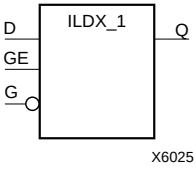


Figure 3-72 ILDX8 XC4000E Implementation

ILDX_1

Transparent Input Data Latch with Inverted Gate



XC4000E	XC5200
Primitive	N/A

ILDX_1 is a transparent data latch, which can be used to hold transient data entering a chip. When the gate input (G) is Low, data on the data input (D) appears on the data output (Q). Data on D during the Low-to-High G transition is stored in the latch. For implementation details, refer to the "ILDX, ILDX4, ILDX8, and ILDX16" section.

The latch is reset with Low output, when power is applied or when global set/reset (GSR) is active. The GSR active level is programmable.

This figure illustrates legal IFDX/ILDX combinations for XC4000E.

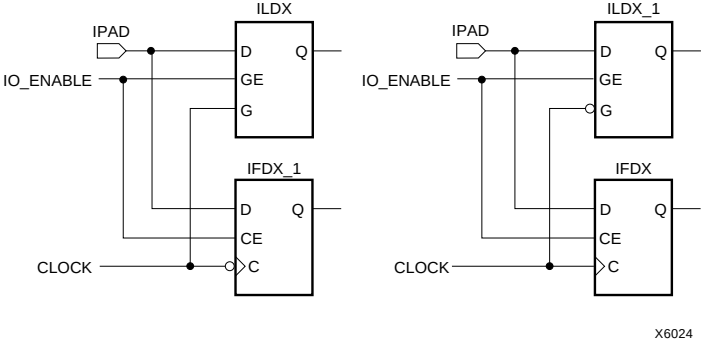


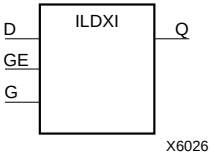
Figure 3-73 Legal Combinations of IFDX and ILDX for a Single XC4000E IOB

Inputs		Outputs
GE	G	Q
1	0	D[a]
1	1	D
0	0	No Chg
0	1	No Chg

a. D = state of referenced input one set-up time prior to Low-to-High gate transition

ILDXI

Input Transparent Data Latch (Asynchronous Set)



XC4000E	XC5200
Macro	N/A

ILDXI is a transparent data latch, which can hold transient data entering a chip. When the gate input (G) is High, data on the input (D) appears on the output (Q). Data on the D input during the High-to-Low G transition is stored in the latch.

The ILDXI is actually the input flip-flop master latch. Two different outputs can be accessed from the input flip-flop: one that responds to the level of the clock signal and another that responds to an edge of the clock signal. When using both outputs from the same input flip-flop, a transparent High latch (ILDXI) corresponds to a falling edge-triggered flip-flop (IFDXI_1). Similarly, a transparent Low latch (ILDXI_1) corresponds to a rising edge-triggered flip-flop (IFDXI). This figure illustrates legal IFDXI/ILDXI combinations for XC4000E.

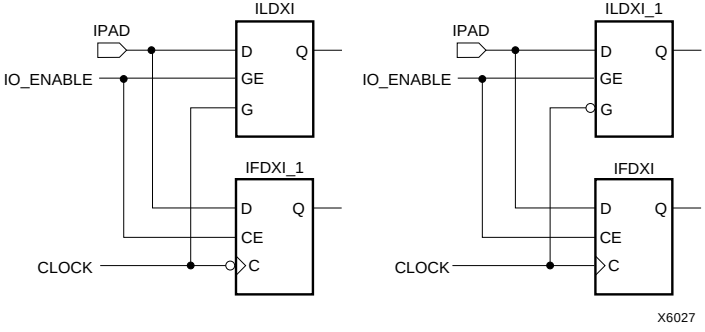


Figure 3-74 Legal Combinations of IFDXI and ILDXI for a Single XC4000E IOB

The latch is set, output High, when power is applied or when global set/reset (GSR) is active. The GSR active level is programmable.

Inputs		Outputs
GE	G	Q
1	1	D[a]
1	0	D
0	1	No Chg
0	0	No Chg

a. D = state of referenced input one set-up time prior to High-to-Low gate transition

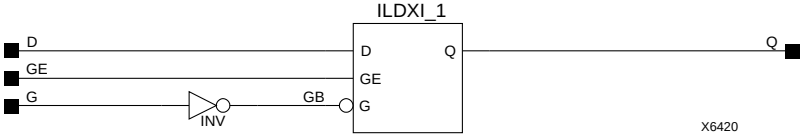
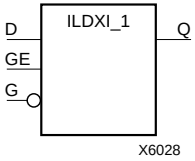


Figure 3-75 ILDXI XC4000E Implementation

ILDXI_1

Transparent Input Data Latch with Inverted Gate (Asynchronous Set)



XC4000E	XC5200
Primitive	N/A

ILDIX_1 is a transparent data latch, which can hold transient data entering a chip. When the gate input (G) is Low, data on the data input (D) appears on the data output (Q). Data on D during the Low-to-High G transition is stored in the latch. For implementation details, refer to the "ILDX, ILDX4, ILDX8, and ILDX16" section.

The latch is set, output High, when power is applied or when global set/reset (GSR) is active. The GSR active level is programmable.

This figure illustrates legal IFDXI/ILDXI combinations XC4000E.

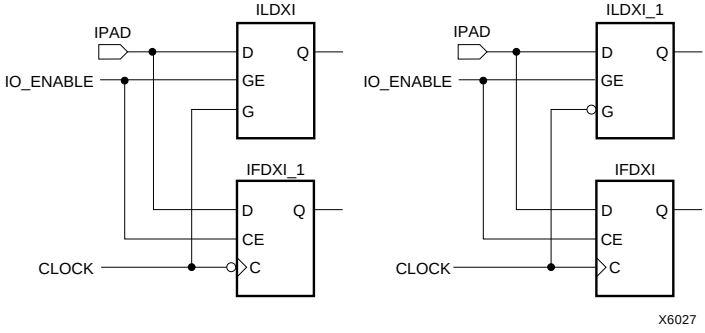


Figure 3-76 Legal Combinations of IFDXI and ILDXI for a Single XC4000E IOB

Inputs		Outputs
GE	G	Q
1	0	D[a]
1	1	D
0	0	No Chg
0	1	No Chg

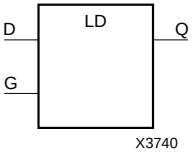
a. D = state of referenced input one set-up time prior to Low-to-High gate transition

LD, LD4, LD8, and LD16

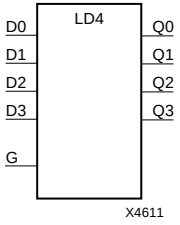
Single and Multiple Transparent Data Latches

Element	XC2000	XC4000E	XC5200	XC7000[a]
LD	Macro	N/A	Macro	Primitive
LD4, LD8, LD16	N/A	N/A	N/A	Primitive

a. not supported for XC7336 designs



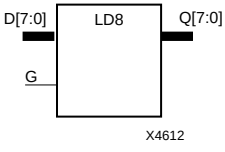
The data output (Q) of the latch reflects the data (D) input while the gate enable (G) input is High. The data on the D input during the High-to-Low gate transition is stored in the latch. The data on the Q output remains unchanged as long as G remains Low. LD4, LD8, and LD16 have 4, 8, and 16 transparent latches, respectively, with a common gate enable (G).

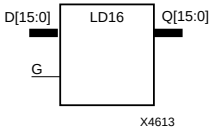


The latch is reset, output Low, when power is applied or when global reset (GR) for XC2000 and 5200 is active. For EPLD designs, the G input may not be driven by a FastCLK signal (BUFG).

Inputs		Outputs
G	D	Q
1	0	0
1	1	1
0	X	No Chg
↓	D	d[a]

a. d = state of input one set-up time prior to High-to-Low gate transition.





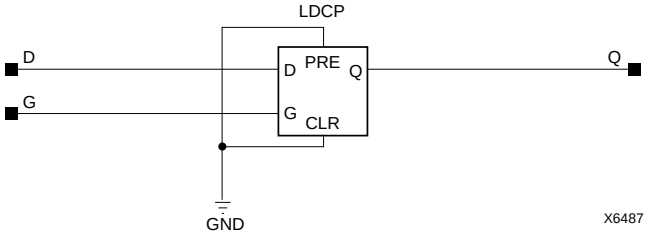


Figure 3-77 LD XC2000 Implementation

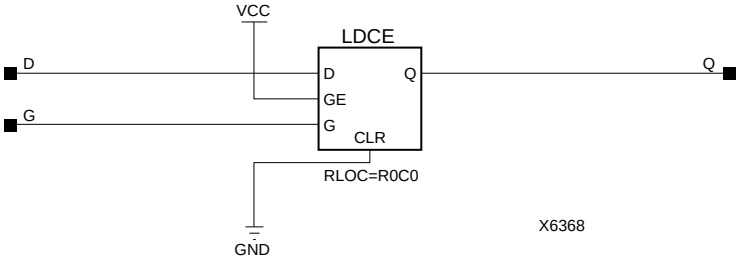
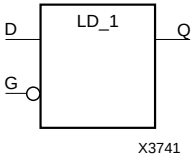


Figure 3-78 LD XC5200 Implementation

LD_1

Transparent Data Latch with Inverted Gate



XC2000	XC4000E	XC5200
Macro	N/A	Macro

The data output (Q) of the latch reflects the data (D) input while the gate enable (G) input is Low. The data on the D input during the Low-to-High gate transition is stored in the latch. The data on the Q output remains unchanged as long as G remains High.

The latch is reset with Low output, when power is applied or when global reset (GR) is active.

Inputs		Outputs
G	D	Q
0	0	0
0	1	1
1	X	No Chg
↑	D	d[a]

a. d = state of input one set-up time prior to Low-to-High gate transition

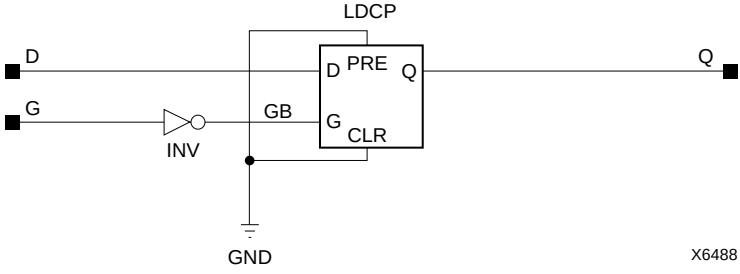


Figure 3-79 LD_1 XC2000 Implementation

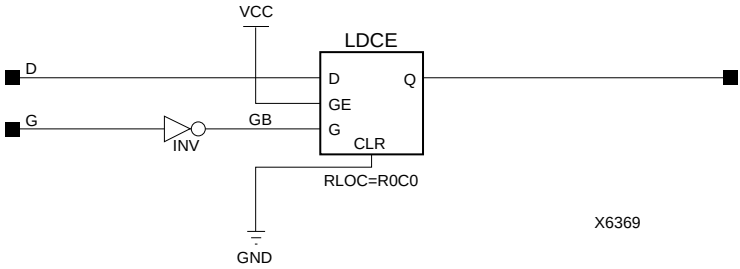
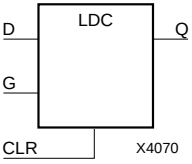


Figure 3-80 LD_1 XC5200 Implementation

LDC

Transparent Data Latch with Asynchronous Clear



XC2000	XC4000E	XC5200
Macro	N/A	Macro

When the asynchronous clear input (CLR) is High, it overrides the other inputs and resets the data (Q) output Low. Q reflects the data (D) input while the gate enable (G) input is High and CLR is Low. The data on the D input during the High-to-Low gate transition is stored in the latch. The data on the Q output remains unchanged as long as G remains low.

The latch is reset with Low output, when power is applied or when global reset (GR) is active.

Inputs			Outputs
CLR	G	D	Q
1	X	X	0
0	1	0	0
0	1	1	1
0	0	X	No Chg
0	↓	D	d[a]

a. d = state of input one setup time prior to High-to-Low gate transition

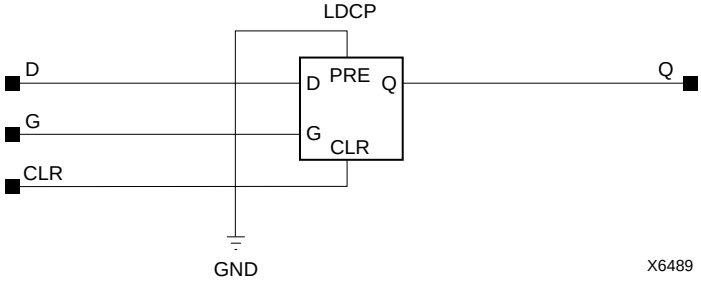


Figure 3-81 LDC XC2000 Implementation

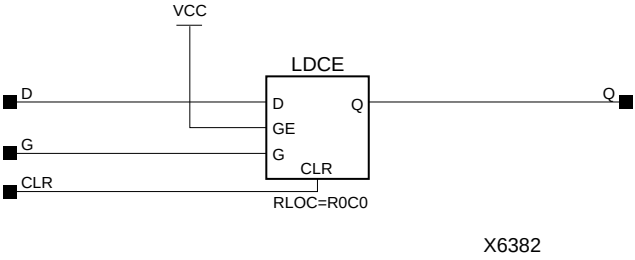
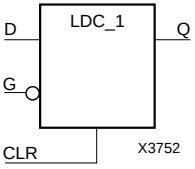


Figure 3-82 LDC XC5200 Implementation

LDC_1

Transparent Data Latch with Asynchronous Clear and Inverted Gate Input



XC2000	XC4000E	XC5200
Macro	N/A	Macro

When the asynchronous clear input (CLR) is High, it overrides the other inputs (D and G) and resets the data (Q) output Low. Q reflects the data (D) input while the gate enable (G) input and CLR are Low. The data on the D input during the Low-to-High gate transition is stored in the latch. The data on the Q output remains unchanged as long as G remains High.

The latch is reset with Low output, when power is applied or when global reset (GR) is active.

Inputs			Outputs
CLR	**G**	**D**	**Q**
1	X	X	0
0	0	0	0
0	0	1	1
0	1	X	No Chg
0	↑	D	d[a]

a. d = state of input one setup time prior to Low-to-High gate transition

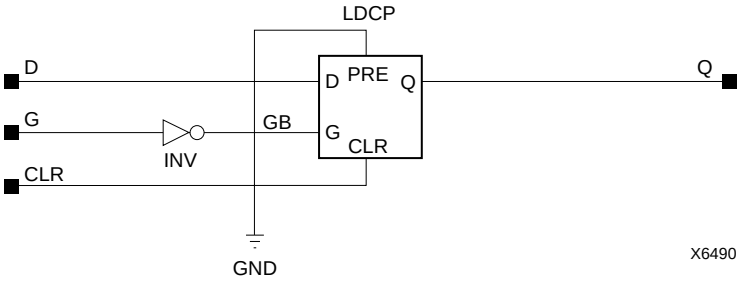


Figure 3-83 LDC_1 XC2000 Implementation

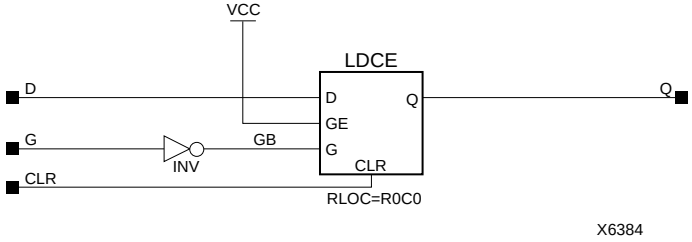
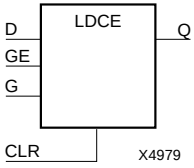


Figure 3-84 LDC_1 XC5200 Implementation

LDCE

Transparent Data Latch with Asynchronous Clear and Gate Enable



XC4000E	XC5200
N/A	Primitive

When the asynchronous clear input (CLR) is High, it overrides the other inputs and resets the data (Q) output Low. Q reflects the data (D) input while the gate (G) input and gate enable (GE) are High and CLR is Low. If GE is Low, data on D cannot be latched. The data on the D input during the High-to-Low gate transition is stored in the latch. The data on the Q output remains unchanged as long as G or GE remains low.

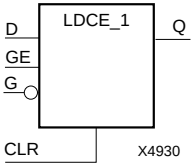
The latch is reset with Low output, when power is applied or when global reset (GR) is active.

Inputs				Outputs
CLR	**GE**	**G**	**D**	**Q**
1	X	X	X	0
0	0	X	X	No Chg
0	1	1	0	0
0	1	1	1	1
0	1	0	X	No Chg
0	1	↓	D	d[a]

a. d = state of input one setup time prior to High-to-Low gate transition

LDCE_1

Transparent Data Latch with Asynchronous Clear, Gate Enable, and Inverted Gate Input



XC4000E	XC5200
N/A	Macro

When the asynchronous clear input (CLR) is High, it overrides the other inputs and resets the data (Q) output Low. Q reflects the data (D) input while the gate (G) input and CLR are Low and gate enable (GE) is High. If GE is Low, the data on D cannot be latched. The data on the D input during the Low-to-High gate transition is stored in the latch. The data on the Q output remains unchanged as long as G remains High or GE remains Low.

The latch is reset with Low output, when power is applied or when global reset (GR) is active.

Inputs				Outputs
CLR	GE	G	D	Q
1	X	X	X	0
0	0	X	X	No Chg
0	1	0	0	0
0	1	0	1	1
0	1	1	X	No Chg
0	1	↑	D	d[a]

a. d = state of input one setup time prior to Low-to-High gate transition

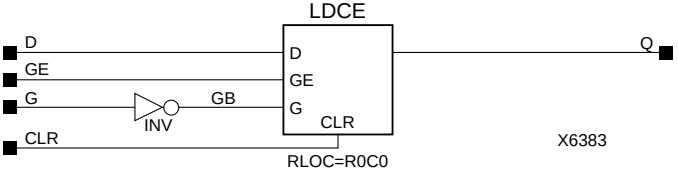


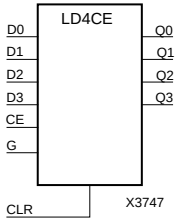
Figure 3-85 LDCE_1 XC5200 Implementation

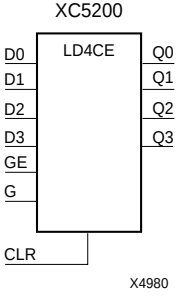
LD4CE, LD8CE, and LD16CE

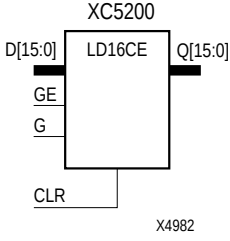
Transparent Data Latches with Asynchronous Clear and Clock Enable

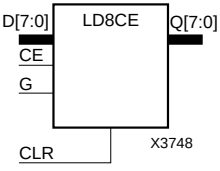
Element	XC2000	XC4000E	XC5200
LD4CE, LD8CE, LD16CE	Macro	N/A	Macro

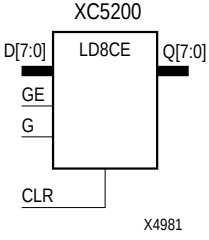
LD4CE, LD8CE, and LD16CE have 4, 8, and 16 transparent data latches, respectively. When the asynchronous clear input (CLR) is High, it overrides the other inputs and resets the data (Q) outputs Low. Q reflects the data (D) inputs while the gate (G) input is High; gate enable (CE for XC2000, GE for XC5200) is High; and CLR is Low. If CE for XC2000 or GE for XC5200 is Low, data on D cannot be latched. The data on the D input during the High-to-Low gate transition is stored in the latch. The data on the Q output remains unchanged as long as G or CE for XC2000/GE for XC5200 remains Low.

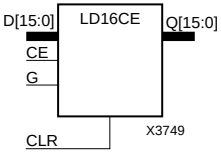












The latch is reset with Low output, when power is applied or when global reset (GR) is active.

Inputs				Outputs
CLR	CE or GE for XC5200	G	Dn[a]	Qn[b]
1	X	X	X	0
0	0	X	X	No Chg
0	1	1	1	1
0	1	1	0	0
0	1	0	X	No Chg
0	1	↓	Dn	dn[c]

a. Dn = referenced input, for example, D0, D1, D2
b. Qn = referenced output, for example, Q0, Q1, Q2
c. dn = referenced input state, one set-up time prior to High-to-Low gate transition

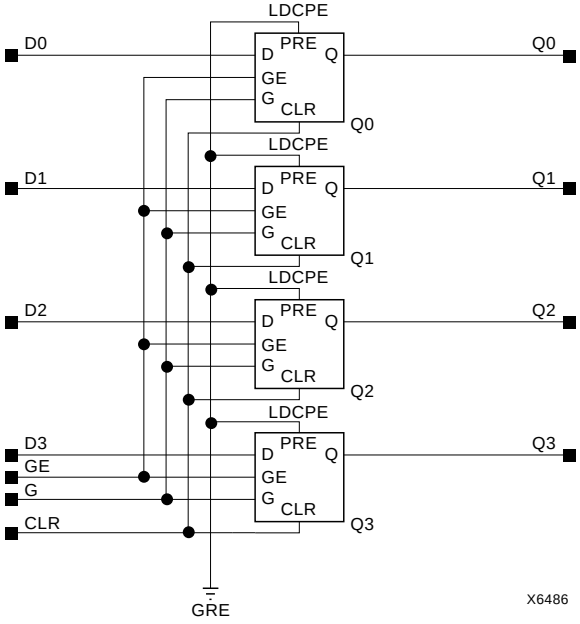


Figure 3-86 LD4CE XC2000 Implementation

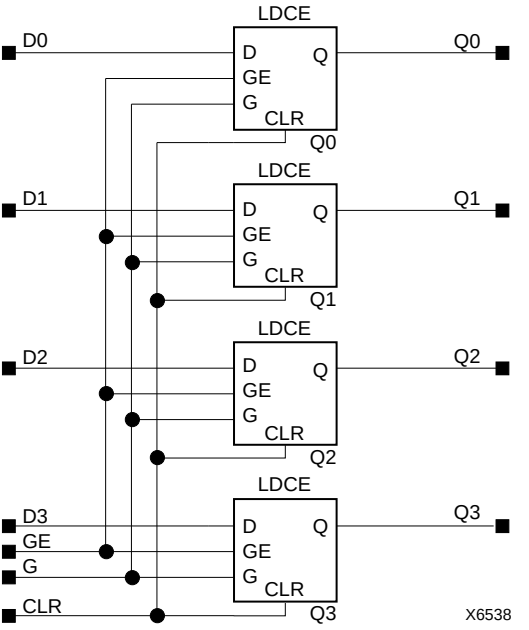


Figure 3-87 LD4CE XC5200 Implementation

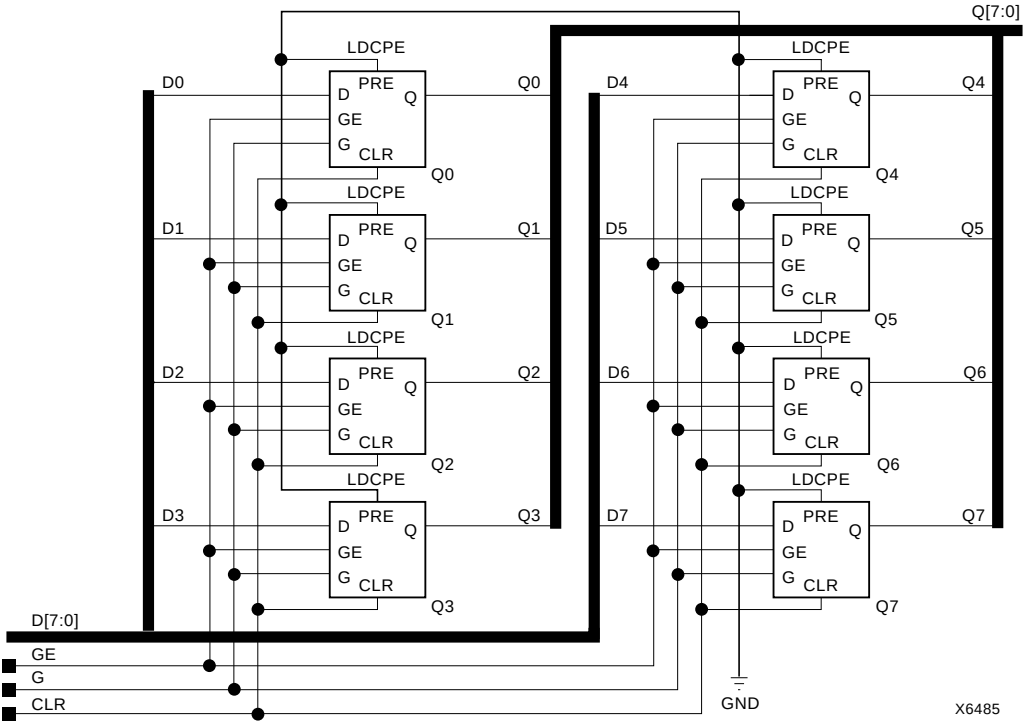


Figure 3-88 LD8CE XC2000 Implementation

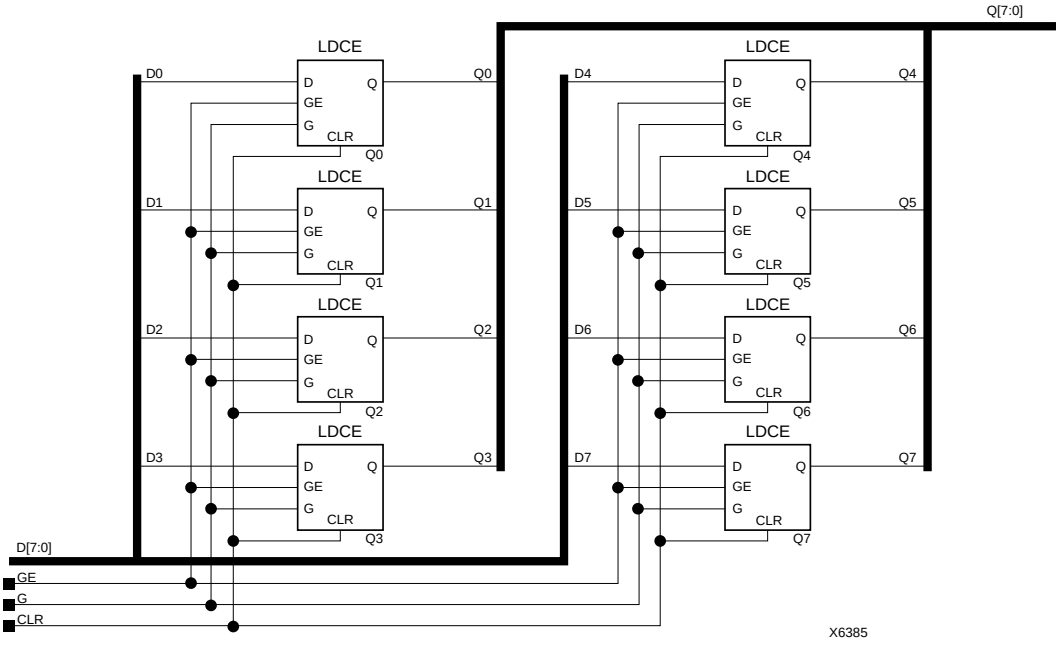


Figure 3-89 LD8CE XC5200 Implementation

NAND

2- to 9-Input NAND Gates with Inverted and Non-Inverted Inputs

Name	XC2000	XC3000	XC4000	XC4000E	XC5200	XC7000
NAND2 NAND2B1, NAND2B2, NAND3, NAND3B1, NAND3B2, NAND3B3, NAND4, NAND4B1, NAND4B2, NAND4B3, NAND4B4	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
NAND5, NAND5B1, NAND5B2, NAND5B3, NAND5B4, NAND5B5	Macro	Primitive	Primitive	Primitive	Macro	Primitive
NAND6, NAND7, NAND8, NAND9	Macro	Macro	Macro	Macro	Macro	Macro
NAND12, NAND16	N/A	N/A	N/A	N/A	Macro	N/A

The NAND function is performed in the Configurable Logic Block (CLB) function generators for XC2000, XC3000, XC4000/4000E, and XC5200. NAND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND functions of six to nine inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Since each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

The 12- and 16-input NAND functions are available only with non-inverting inputs. To invert some or all inputs, use external inverters.

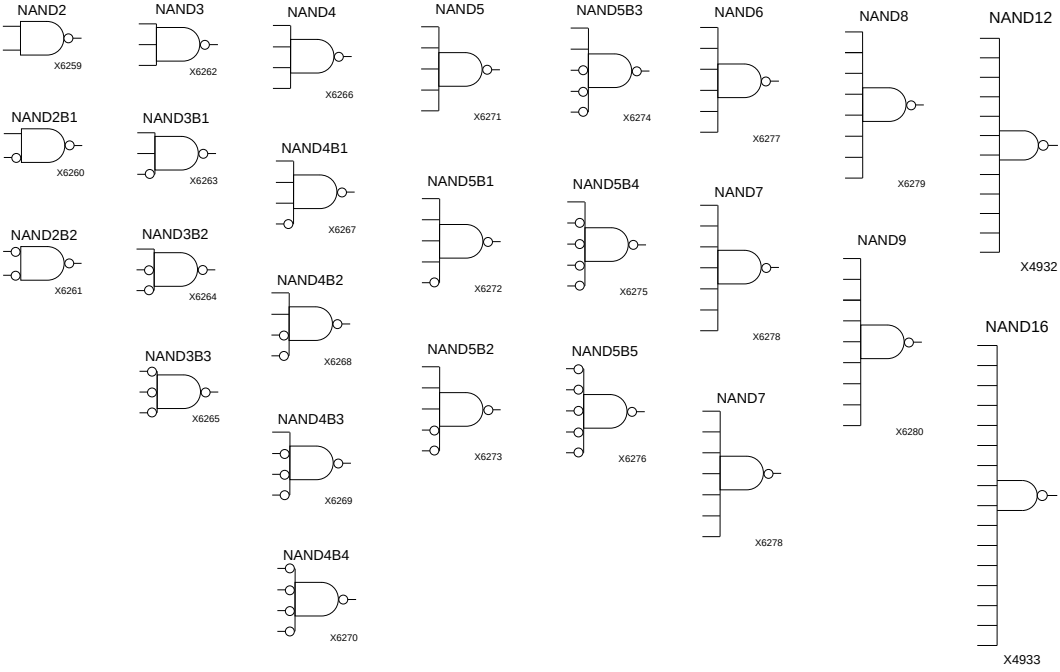


Figure 3-90 NAND Gate Representations

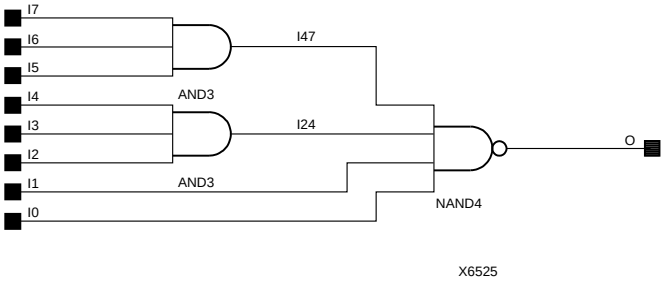


Figure 3-91 NAND8 XC2000 Implementation

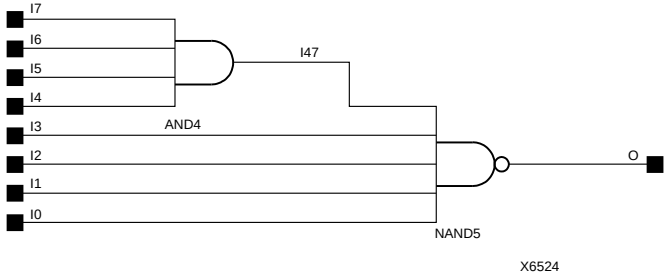


Figure 3-92 NAND8 XC3000 Implementation

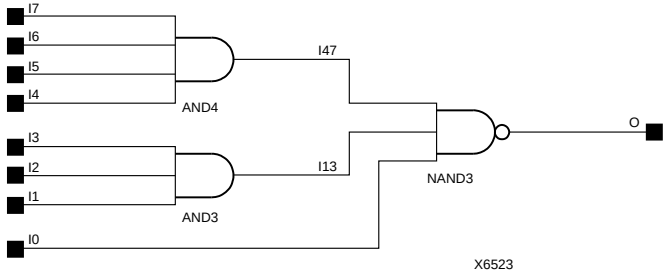


Figure 3-93 NAND8 XC4000/XC4000E Implementation

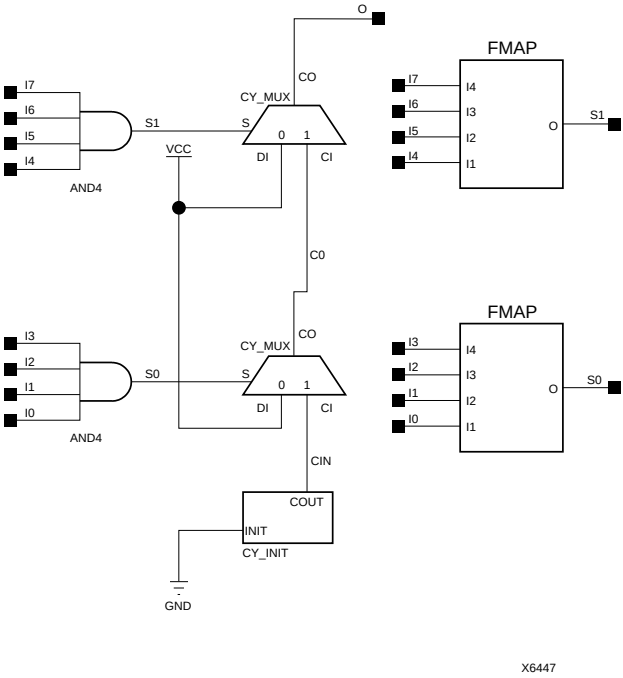


Figure 3-94 NAND8 XC5200 Implementation

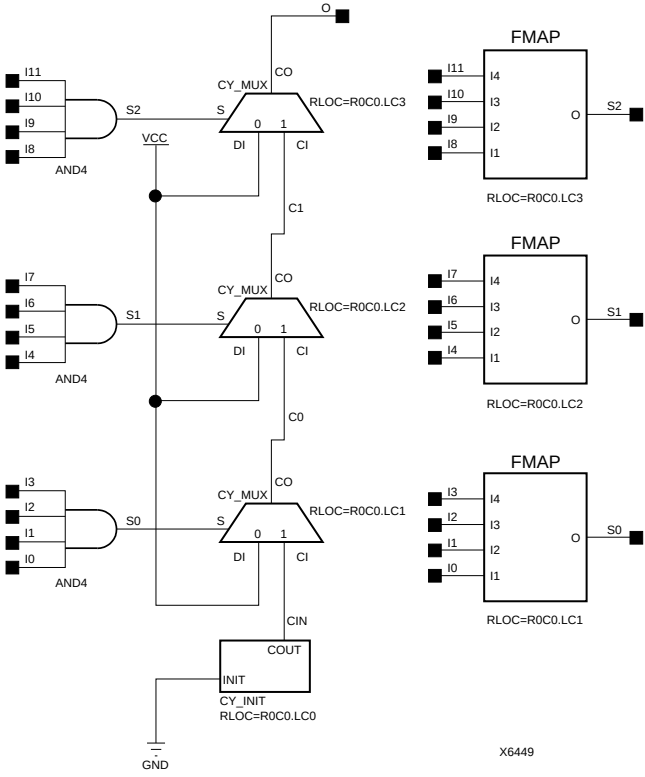


Figure 3-95 NAND12 XC5200 Implementation

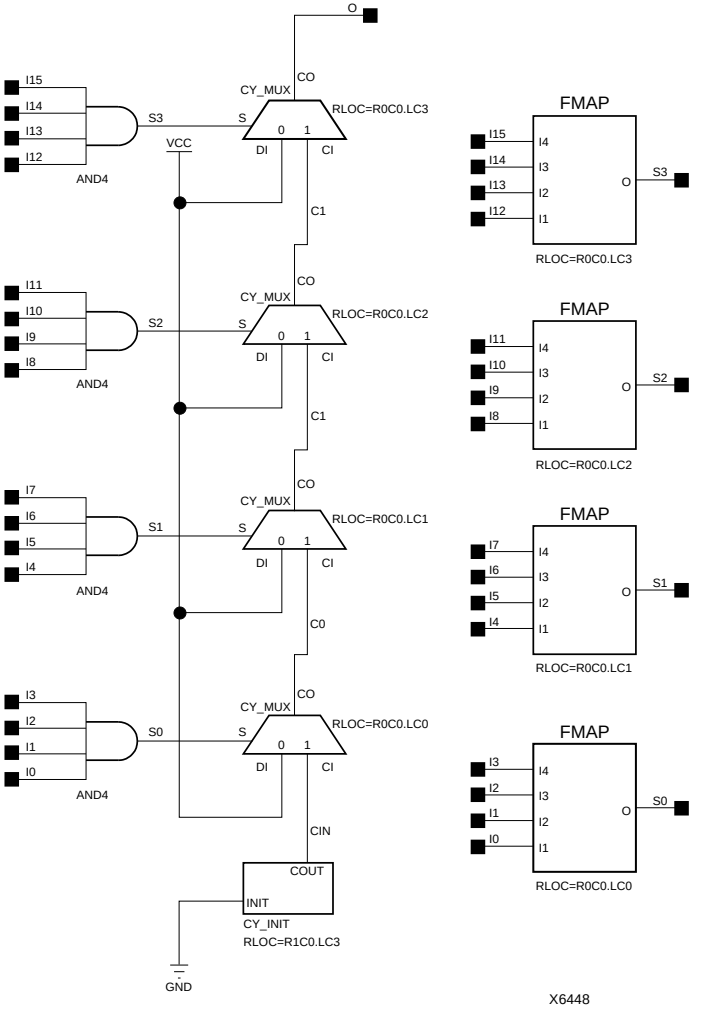


Figure 3-96 NAND16 XC5200 Implementation

NOR

2- to 9-Input NOR Gates with Inverted and Non-Inverted Inputs

Name	XC2000	XC3000	XC4000	XC4000E	XC5200	XC7000
NOR2 – NOR4B4	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
NOR5 – NOR5B5	Macro	Primitive	Primitive	Primitive	Macro	Primitive
NOR6, NOR7, NOR8, NOR9	Macro	Macro	Macro	Macro	Macro	Primitive
NOR12, NOR16	N/A	N/A	N/A	N/A	Macro	N/A

The NOR function is performed in the Configurable Logic Block (CLB) function generators for XC2000, XC3000, XC4000/4000E, and XC5200. NOR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR functions of six to nine inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Since each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

The 12- and 16-input NOR functions are available only with non-inverting inputs. To invert some or all inputs, use external inverters.

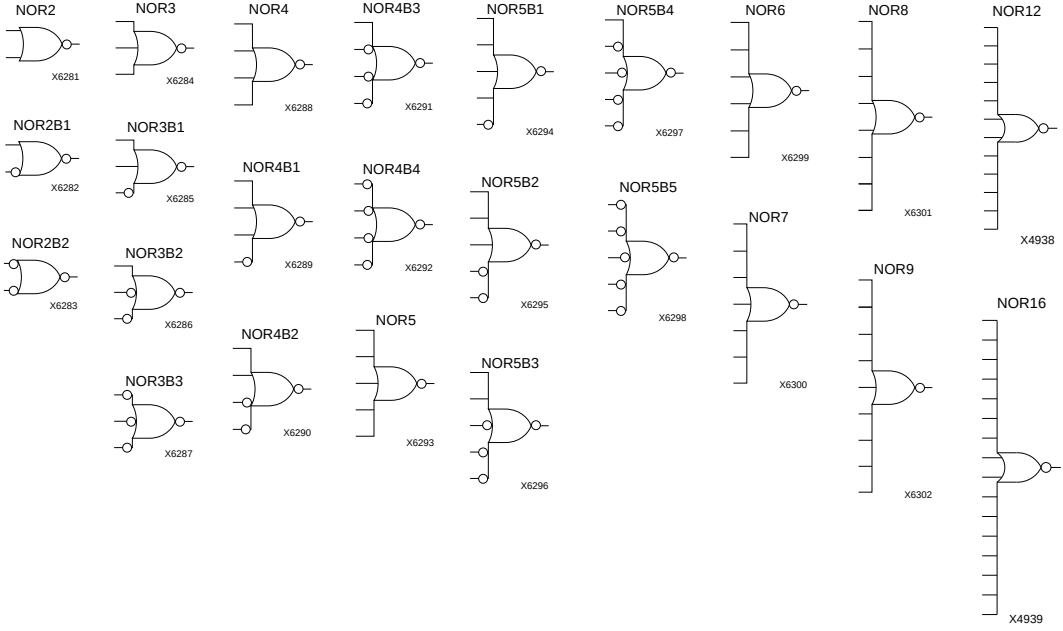


Figure 3-97 NOR Gate Representations

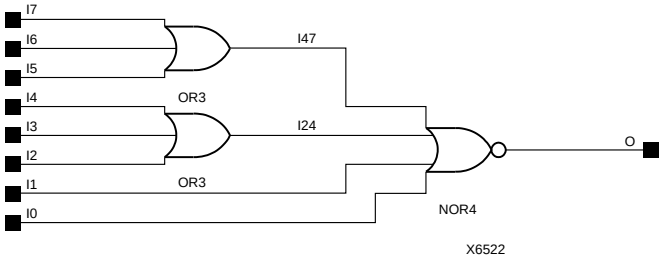


Figure 3-98 NOR8 XC2000 Implementation

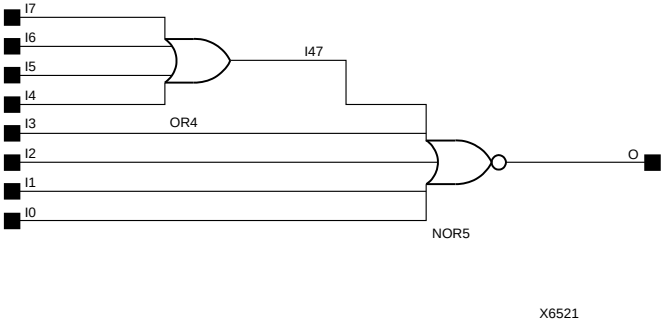


Figure 3-99 NOR8 XC3000 Implementation

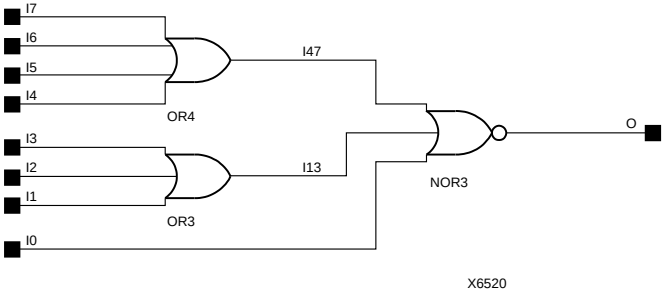


Figure 3-100 NOR8 XC4000/4000E Implementation

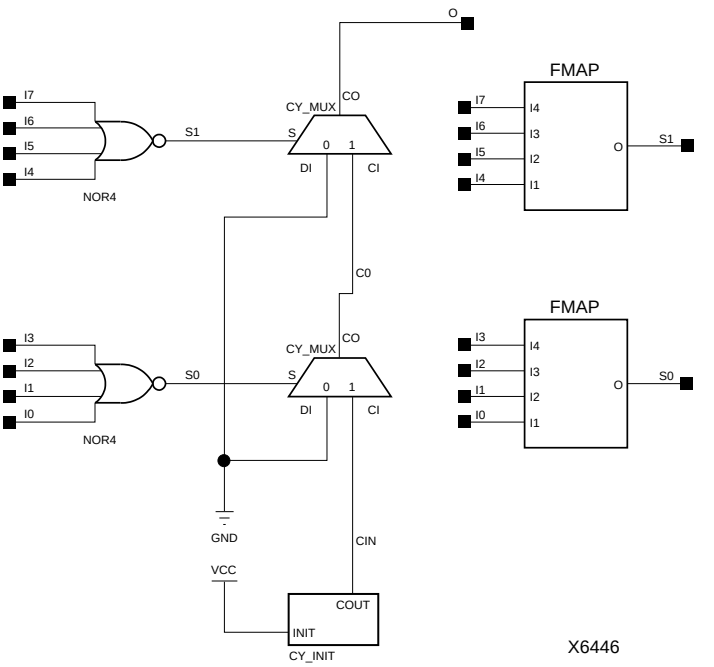


Figure 3-101 NOR8 XC5200 Implementation

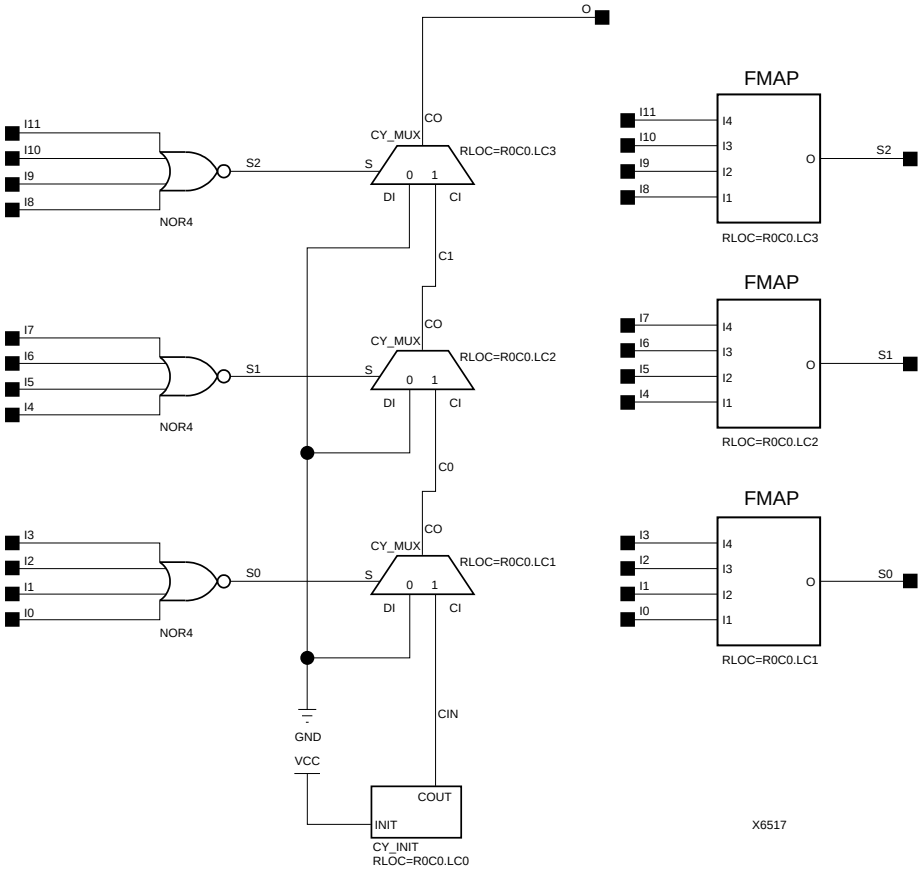


Figure 3-102 NOR12 XC5200 Implementation

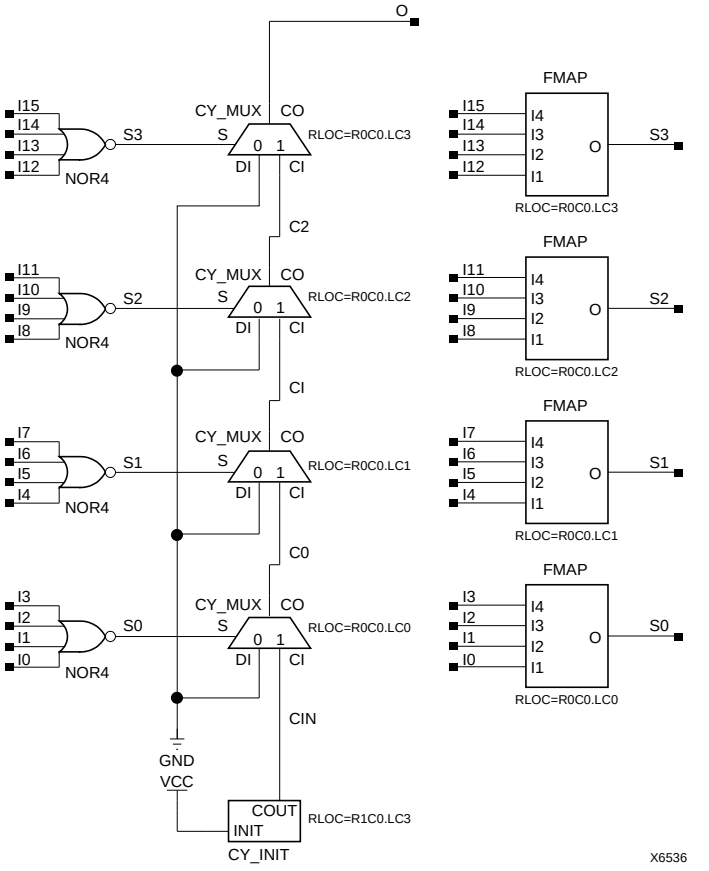
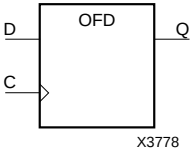


Figure 3-103 NOR16 XC5200 Implementation

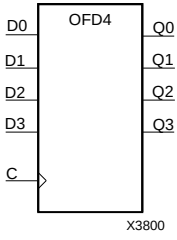
OFD, OFD4, OFD8, and OFD16

Single- and Multiple-Output D Flip-Flops

Name	XC3000	XC4000	XC4000E	XC5200	XC7000
OFD	Primitive	Primitive	Macro	Macro	Macro
OFD4, OFD8, OFD16	Macro	Macro	Macro	Macro	Macro



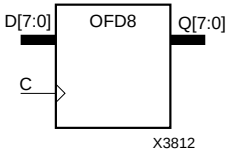
OFD, OFD4, OFD8, and OFD16 are single and multiple output D flip-flops except for XC5200. The flip-flops exist in an input/output block (IOB) for XC3000 and XC4000/4000E. The outputs (for example, Q3 – Q0) are connected to OPADs or IOPADs. The data on the D inputs is loaded into the flip-flops during the Low-to-High clock (C) transition and appears on the Q outputs.

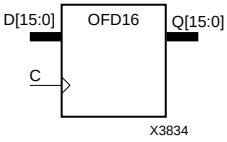


The flip-flops are asynchronously reset with Low outputs, when power is applied or when global reset (GR) for XC3000 and 5200 or global set/reset (GSR) for XC4000/4000E is active. GR is active-Low for XC3000. The GR active level is programmable for XC5200. The GSR active level is programmable for XC4000/4000E.

Inputs		Outputs
D	C	Q
D	↑	dn[a]

a. dn = state of referenced input one set-up time prior to active clock transition





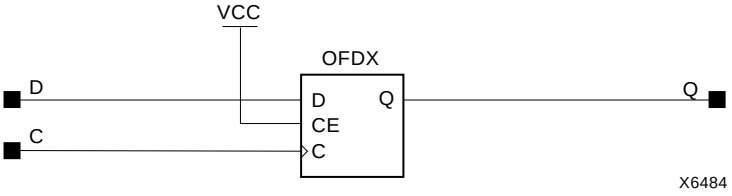


Figure 3-104 OFD XC4000E Implementation

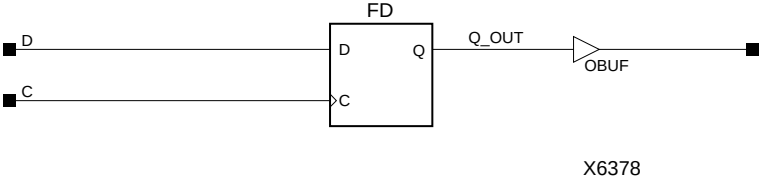


Figure 3-105 OFD XC5200 Implementation

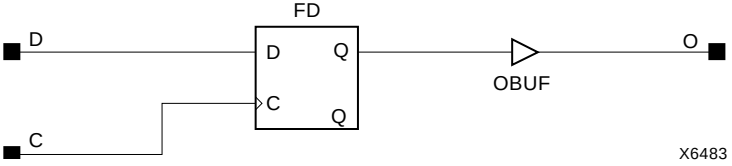


Figure 3-106 OFD XC7000 Implementation

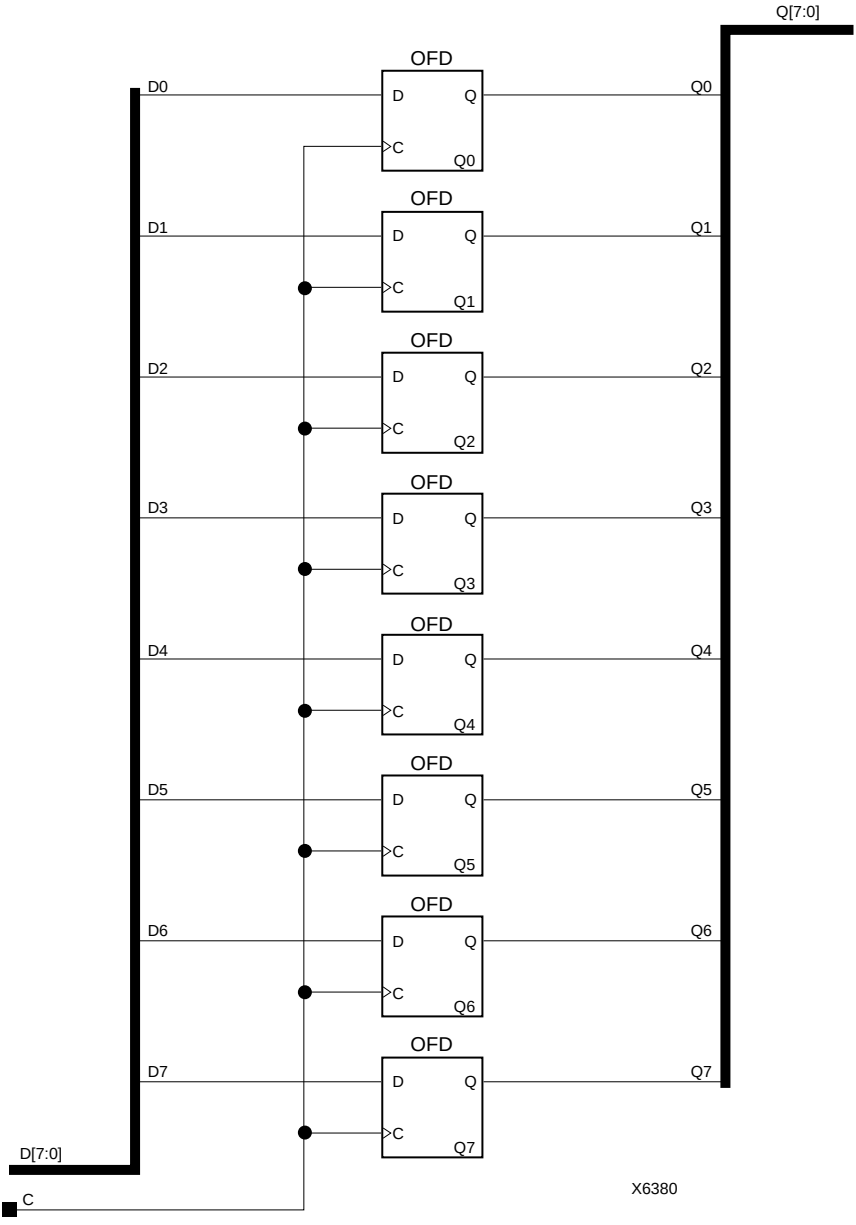


Figure 3-107 OFD8 XC3000/4000/4000E/5200 Implementation

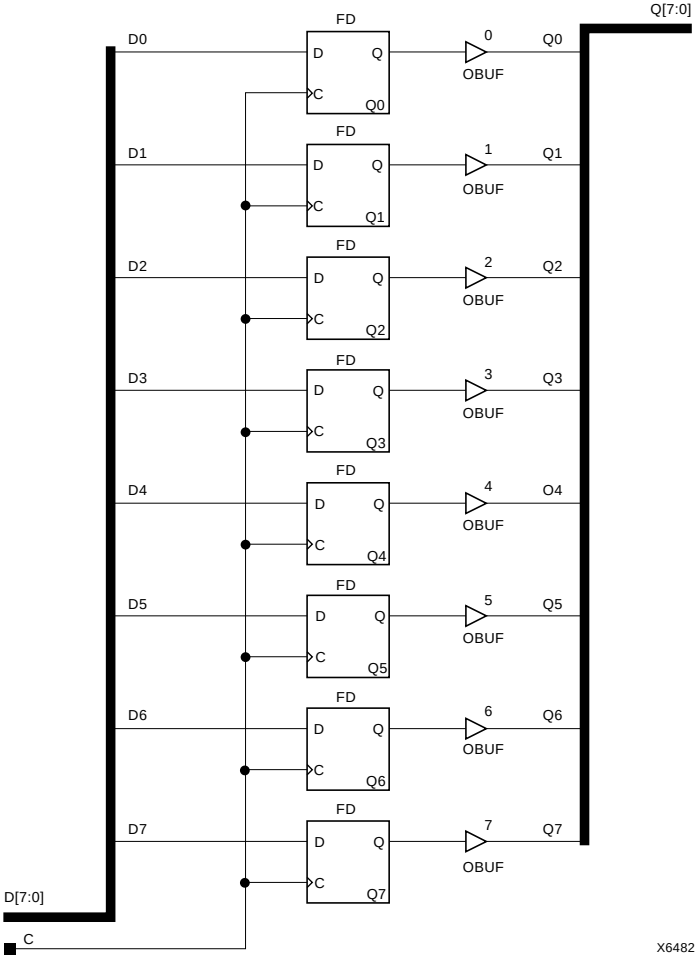
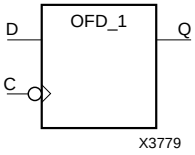


Figure 3-108 OFD8 XC7000 Implementation

OFD_1

Output D Flip-Flop with Inverted Clock



XC3000	XC4000	XC4000E	XC5200
Macro	Macro	Macro	Macro

OFD_1 is located in an input/output block (IOB) except for XC5200. The output (Q) of the D flip-flop is connected to an OPAD or an IOPAD. The data on the D input is loaded into the flip-flop during the High-to-Low clock (C) transition and appears on the Q output.

The flip-flop is asynchronously reset with Low output, when power is applied or when global reset (GR) for XC3000 and 5200 or global set/reset (GSR) for XC4000/4000E is active. GR is active-Low for XC3000. The GR active level is programmable for XC5200. The GSR active level is programmable for XC4000/4000E.

Inputs		Outputs
D	**C**	**Q**
D	↓	d[a]

a. d = state of referenced input one set-up time prior to active clock transition

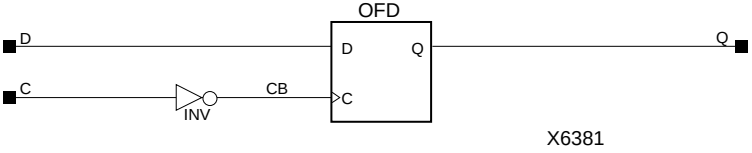
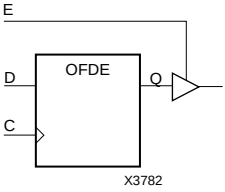


Figure 3-109 OFD_1 XC3000/4000/4000E/5200 Implementation

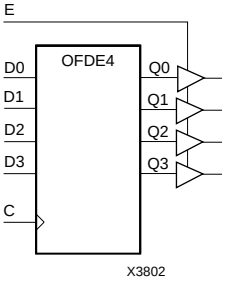
OFDE, OFDE4, OFDE8, and OFDE16

D Flip-Flops with Active-High Enable Output Buffers

Element	XC3000	XC4000	XC4000E	XC5200	XC7000
OFDE, OFDE4, OFDE8, OFDE16	Macro	Macro	Macro	Macro	Macro

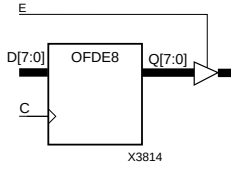


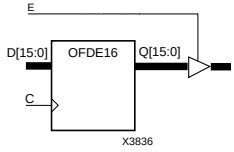
OFDE, OFDE4, OFDE8, and OFDE16 are single or multiple D flip-flops whose outputs are enabled by tristate buffers. The flip-flop data outputs (Q) are connected to the inputs of output buffers (OBUFE). The OBUFE outputs (O) are connected to OPADs or IOPADs. These flip-flops and buffers are contained in input/output blocks (IOB) for XC3000 and XC4000/4000E. The data on the data inputs (D) is loaded into the flip-flops during the Low-to-High clock (C) transition. When the active-High enable inputs (E) are High, the data on the flip-flop outputs (Q) appears on the O outputs. When E is Low, outputs are high impedance (Z state or Off).



The flip-flops are asynchronously reset with Low outputs, when power is applied or when global reset (GR) for XC3000 and 5200 or global set/reset (GSR) for XC4000/4000E is active. GR is active-Low for XC3000. The GR active level is programmable for XC5200. The GSR active level is programmable for XC4000/4000E.

Inputs			Outputs
E	**D**	**C**	**O**
0	X	X	Z, not off
1	1	↑	1
1	0	↑	0





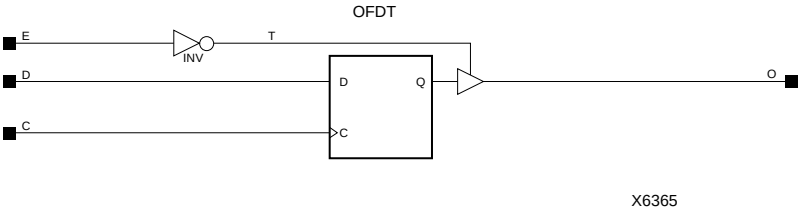


Figure 3-110 OFDE XC3000/4000/4000E/5200 Implementation

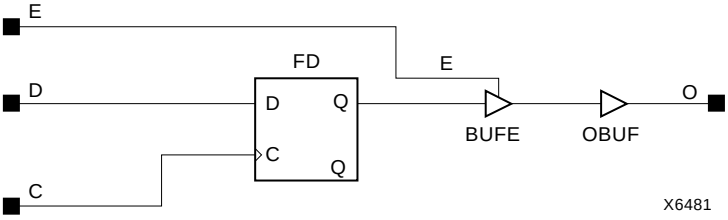


Figure 3-111 OFDE XC7000 Implementation

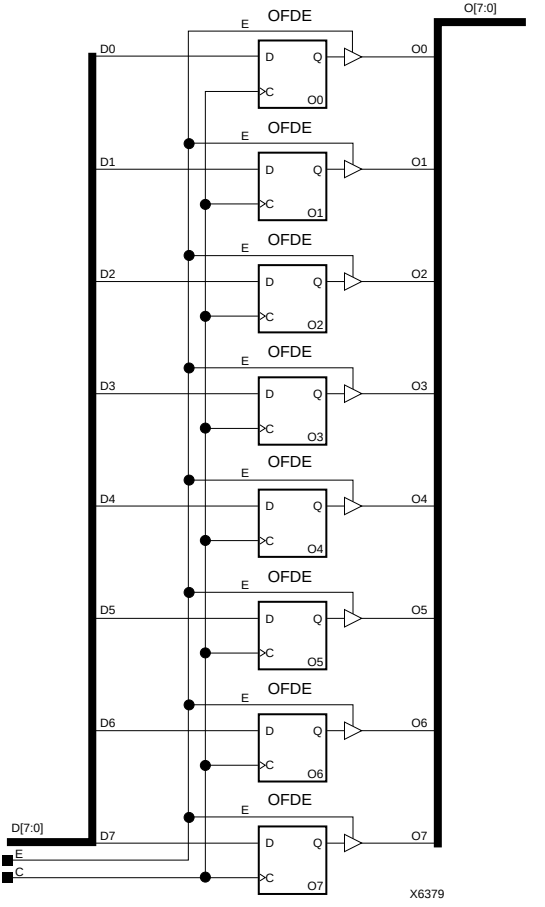


Figure 3-112 OFDE8 XC3000/4000/4000E/5200 Implementation

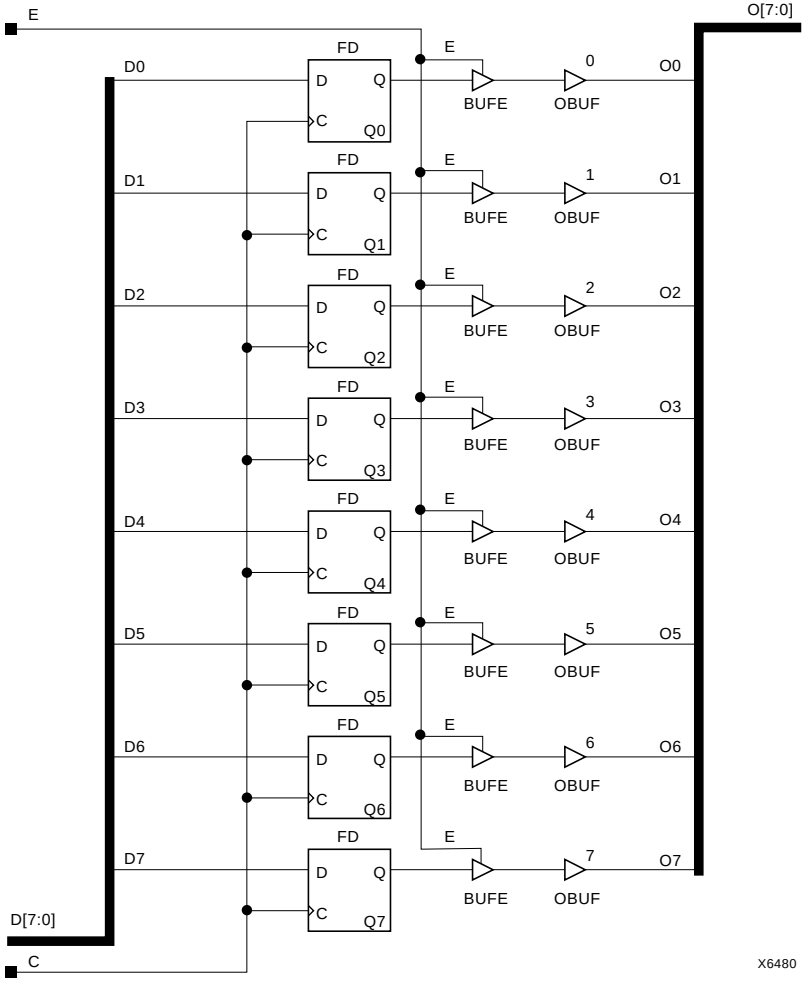
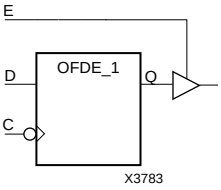


Figure 3-113 OFDE8 XC7000 Implementation

OFDE_1

D Flip-Flop with Active-High Enable Output Buffer and Inverted Clock



XC3000	XC4000	XC4000E	XC5200
Macro	Macro	Macro	Macro

OFDE_1 and its output buffer are located in an input/output block (IOB) except for XC5200. The data output of the flip-flop (Q) is connected to the input of an output buffer or OBUF. The output of the OBUF is connected to an OPAD or an IOPAD. The data on the data input (D) is loaded into the flip-flop on the High-to-Low clock (C) transition. When the active-High enable input (E) is High, the data on the flip-flop output (Q) appears on the O output. When E is Low, the output is high impedance (Z state or Off).

The flip-flop is asynchronously reset with Low output, when power is applied or when global reset (GR) for XC3000 and 5200 or global set/reset (GSR) for XC4000/4000E is active. GR is active-Low for XC3000. The GR active level is programmable for XC5200. The GSR active level is programmable for XC4000/4000E.

Inputs			Outputs
E	**D**	**C**	**O**
0	X	X	Z
1	1	↓	1
1	0	↓	0

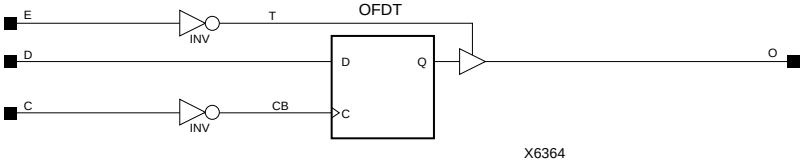
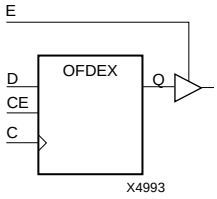


Figure 3-114 OFDE_1 XC3000/4000/4000E/5200 Implementation

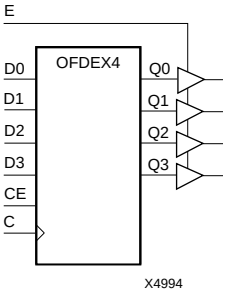
OFDEX, OFDEX4, OFDEX8, and OFDEX16

D Flip-Flops with Active-High Enable Output Buffers

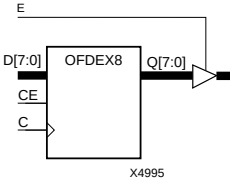


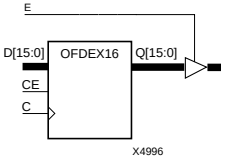
XC4000E	XC5200
Macro	N/A

OFDEX, OFDEX4, OFDEX8, and OFDEX16 are single or multiple D flip-flops whose outputs are enabled by tristate buffers. The flip-flop data outputs (Q) are connected to the inputs of output buffers (OBUFE). The OBUFE outputs (O) are connected to OPADs or IOPADs. These flip-flops and buffers are contained in input/output blocks (IOB). The data on the data inputs (D) is loaded into the flip-flops during the Low-to-High clock (C) transition. When the active-High enable inputs (E) are High, the data on the flip-flop outputs (Q) appears on the O outputs. When E is Low, outputs are high impedance (Z state or Off). When CE is Low and E is High, the outputs do not change.



The flip-flops are asynchronously reset with Low outputs, when power is applied or when global set/reset (GSR) is active. The GSR active level is programmable.





Inputs				Outputs
CE	E	D	C	O
X	0	X	X	Z, not off
1	1	1	↑	1
1	1	0	↑	0
0	1	X	X	No Chg

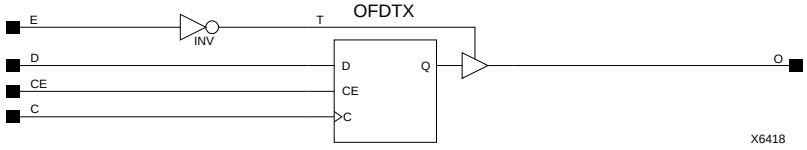


Figure 3-115 OFDEX XC4000E Implementation

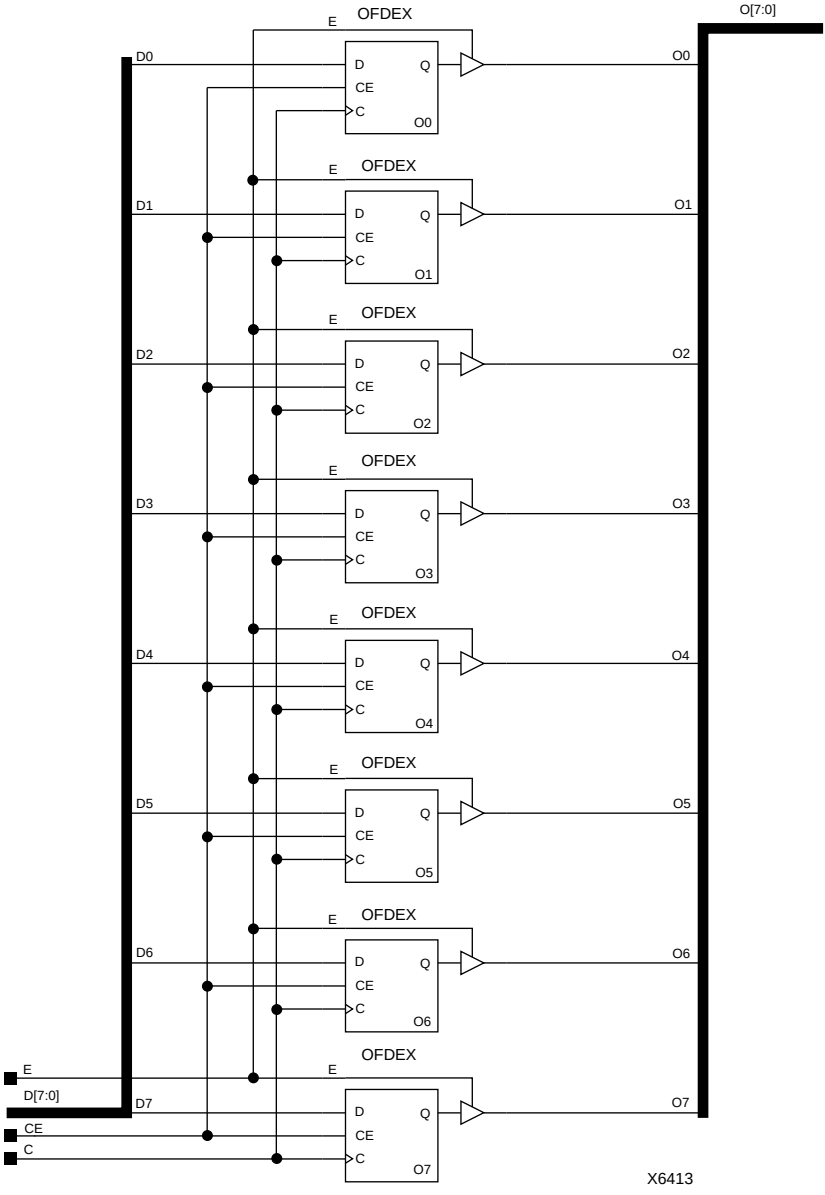
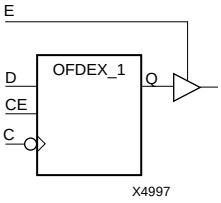


Figure 3-116 OFDEX8 XC4000E Implementation

OFDEX_1

D Flip-Flop with Active-High Enable Output Buffer and Inverted Clock



XC4000E	XC5200
Macro	N/A

OFDEX_1 and its output buffer are located in an input/output block (IOB). The data output of the flip-flop (Q) is connected to the input of an output buffer or OBUF. The output of the OBUF is connected to an OPAD or an IOPAD. The data on the data input (D) is loaded into the flip-flop on the High-to-Low clock (C) transition. When the active-High enable input (E) is High, the data on the flip-flop output (Q) appears on the Q output. When E is Low, the output is high impedance (Z state or Off). When CE is Low and E is High, the output does not change.

The flip-flop is asynchronously reset with Low output, when power is applied or when global set/reset (GSR) is active. The GSR active level is programmable.

Inputs				Outputs
CE	E	D	C	O
X	0	X	X	Z
1	1	1	↓	1
1	1	0	↓	0
0	1	X	X	No Chg

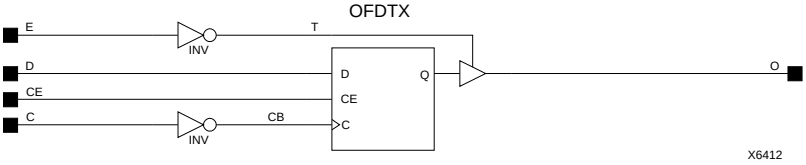
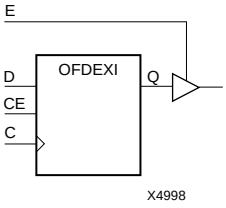


Figure 3-117 OFDEX_1 XC4000E Implementation

OFDEXI

D Flip-Flop with Active-High Enable Output Buffer (Asynchronous Set)



XC4000E	XC5200
Macro	N/A

OFDEXI is a D flip-flop whose output is enabled by a tristate buffer. The data output (Q) of the flip-flop is connected to the input of an output buffer or OBUF. The output of the OBUF (O) is connected to an OPAD or an IOPAD. These flip-flops and buffers are contained in input/output blocks (IOB). The data on the data input (D) is loaded into the flip-flop during the Low-to-High clock (C) transition. When the active-High enable input (E) is High, the data on the flip-flop output (Q) appears on the O output. When E is Low, the output is high impedance (Z state or Off). When CE is Low and E is High, the output does not change. The flip-flop is asynchronously set, output High, when power is applied or when global set/reset (GSR) is active. The GSR active level is programmable.

Inputs				Outputs
CE	E	D	C	O
X	0	X	X	Z
1	1	1	↑	1
1	1	0	↑	0
0	1	X	X	No Chg

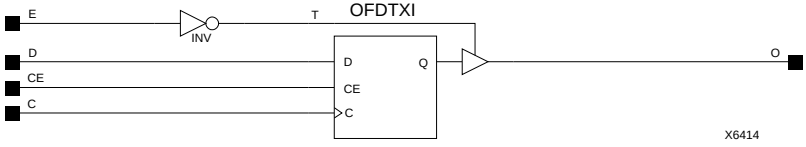
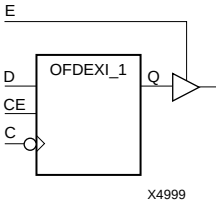


Figure 3-118 OFDEXI XC4000E Implementation

OFDEXI_1

D Flip-Flop with Active-High Enable Output Buffer and Inverted Clock (Asynchronous Set)



XC4000E	XC5200
Macro	N/A

OFDEXI_1 and its output buffer are located in an input/output block (IOB). The data output of the flip-flop (Q) is connected to the input of an output buffer or OBUF. The output of the OBUF is connected to an OPAD or an IOPAD. The data on the data input (D) is loaded into the flip-flop on the High-to-Low clock (C) transition. When the active-High enable input (E) is High, the data on the flip-flop output (Q) appears on the O output. When E is Low, the output is high impedance (Z state or Off). When CE is Low and E is High, the output does not change. The flip-flop is asynchronously set, output High, when power is applied or when global set/reset (GSR) is active. The GSR active level is programmable.

Inputs				Outputs
CE	E	D	C	O
X	0	X	X	Z
1	1	1	↓	1
1	1	0	↓	0
0	1	X	X	No Chg

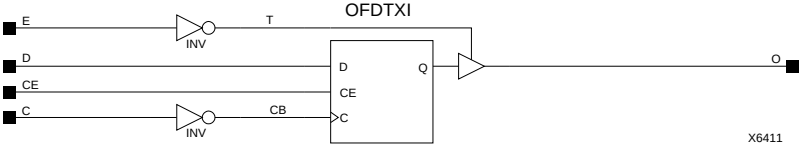


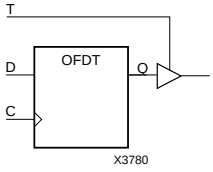
Figure 3-119 OFDEXI_1 XC4000E Implementation

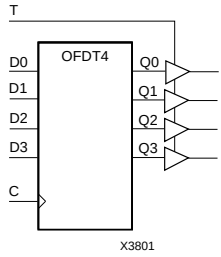
OFDT, OFDT4, OFDT8, and OFDT16

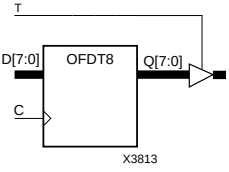
Single and Multiple D Flip-Flops with Active-High Tristate Active-Low Output Enable Buffers

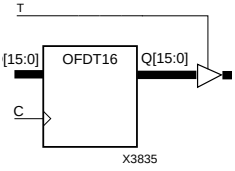
Name	XC3000	XC4000	XC4000E	XC5200	XC7000[a]
OFDT	Primitive	Primitive	Macro	Macro	Macro
OFDT4, OFDT8, OFDT16	Macro	Macro	Macro	Macro	Macro

a. not supported for XC7336 designs









OFDT, OFDT4, OFDT8, and OFDT16 are single or multiple D flip-flops whose outputs are enabled by a tristate buffers. The data outputs (Q) of the flip-flops are connected to the inputs of output buffers (OBUFT). The outputs of the OBUFTs (O) are connected to OPADs or IOPADs. These flip-flops and buffers are located in input/output blocks (IOB) for XC3000 and XC4000/4000E. The data on the data inputs (D) is loaded into the flip-flops during the Low-to-High clock (C) transition. When the active-Low enable inputs (T) are Low, the data on the flip-flop outputs (Q) appears on the O outputs. When T is High, outputs are high impedance (Off).

The flip-flops are asynchronously reset with Low outputs, when power is applied or when global reset (GR) for XC3000 and 5200 or global set/reset (GSR) for XC4000/4000E is active. GR is active-Low for XC3000. The GR active level is programmable for XC5200. The GSR active level is programmable for XC4000/4000E.

Inputs			Outputs
T	D	C	O
1	X	X	Z
0	D	↑	d[a]

a. d = state of referenced input one set-up time prior to active clock transition

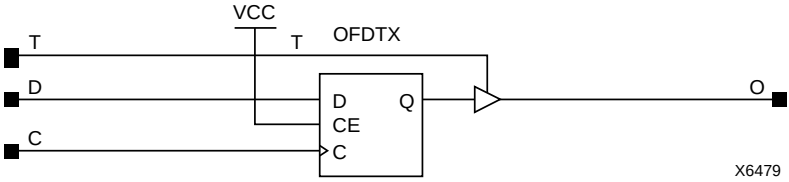


Figure 3-120 OFDT XC4000/4000E Implementation

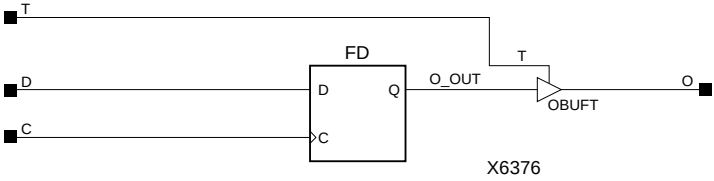


Figure 3-121 OFDT XC5200 Implementation

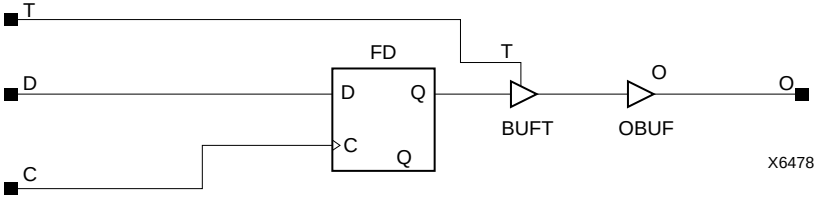


Figure 3-122 OFDT XC7000 Implementation

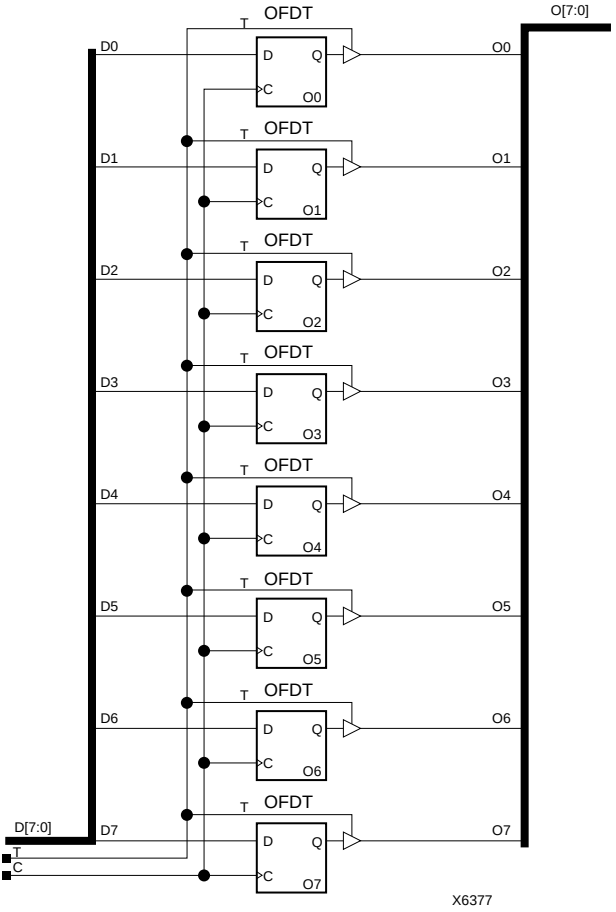


Figure 3-123 OFDT8 XC3000/4000/4000E/5200 Implementation

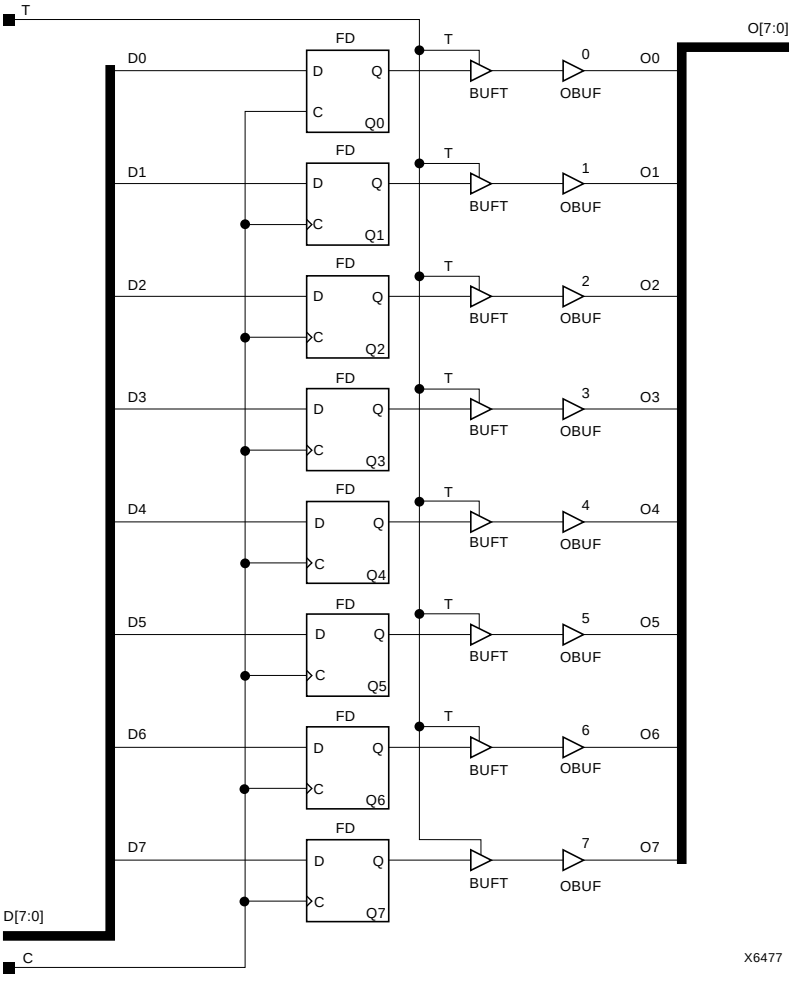
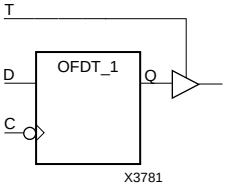


Figure 3-124 OFDT8 XC7000 Implementation

OFDT_1

D Flip-Flop with Active-High Tristate and Active-Low Output Buffer and Inverted Clock



Name	XC3000	XC4000	XC4000E	XC5200
OFDT	Primitive	Primitive	Macro	Macro
OFDT4, OFDT8, OFDT16	Macro	Macro	Macro	Macro

OFDT_1 and its output buffer are located in an input/output block (IOB). The flip-flop data output (Q) is connected to the input of an output buffer (OBUF). The OBUF output is connected to an OPAD or an IOPAD. The data on the data input (D) is loaded into the flip-flop on the High-to-Low clock (C) transition. When the active-Low enable input (T) is Low, the data on the flip-flop output (Q) appears on the O output. When T is High, the output is high impedance (Off).

The flip-flop is asynchronously reset with Low output, when power is applied or when global reset (GR) for XC3000 and 5200 or global set/reset (GSR) for XC4000/4000E is active. GR is active-Low for XC3000. The GR active level is programmable for XC5200. The GSR active level is programmable for XC4000/4000E.

Inputs			Outputs
T	**D**	**C**	**O**
1	X	X	Z
0	1	↓	1
0	0	↓	0

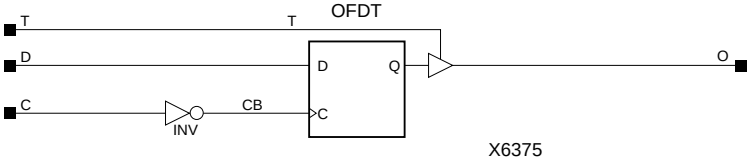
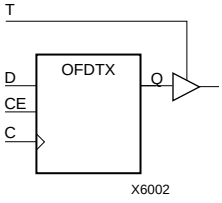


Figure 3-125 OFDT_1 XC3000/4000/4000E/5200 Implementation

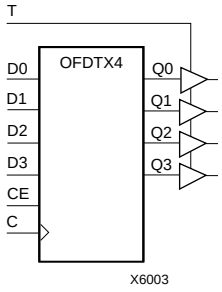
OFDTX, OFDTX4, OFDTX8, and OFDTX16

Single and Multiple D Flip-Flops with Active-High Tristate and Active-Low Output Enable Buffers

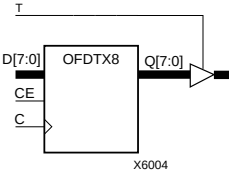


XC4000E	XC5200
Macro	N/A

OFDTX, OFDTX4, OFDTX8, and OFDTX16 are single or multiple D flip-flops whose outputs are enabled by a tristate buffers. The data outputs (Q) of the flip-flops are connected to the inputs of output buffers (OBUFT). The outputs of the OBUFTs (O) are connected to OPADs or IOPADs. These flip-flops and buffers are located in input/output blocks (IOB) for XC4000E. The data on the data inputs (D) is loaded into the flip-flops during the Low-to-High clock (C) transition. When the active-Low enable inputs (T) are Low, the data on the flip-flop outputs (Q) appears on the O outputs. When T is High, outputs are high impedance (Off). When CE is High and T is Low, the outputs do not change.

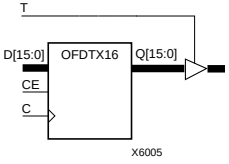


The flip-flops are asynchronously reset with Low output, when power is applied or when global set/reset (GSR) is active. The GSR active level is programmable.



Inputs				Outputs
CE	T	D	C	Q
X	1	X	X	Z
1	0	D	↑	d[a]
0	0	X	X	No Chg

a. d = state of referenced input one set-up time prior to active clock transition



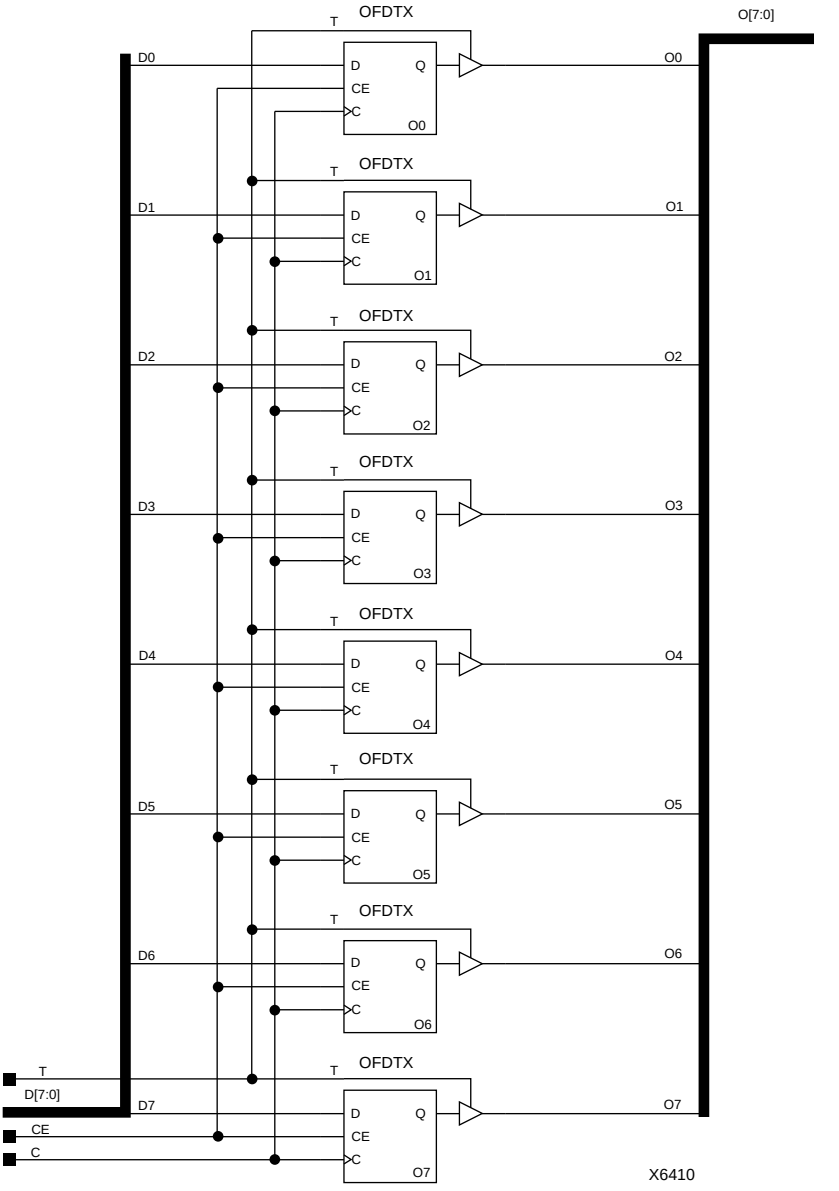
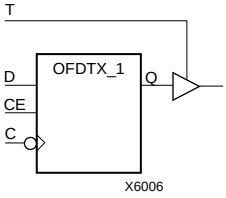


Figure 3-126 OFDTX8 XC4000E Implementation

OFDTX_1

D Flip-Flop with Active-High Tristate and Active-Low Output Buffer and Inverted Clock



XC4000E	XC5200
Macro	N/A

OFDTX_1 and its output buffer are located in an input/output block (IOB). The flip-flop data output (Q) is connected to the input of an output buffer (OBUF). The OBUF output is connected to an OPAD or an IOPAD. The data on the data input (D) is loaded into the flip-flop on the High-to-Low clock (C) transition. When the active-Low enable input (T) is Low, the data on the flip-flop output (Q) appears on the O output. When T is High, the output is high impedance (Off). When CE is High and T is Low, the outputs do not change.

The flip-flop is asynchronously reset with Low output, when power is applied or when global set/reset (GSR) is active. The GSR active level is programmable.

Inputs				Outputs
CE	T	D[a]	C	Q
X	1	X	X	Z
1	0	1	↓	0
1	0	0	↓	0
0	0	X	X	No Chg

a. d = state of referenced input one set-up time prior to active clock transition

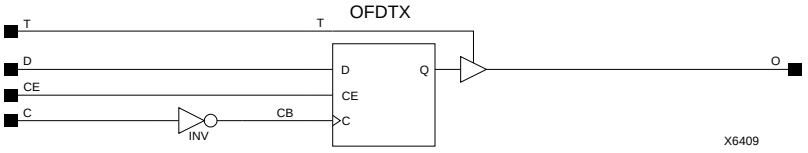
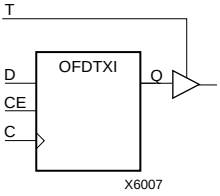


Figure 3-127 OFDTX_1 XC4000E Implementation

OFDTXI

D Flip-Flop with Active-High Tristate and Active-Low Output Buffer (Asynchronous Set)



XC4000E	XC5200
Primitive	N/A

OFDTXI and its output buffer are contained in an input/output block (IOB). The data output of the flip-flop (Q) is connected to the input of an output buffer (OBUF). The output of the OBUF is connected to an OPAD or an IOPAD. The data on the data input (D) is loaded into the flip-flop on the Low-to-High clock (C) transition. When the active-Low enable input (T) is Low, the data on the flip-flop output (Q) appears on the output (O). When T is High, the output is high impedance (Off). When CE is Low and T is Low, the output does not change.

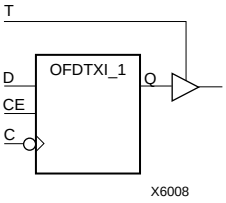
The flip-flop is asynchronously set with High output, when power is applied or when global set/reset (GSR) is active. The GSR active level is programmable.

Inputs				Outputs
CE	T	D[a]	C	O
X	1	X	X	Z
1	0	1	↑	1
1	0	0	↑	0
0	0	X	X	No Chg

a. D = state of referenced input one set-up time prior to active clock transition

OFDTXI_1

D Flip-Flop with Active-High Tristate, Active-Low Output Buffer and Inverted Clock



XC4000E	XC5200
Macro	N/A

OFDTXI_1 and its output buffer are contained in an input/output block (IOB). The data output of the flip-flop (Q) is connected to the input of an output buffer (OBUF). The OBUF output is connected to an OPAD or an IOPAD. The data on the data input (D) is loaded into the flip-flop on the High-to-Low clock (C) transition. When the active-Low enable input (T) is Low, the data on the flip-flop output (Q) appears on the O output. When T is High, the output is high impedance (Off). When CE is Low and T is Low, the output does not change.

The flip-flop is asynchronously set with High output, when power is applied or when global set/reset (GSR) is active. The GSR active level is programmable.

Inputs				Outputs
CE	**T**	**D[a]**	**C**	**O**
X	1	X	X	Z
1	0	1	↓	1
1	0	0	↓	0
0	0	X	X	No Chg

a. d = state of referenced input one set-up time prior to active clock transition

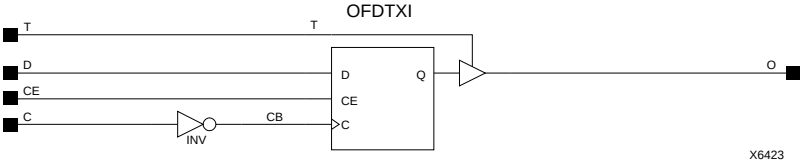
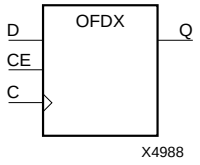
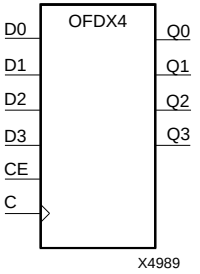


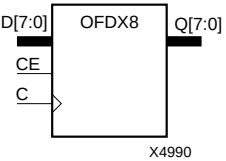
Figure 3-128 OFDTXI_1 XC4000E Implementation

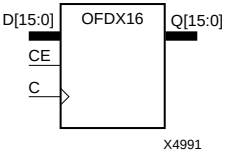
OFDX, OFDX4, OFDX8, and OFDX16

Single- and Multiple-Output D Flip-Flops









Name	XC4000E	XC5200
OFDX	Primitive	N/A
OFDX4, OFDX8, OFDX16	Macro	N/A

OFDX, OFDX4, OFDX8, and OFDX16 are single and multiple output D flip-flops. The flip-flops are located in an input/output block (IOB) for XC4000E. The outputs (for example, Q3 – Q0) are connected to OPADs or IOPADs. The data on the D inputs is loaded into the flip-flops during the Low-to-High clock (C) transition and appears on the Q outputs. When CE is Low, flip-flop outputs do not change.

The flip-flops are asynchronously reset with Low outputs, when power is applied or when global set/reset (GSR) is active. The GSR active level is programmable.

Inputs			Outputs
CE	D	C	Q
1	D	↑	dn[a]
0	X	X	No Chg

a. dn = state of referenced input one set-up time prior to active clock transition

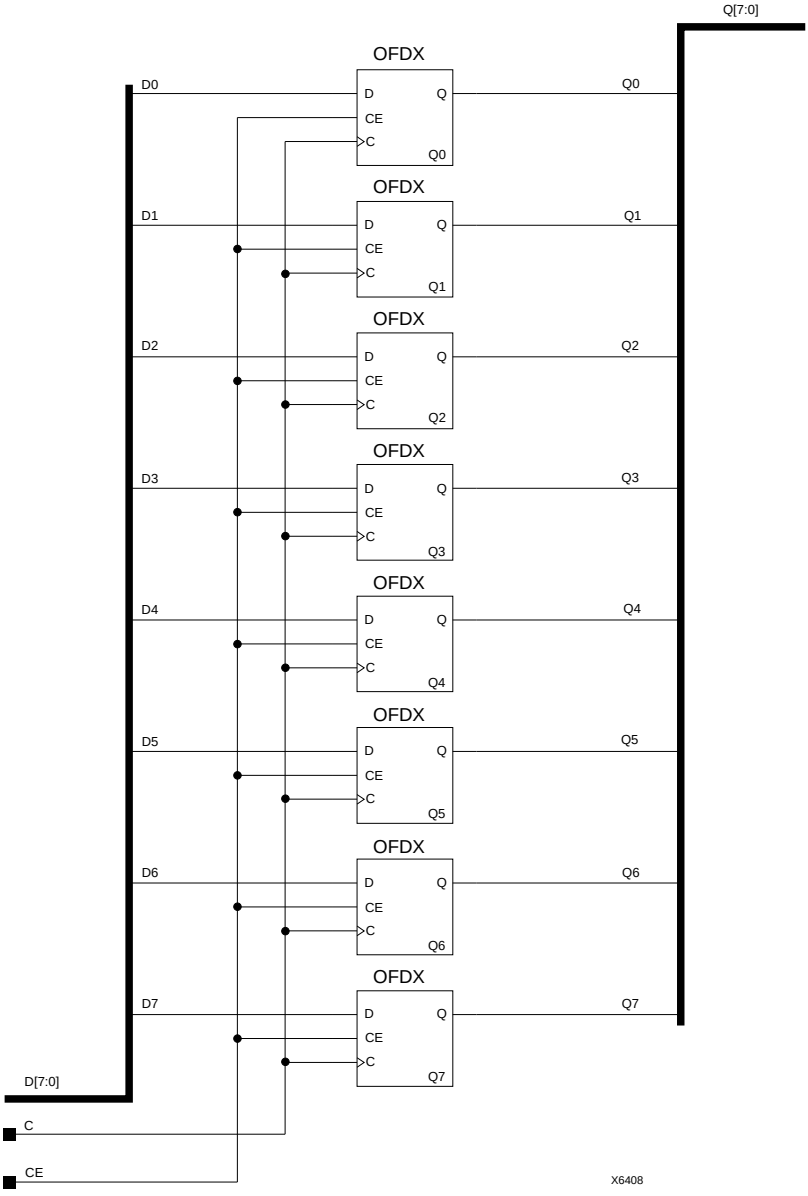
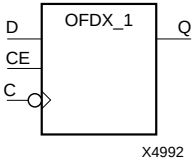


Figure 3-129 OFDX8 XC4000E Implementation

OFDX_1

Output D Flip-Flop with Inverted Clock



XC4000E	XC5200
Macro	N/A

OFDX_1 is located in an input/output block (IOB). The output (Q) of the D flip-flop is connected to an OPAD or an IOPAD. The data on the D input is loaded into the flip-flop during the High-to-Low clock (C) transition and appears on the Q output. When the CE pin is Low, the output (Q) does not change.

The flip-flop is asynchronously reset with Low output, when power is applied or when global set/reset (GSR) is active. The GSR active level is programmable.

Inputs			Outputs
CE	D	C	Q
1	D	↓	d[a]
0	X	X	No Chg

a. d = state of referenced input one set-up time prior to active clock transition

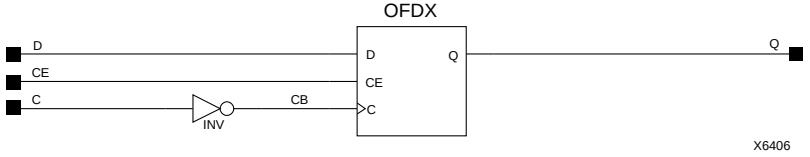
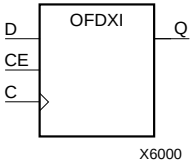


Figure 3-130 OFDX_1 XC4000E Implementation

OFDXI

Output D Flip-Flop (Asynchronous Set)



XC4000E	XC5200
Primitive	N/A

OFDXI is contained in an input/output block (IOB). The output (Q) of the D flip-flop is connected to an OPAD or an IOPAD. The data on the D input is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). When CE is Low, the output does not change.

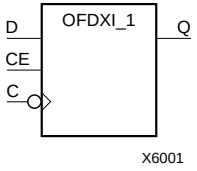
The flip-flop is asynchronously set with High output, when power is applied or when global set/reset (GSR) is active. The GSR active level is programmable.

Inputs			Outputs
CE	D	C	Q
1	D	↑	d[a]
0	X	X	No Chg

a. d = state of referenced input one set-up time prior to active clock transition

OFDXI_1

Output D Flip-Flop with Inverted Clock (Asynchronous Set)



XC4000E	XC5200
Macro	N/A

OFDXI_1 is located in an input/output block (IOB). The D flip-flop output (Q) is connected to an OPAD or an IOPAD. The data on the D input is loaded into the flip-flop during the High-to-Low clock (C) transition and appears on the Q output. The flip-flop is asynchronously set with High output, when power is applied or when global set/reset (GSR) is active. The GSR active level is programmable. When CE is Low, the output (Q) does not change.

Inputs			Outputs
CE	**D**	**C**	**Q**
1	D	↓	d[a]
0	X	X	No Chg

a. d = state of referenced input one set-up time prior to active clock transition

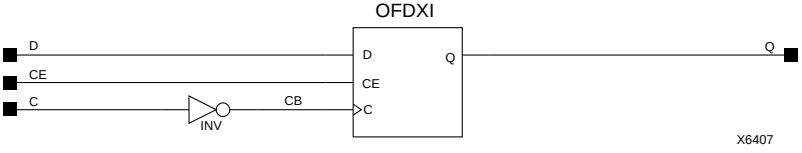


Figure 3-131 OFDXI_1 XC4000E Implementation

OR

2- to 9-Input OR Gates with Inverted and Non-Inverted Inputs

Name	XC2000	XC3000	XC4000	XC4000E	XC5200	XC7000
OR2, OR2B1, OR2B2, OR3, OR3B1, OR3B2, OR3B3, OR4, OR4B1, OR4B2, OR4B3, OR4B4	Primitive	Primitive	Primitive	Primitive	Primitive	Primitive
OR5, OR5B1, OR5B2, OR5B3, OR5B4, OR5B5	Macro	Primitive	Primitive	Primitive	Macro	Primitive
OR6, OR7, OR8, OR9	Macro	Macro	Macro	Macro	Macro	Primitive
OR12, OR16	N/A	N/A	N/A	N/A	Macro	N/A

The OR function is performed in the configurable logic block (CLB) function generators for XC2000, XC3000, XC4000/4000E, and XC5200. OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Since each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

The 12- and 16-input OR functions are available only with non-inverting inputs. To invert inputs, use external inverters.

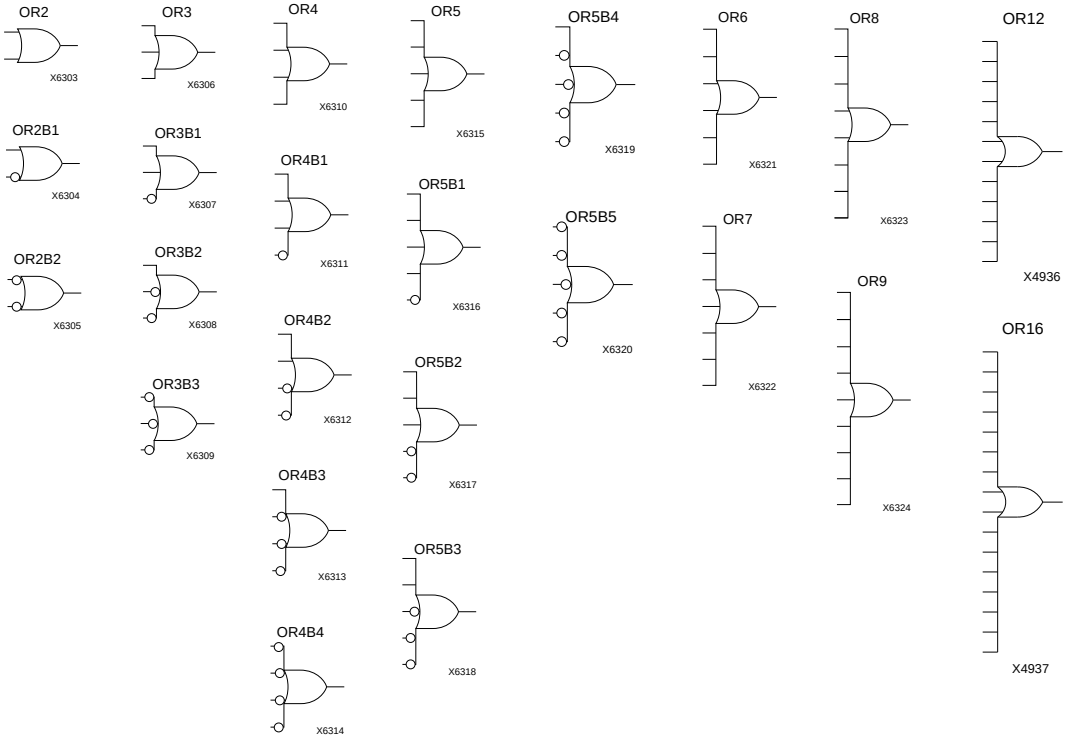


Figure 3-132 OR Gate Representations

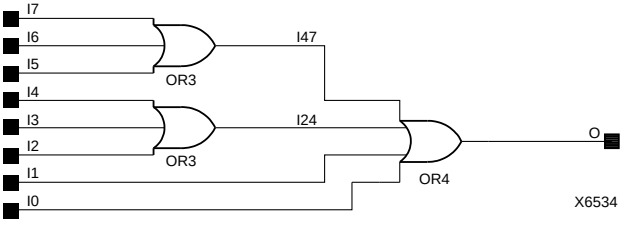


Figure 3-133 OR8 XC2000 Implementation

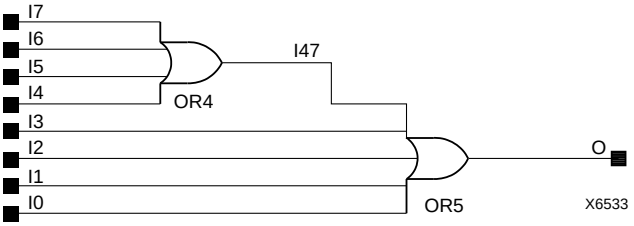


Figure 3-134 OR8 XC3000 Implementation

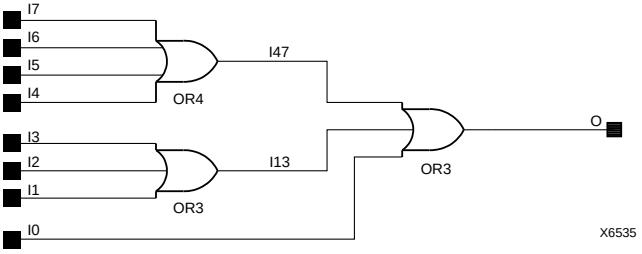


Figure 3-135 OR8 XC4000/4000E/5200 Implementation

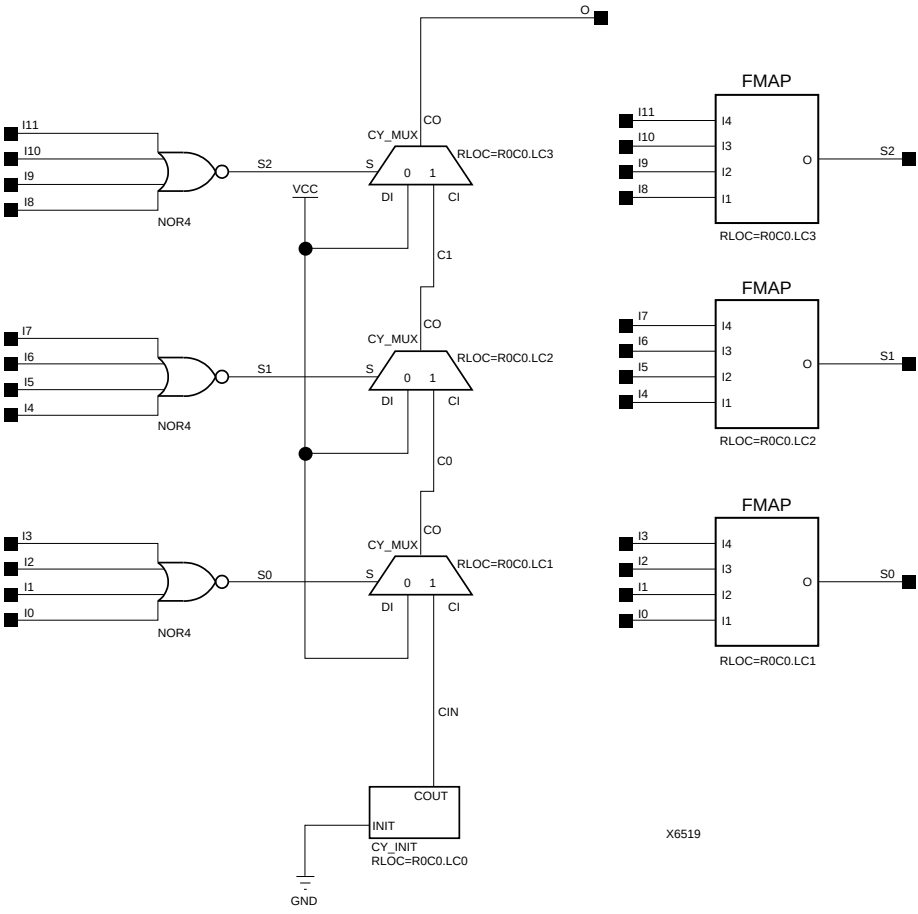


Figure 3-136 OR12 XC5200 Implementation

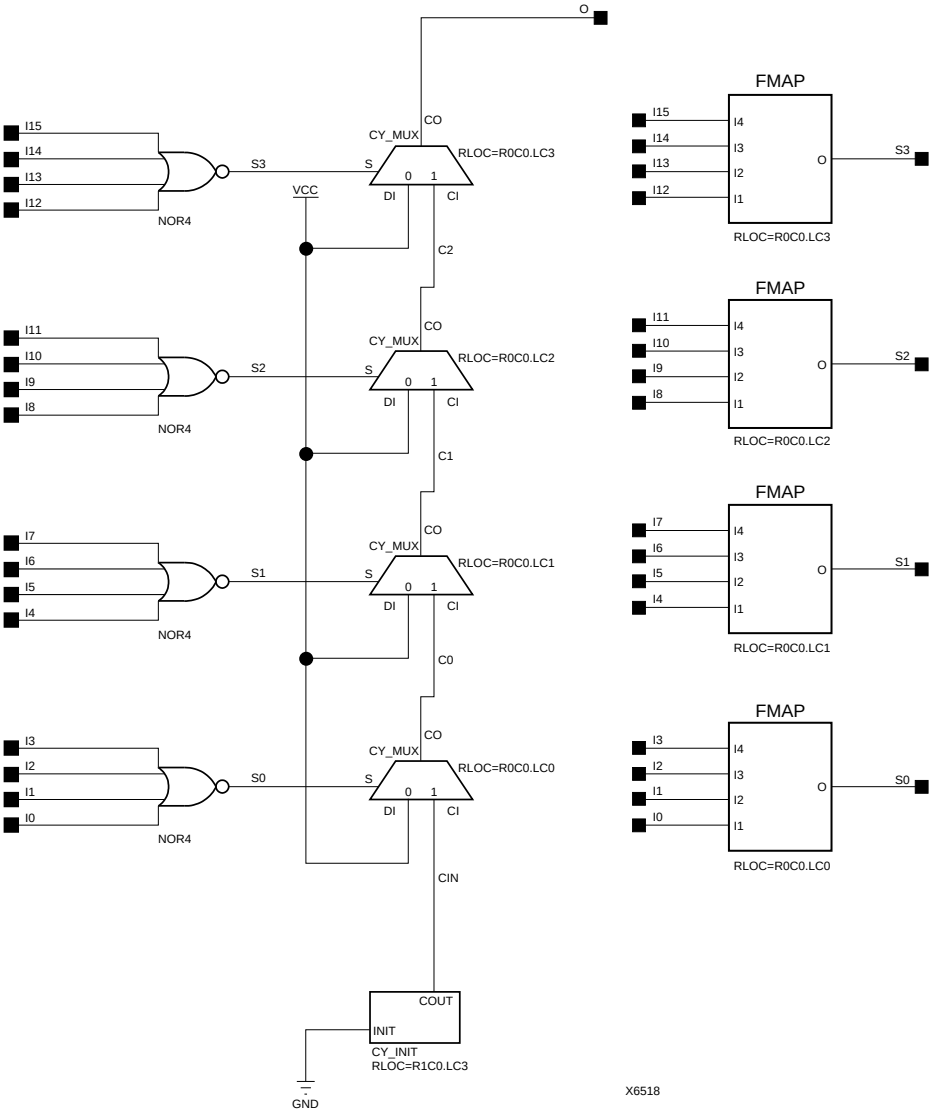
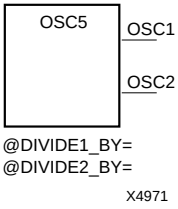


Figure 3-137 OR16 XC5200 Implementation

OSC5

Internal Multiple-Frequency Clock-Signal Generator



XC4000E	XC5200
N/A	Macro

OSC5 provides internal clock signals in applications where timing is not critical. The available frequencies are determined by FPGA device components that are process dependent. Therefore, the available frequencies vary from device to device. Use only one OSC5 per design. The OSC5 is not available if the CK_DIV element is used.

The clock frequencies of the OSC1 and OSC2 outputs are determined by specifying the DIVIDE1_BY=n_1 attribute for the OSC1 output, and the DIVIDE2_BY=n_2 attribute for the OSC2 output. n_1 and n_2 are integer numbers by which the internal 16-MHz clock is divided to produce the desired clock frequency. The available frequency options are shown in the table.

n_1	OSC1 Frequency	n_2	OSC2 Frequency
4	4 MHz	2	8 MHz
16	1 MHz	8	2 MHz
64	250 kHz	32	500 kHz
256	63 kHz	128	125 kHz
		1,024	16 kHz
		4,096	4 kHz
		16,384	1 kHz
		65,536	244 Hz

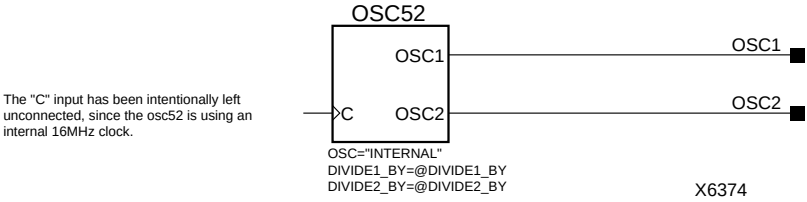
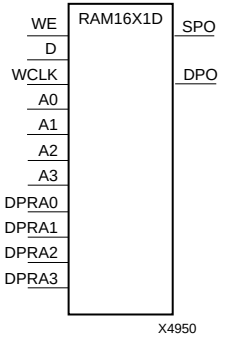


Figure 3-138 OSC5 XC5200 Implementation

RAM16X1D

16-Deep by 1-Wide Static Dual Port Synchronous RAM



XC4000E	XC5200
Primitive	N/A

RAM16X1D is a 16-word by 1-bit static dual port random access memory with synchronous write capability. The device has two separate address ports: the read address (DPRA3 – DPRA0) and the write address (A3 – A0). These two address ports are completely asynchronous. The read address controls the location of the data driven out of the output pin (DPO), and the write address controls the destination of a valid write transaction.

When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data input (D) into the word selected by the 4-bit write address. For predictable performance, write address and data inputs must be stable before a Low-to-High write transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

You can initialize RAM16X1D during configuration.

Inputs			Internal Memory Cell Addressed by A3:A0
WE	WCLK	D[a]	
0	X	X	No Chg
1	0	X	No Chg
1	1	X	No Chg
1	^	D	D

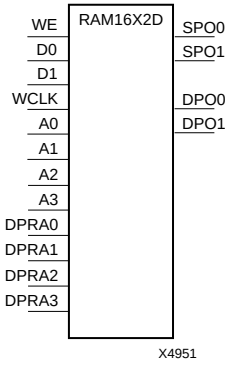
a. D = data written during last write transaction

The SPO output reflects the data in the memory cell addressed by A3 – A0. The DPO output reflects the data in the memory cell addressed by DPRA3 – DPRA0.

Note: The write process is not affected by the address on the read address port.

RAM16X2D

16-Deep by 2-Wide Static Dual Port Synchronous RAM



XC4000E	XC5200
Macro	N/A

RAM16X2D is a 16-word by 2-bit static dual port random access memory with synchronous write capability. The device has two separate address ports: the read address (DPRA3 – DPRA0) and the write address (A3 – A0). These two address ports are completely asynchronous. The read address controls the location of data driven out of the output pin (DPO1 – DPO0), and the write address controls the destination of a valid write transaction.

When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data input (D1 – D0) into the word selected by the 4-bit write address. For predictable performance, write address and data inputs must be stable before a Low-to-High write input transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

You can initialize RAM16X2D during configuration.

Inputs			Outputs
WE	WCLK	D[a]	Memory Cell Addressed by A3:A0
0	X	X	No Chg
1	0	X	No Chg
1	1	X	No Chg
1	^	D	D

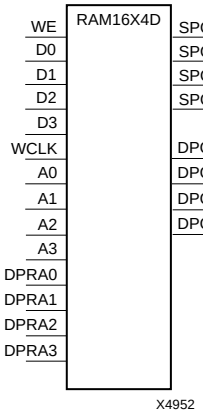
a. D = data written during last write transaction

The SPO output reflects the data in the memory cell addressed by A3 – A0. The DPO output reflects the data in the memory cell addressed by DPRA3 – DPRA0.

Note: The write process is not affected by the address on the read address port.

RAM16X4D

16-Deep by 4-Wide Static Dual Port Synchronous RAM



XC4000E	XC5200
Macro	N/A

RAM16X4D is a 16-word by 4-bit static dual port random access memory with synchronous write capability. The device has two separate address ports: the read address (DPRA3 – DPRA0) and the write address (A3 – A0). These two address ports are completely asynchronous. The read address controls the location of data driven out of the output pin (DPO3 – DPO0), and the write address controls the destination of a valid write transaction.

When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data input (D3 – D0) into the word selected by the 4-bit write address. For predictable performance, write address and data inputs must be stable before a Low-to-High write input transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

You can initialize RAM16X4D during configuration.

Inputs			Outputs
WE	WCLK	D[a]	Memory Cell Addressed by A3:A0
0	X	X	No Chg
1	0	X	No Chg
1	1	X	No Chg
1	^	D	D

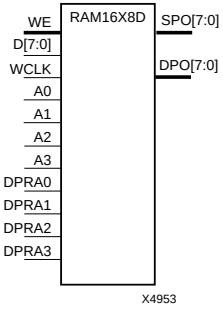
a. D = data written during last write transaction

The SPO output reflects the data in the memory cell addressed by A3 – A0. The DPO output reflects the data in the memory cell addressed by DPRA3 – DPRA0.

Note: The write process is not affected by the address on the read address port.

RAM16X8D

16-Deep by 8-Wide Static Dual Port Synchronous RAM



XC4000E	XC5200
Macro	N/A

RAM16X8D is a 16-word by 8-bit static dual port random access memory with synchronous write capability. The device has two separate address ports: the read address (DPRA3 – DPRA0) and the write address (A3 – A0). These two address ports are completely asynchronous. The read address controls the location of data driven out of the output pin (DPO7 – DPO0), and the write address controls the destination of a valid write transaction.

When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data input (D7 – D0) into the word selected by the 4-bit write address (A3 – A0). For predictable performance, write address and data inputs must be stable before a Low-to-High write input transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

You can initialize RAM16X8D during configuration.

Inputs			Outputs
WE	**WCLK**	**D[a]**	**Memory Cell Addressed by A3:A0**
0	X	X	No Chg
1	0	X	No Chg
1	1	X	No Chg
1	^	D	D

a. D = data written during last write transaction

The SPO output reflects the data in the memory cell addressed by A3 – A0. The DPO output reflects the data in the memory cell addressed by DPRA3 – DPRA0.

Note: The write process is not affected by the address on the read address port.

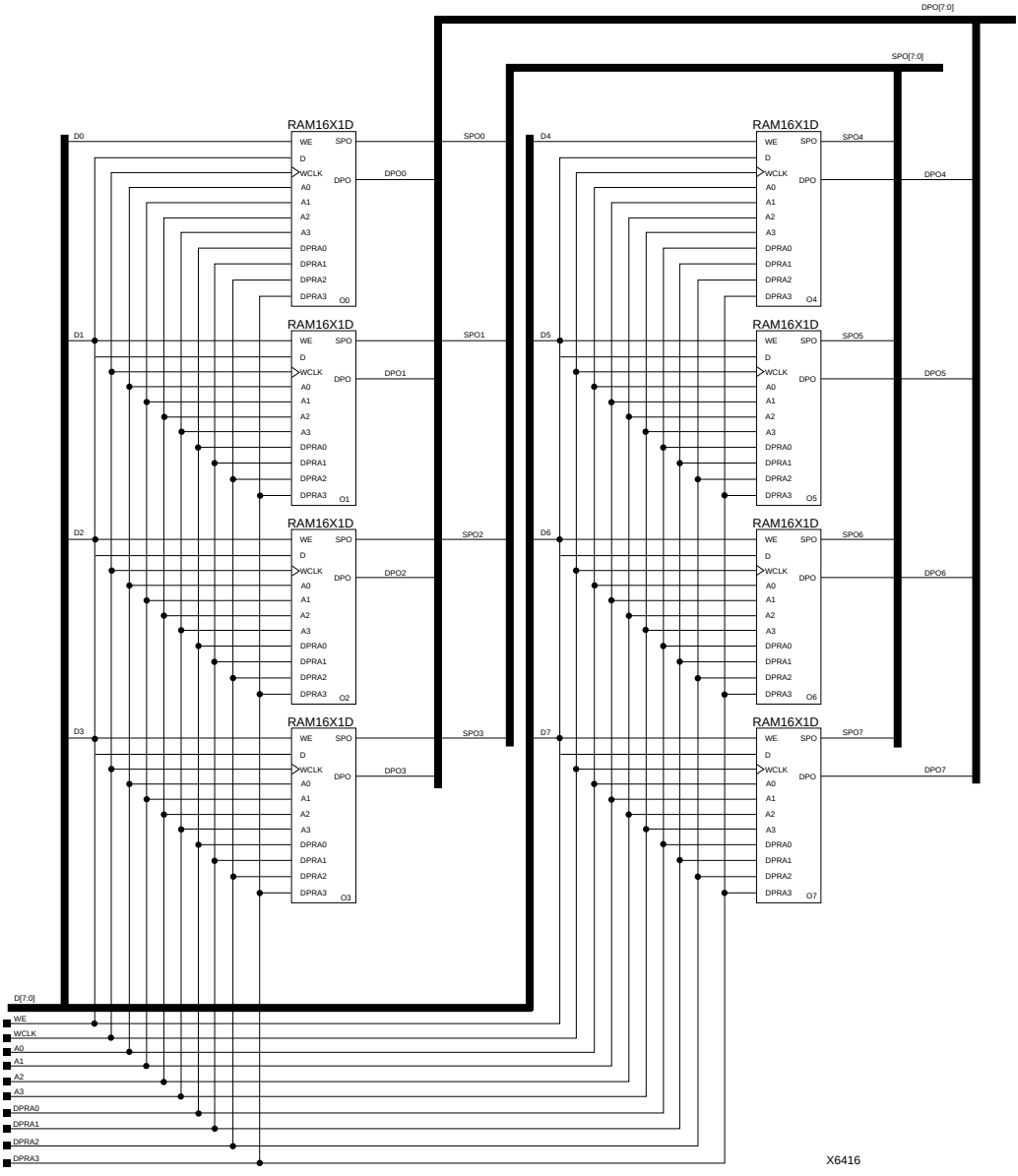
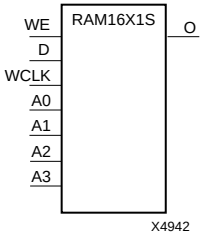


Figure 3-139 RAM16X8D XC4000E Implementation

RAM16X1S

16-Deep by 1-Wide Static Synchronous RAM



XC4000E	XC5200
Primitive	N/A

RAM16X1S is a 16-word by 1-bit static random access memory with synchronous write capability. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data input (D) into the word selected by the 4-bit address (A3 – A0). For predictable performance, address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pin (O) is the data that is stored in the RAM at the location defined by the values on the address pins.

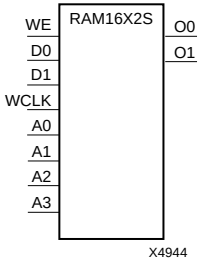
You can initialize RAM16X1S during configuration.

Inputs			Outputs
WE	WCLK	D	O
0	X	X	Data[a]
1	0	X	Data
1	^	D	D
1	1	X	Data

a. Data = word addressed by bits A3 – A0

RAM16X2S

16-Deep by 2-Wide Static Synchronous RAM



XC4000E	XC5200
Macro	N/A

RAM16X2S is a 16-word by 2-bit static random access memory with synchronous write capability. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data input (D1 – D0) into the word selected by the 4-bit address (A3 – A0). For predictable performance, address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pin (O1 – O0) is the data that is stored in the RAM at the location defined by the values on the address pins.

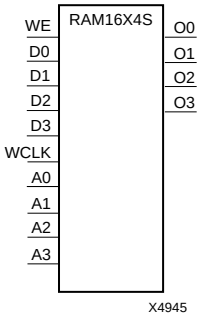
You can initialize RAM16X2S during configuration.

Inputs			Outputs
WE	**WCLK**	**D**	**O**
0	X	X	Data[a]
1	0	X	Data
1	^	D	D
1	1	X	Data

a. Data = word addressed by bits A3 – A0

RAM16X4S

16-Deep by 4-Wide Static Synchronous Ram



XC4000E	XC5200
Macro	N/A

RAM16X4S is a 16-word by 4-bit static random access memory with synchronous write capability. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data input (D3 – D0) into the word selected by the 4-bit address (A3 – A0). For predictable performance, address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pin (O3 – O0) is the data that is stored in the RAM at the location defined by the values on the address pins.

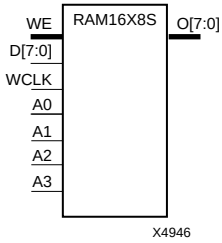
You can initialize RAM16X4S during configuration.

Inputs			Outputs
WE	**WCLK**	**D3 – D0**	**O3 – O0**
0	X	X	Data[a]
1	0	X	Data
1	^	D	D
1	1	X	Data

a. Data = word addressed by bits A3 – A0

RAM16X8S

16-Deep by 8-Wide Static Synchronous RAM



XC4000E	XC5200
Macro	N/A

RAM16X8 is a 16-word by 8-bit static random access memory with synchronous write capability. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on data inputs (D7 – D0) into the word selected by the 4-bit address (A3 – A0). For predictable performance, address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pin (O7 – O0) is the data that is stored in the RAM at the location defined by the values on the address pins.

You can initialize RAM16X8 during configuration.

Inputs			Outputs
WE	**WCLK**	**D**	**O**
0	X	X	Data[a]
1	0	X	Data
1	^	D	D
1	1	X	Data

a. Data = word addressed by bits A3 – A0

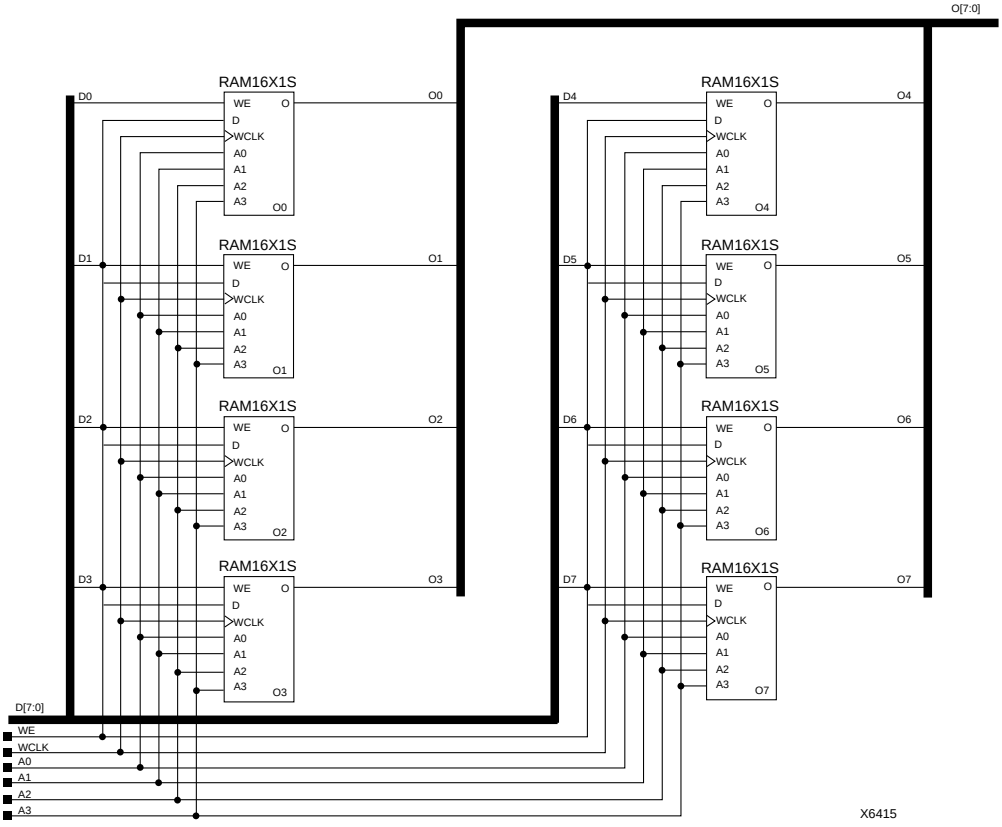
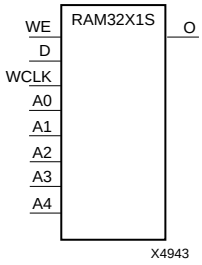


Figure 3-140 RAM16X8S XC4000E Implementation

RAM32X1S

32-Deep by 1-Wide Static Synchronous RAM



XC4000E	XC5200
Primitive	N/A

RAM32X1 is a 32-word by 1-bit static random access memory with synchronous write capability. When the write enable is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data input (D) into the word selected by the 5-bit address (A4 – A0). For predictable performance, address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pin (O) is the data that is stored in the RAM at the location defined by the values on the address pins.

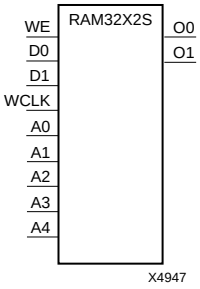
You can initialize RAM32X1 during configuration.

Inputs			Outputs
WE	**WCLK**	**D**	**O**
0	X	X	Data[a]
1	0	X	Data
1	^	D	D
1	1	X	Data

a. Data = word addressed by bits A4 – A0

RAM32X2S

32-Deep by 2-Wide Static Synchronous RAM



XC4000E	XC7000
Macro	N/A

RAM32X2 is a 32-word by 2-bit static random access memory with synchronous write capability. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data input (D1 – D0) into the word selected by the 5-bit address (A4 – A0). For predictable performance, address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pin (O1 – O0) is the data that is stored in the RAM at the location defined by the values on the address pins.

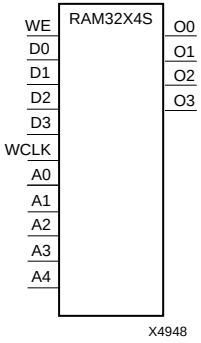
You can initialize RAM32X2 during configuration.

Inputs			Outputs
WE	**WCLK**	**D**	**O**
0	X	X	Data[a]
1	0	X	Data
1	^	D	D
1	1	X	Data

a. Data = word addressed by bits A4 – A0

RAM32X4S

32-Deep by 4-Wide Static Synchronous RAM



XC4000E	XC5200
Macro	N/A

RAM32X4 is a 32-word by 4-bit static random access memory with synchronous write capability. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data inputs (D3 – D0) into the word selected by the 5-bit address (A4 – A0). For predictable performance, address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pin (O3 – O0) is the data that is stored in the RAM at the location defined by the values on the address pins.

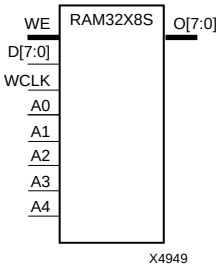
You can initialize RAM32X4 during configuration.

Inputs			Outputs
WE	**WCLK**	**D**	**O**
0	X	X	Data[a]
1	0	X	Data
1	^	D	D
1	1	X	Data

a. Data = word addressed by bits A4 – A0

RAM32X8S

32-Deep by 8-Wide Static Synchronous RAM



XC4000E	XC5200
Macro	N/A

RAM32X8 is a 32-word by 8-bit static random access memory with synchronous write capability. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is High, any positive transition on WCLK loads the data on the data inputs (D7 – D0) into the word selected by the 5-bit address (A4 – A0). For predictable performance, address and data inputs must be stable before a Low-to-High WCLK transition. This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pin (O7 – O0) is the data that is stored in the RAM at the location defined by the values on the address pins.

You can initialize RAM32X8 during configuration.

Inputs			Outputs
WE	**WCLK**	**D**	**O**
0	X	X	Data[a]
1	0	X	Data
1	^	D	D
1	1	X	Data

a. Data = word addressed by bits A4 – A0

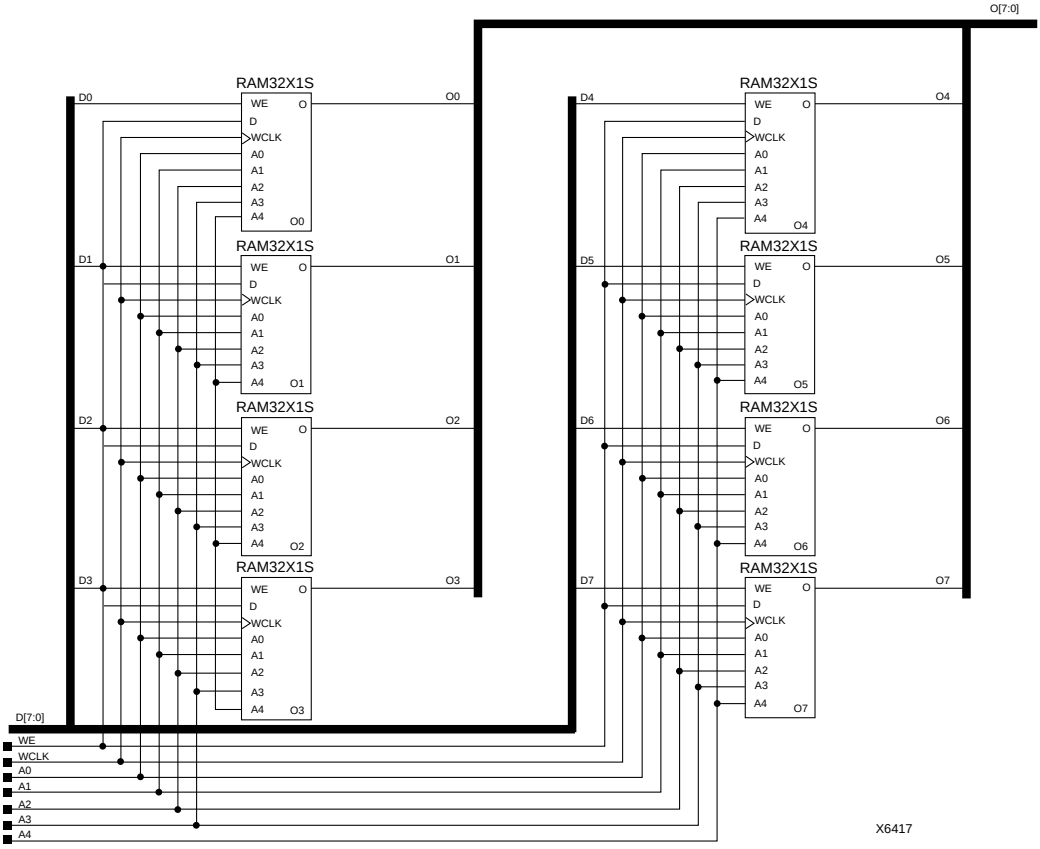
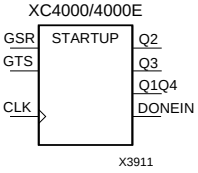
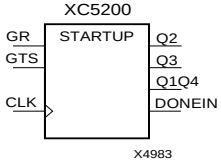


Figure 3-141 RAM32X8S XC4000E Implementation

STARTUP

User Interface to Global Clock, Reset, and Tristate Controls





XC4000	XC4000E	XC5200
Primitive	Primitive	Primitive

STARTUP is used primarily to provide access to global set/reset (GSR) for XC4000/4000E or global reset (GR) for XC5200; global tristate control (GTS); and the user configuration clock.

GSR can asynchronously re-initialize all CLB and IOB flip-flops to the state they had at the end of the configuration process. GR can asynchronously reset all CLB and IOB flip-flops in a design. Following configuration, GTS can be used to force all of the IOB outputs to High impedance mode, which isolates the device outputs from the circuit, while the inputs remain active. By default, the GSR, GR, and GTS signals are active High. The change the polarity of these signals, add an inverter to the net that sources these signals.

The configuration clock input (CLK) must be connected to a user clock if the start-up of the device is synchronized with the user clock. Also, “user clock” must be selected in the MakeBits program.

The STARTUP outputs (Q2, Q3, Q1Q4, and DONEIN) display the progress/status of the start-up process following the configuration.

Trademark Information

4,855,619; 4,855,669; 4,902,910; 4,940,909; 4,967,107; 5,012,135; 5,023,606; 5,028,821; 5,047,710; 5,068,603; 5,140,193; 5,148,390; 5,155,432; 5,166,858; 5,224,056; 5,243,238; 5,245,277; 5,267,187; 5,291,079; 5,295,090; 5,302,866; 5,319,252; 5,319,254; 5,321,704; 5,329,174; 5,329,181; 5,331,220; 5,331,226; 5,332,929; 5,337,255; 5,343,406; 5,349,248; 5,349,249; 5,349,250; 5,349,691; 5,357,153; 5,360,747; 5,361,229; 5,362,999; 5,365,125; 5,367,207; 5,386,154; 5,394,104; 5,399,924; 5,399,925; 5,410,189; 5,410,194; 5,414,377; RE 34,363, RE 34,444, and RE 34,808. Other U.S. and foreign patents pending. Xilinx, Inc. does not represent that devices shown or products described herein are free from patent infringement or from any other third party right. Xilinx assumes no obligation to correct any errors contained herein or to advise any user of this text of any correction if such be made. Xilinx will not assume any liability for the accuracy or correctness of any engineering or software support or assistance provided to a user.

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