LogiCORE

DFT Cores
(Real Data In, Complex Data Out)

XILINX®

DSP CORE Generator

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DFT technology developed by Rice Electronics.

Features

- 2's complement, fixed point arithmetic
- Real-valued input data (15 bit)
- Complex output data (16 bit ~86 dB available output SNR)
- Integrated Input Buffer (no external memory requirements)
- Transform size (N) = 32, 64, or 128
- Process real-time sampling rates >1Mhz (>12Mhz for N=32)
- Simplified interface (nominal support logic required)
- Synchronous design, optimized for XC4000E, EX, and XL families of FPGAs

Applications

- Communications (high speed modems, transmultiplexers)
- Instrumentation (medical, scientific, test)
- Multi-media (signal compression/decompression)
- Military (radar, EW, ELINT, ESM)

General Description

The 16-bit Discrete Fourier Transform (DFT) Cores are functionally complete elements. The designs present a simplified interface and require no external memory. The Cores target the Xilinx XC4000E, EX, and XL FPGA product series.

The Cores render the following transform for a real-valued input vector, f(n):

$$F(j) = \sum_{n=0}^{N-1} f(n)e^{-2\pi in\frac{j}{N}}$$

for n=0 to N-1, j=0 to (N/2-1)

where:

$F(j)$ = output (frequency domain) coefficients
$f(n)$ = input (time domain) sequence
N = length of input sequence (transform size)

The Cores accept a real-valued input sequence f(n) and produce a complex output sequence F(j). Due to the real-valued nature of f(n), only the lower half of the set of F(j) is generated. The upper half of the F(j) is the complex conjugate of the lower half, and therefore represents redundant information.

The Cores are optimized for small to medium size transforms (32 - 128 points). A 32-point transform can be executed in less than 5 microseconds (XC4000-3). General specifications of the Cores are listed in Table 1.

Table 1. 16-bit DFT Family Parameters

Core Name	N = Size of Transform	P = Clock Periods[1]	Clock Speed[2]	Execution Time[3]	Core Size[4]
16b32pt	32 points	144	59 Mhz	2.5 usecs	274 CLBs
16b64pt	64 points	1088	59 Mhz	18.5 usecs	302 CLBs
16b128pt	128 points	4224	59 Mhz	71.8 usecs	394 CLBs

1. P = number of clock periods for transform execution
2. Maximum clock speeds based on XC4000E-1 series
3. Execution Time = P/(Clock Speed in Mhz)
4. XC4008 = 324 CLBs
   XC4010 = 400 CLBs
   XC4085 = 3,136 CLBs

Functional Description

The 16-bit DFT Cores are functionally complete processors requiring minimal external control.

The Cores incorporate an Input Buffer, which is loaded with the vector f(n) to be processed. This constitutes the **Initialization** state of the Core.

After initialization, the Core can perform the DFT function with no external control. During this time, output coefficients F(j) are produced by the Core at a constant rate. This is termed the **Execution** state of the Core.

The DFT Cores possess physically separate input and output interfaces.

The input interface is used only during the **Initialization** state. Separate data and address busses are provided, allowing access to individual locations of the Input Buffer memory.

The output interface is active only during the **Execution** state. This interface provides physically separate busses for output coefficients, and index information. The index identifies the specific output coefficient F(j).

Pinout

DATA INPUT

Prior to processing, an input vector f(n) is loaded to the Core's Input Buffer memory. Data is written to the Input Buffer using the 15 bit Data Input bus (IN[14:0]), the Address bus (ADR[x:0]), and a Write Enable (WREN).

DATA OUTPUT

Output consists of the 16-bit Output bus (FREQ[15:0]), the Index bus (INDEX[x:0]), and an output Synchronization signal (SYNC). Output coefficients F(j) are presented on the Output bus. The corresponding value of j appears on the Index bus.

The Index bus identifies the component (imaginary or real) and the coefficient number (j), associated with the data on the Output bus.

TIMING INPUTS

Timing inputs consist of a START signal, and a continuous clock (MULCK). A pre-defined number of clock pulses is required for execution of the transform (see Table 1).

Figure 1 illustrates the 16-bit DFT Core interface signals.
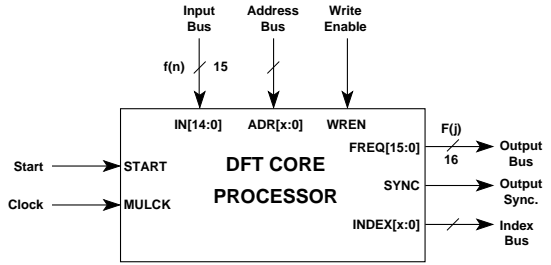
Note: $x=(\log_2 N)-1$

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Figure 1. 16-bit DFT Core Interfaces

The format of the interface signals is summarized in Table 2.

Table 2. Core Signal Pinout

Signal	Signal Direction	Description
START	Input	Logic level dictates operational state: 0=Initialization, 1=Execution
MULCK	Input	Continuous clock (see Table 1 for max.frequency)
WREN	Input	Logic level controls writing to Core Input Buffer memory: 1=Write, 0=No action. Active only when START is low
IN[14:0]	Input	One sign bit + 14 magnitude bits; 2's complement notation. Uni-directional input bus for f(n)
ADR[x:0]	Input	Consists of $\log_2 N$ bits, where N is transform size (e.g., 5 address lines for N=32). Specifies write address to Input Buffer memory
SYNC	Output	Positive pulse indicates presence of new output component on FREQ output bus (pulse width = 1 clock period)
FREQ[15:0]	Output	One sign bit + 15 magnitude bits; 2's complement notation. Uni-directional output bus for F(j)
INDEX[x:0]	Output	Consists of $\log_2 N$ bits, where N is transform size (e.g., 5 bits for N=32). Identifies F(j) value on FREQ bus. Index MSB indicates imaginary or real component: 0=Imaginary, 1=Real. Remainder of Index indicates j

Timing and Control

The 16-bit DFT cores possesses two operational states as follows:

1) **Initialization** (input vector f(n) is loaded into Core)

2) **Execution** (output vector F(j) is produced by Core)

The Start signal determines whether the Core is in the Initialization or Execution state. The Core requires a continuous clock input (MULCK) in both states. (Table 1 lists maximum clock frequency.)

Initialization (START=0)

(Input State)

When Start is low, DFT processing is disabled and the Input Buffer can be initialized (loaded). Individual address locations are loaded by means of the Address Bus, Input Bus, and Write Enable (WREN).

The Core latches these inputs on the rising edge of MULCK. All inputs should be stable at least 20ns prior to the rising edge of MULCK. When WREN is high and Start is low, data is written to the specified address.

The input, f(n), must be loaded into the following Input Buffer address locations:

$$f(0)--->location\ 0$$
$$f(1)--->location\ 1$$
$$f(2)--->location\ 2$$
$$\bullet$$
$$\bullet$$
$$\bullet$$
$$f(N-1)--->location\ (N-1)$$

When Start is high, WREN has no effect on the Input Buffer.

Execution (START=1)

(Output State)

Setting Start high begins DFT processing. The number of clock periods (P) required to execute the DFT is given in Table 1.

Access to the Core internal memory is disabled during the execution phase.

During execution, the frequency coefficients F(j) are produced at the Output bus. Separate 16 bit values are generated for the real and imaginary components of F(j). The components are produced in a specific order, as defined in Table 3.

Table 3. DFT Output Order

| Output Bus	Index Bus LSBs	Index Bus MSB
$F_I(0)$ [First out]	0	0
$F_I(0)$	0	0
$F_R(0)$	0	1
$F_R(0)$	0	1
$F_I(1)$	1	0
$F_I(N/2 - 1)$	N/2 - 1	0
$F_R(1)$	1	1
$F_R(N/2 - 1)$	N/2 - 1	1
$F_I(2)$	2	0
$F_I(N/2 - 2)$	N/2 - 2	0
$F_R(2)$	2	1
$F_R(N/2 - 2)$	N/2 - 2	1
$F_I(3)$	3	0
$F_I(N/2 - 3)$	N/2 - 3	0
$F_R(3)$	3	1
$F_R(N/2 - 3)$	N/2 - 3	1
:	:	:
$F_I(N/4)$	N/4	0
$F_I(N/2 - N/4)$	N/2 - N/4	0
$F_R(N/4)$	N/4	1
$F_R(N/2 - N/4)$ [Last out]	N/2 - N/4	1

Note: The 16-bit DFT core generates redundant information at the beginning and end of the transform, resulting in (N+4) total output values.

The output components are produced at a constant rate, with P/(N+4) clock pulses between outputs (P=number of clocks for transformation, N=transform size).

The Output Sync line produces a positive pulse for each new output component. The pulse is one clock cycle wide, and occurs one clock cycle after the appearance of a new component. Figure 2 illustrates output timing.

The Index bus identifies the component on the Output Bus. The Index MSB is low (0) for <u>imaginary</u> output and high (1) for <u>real</u> output. The remainder of the Index bus represents j, which ranges from 0 (DC) to (N/2-1).

An Index value of all zeros indicates no meaningful data is on the Output bus. This corresponds to the component $F_I(0)$, which is defined by the DFT equation as zero, for a real-valued input sequence. Simulation output for this component may be either undefined (xxxx) or zero.
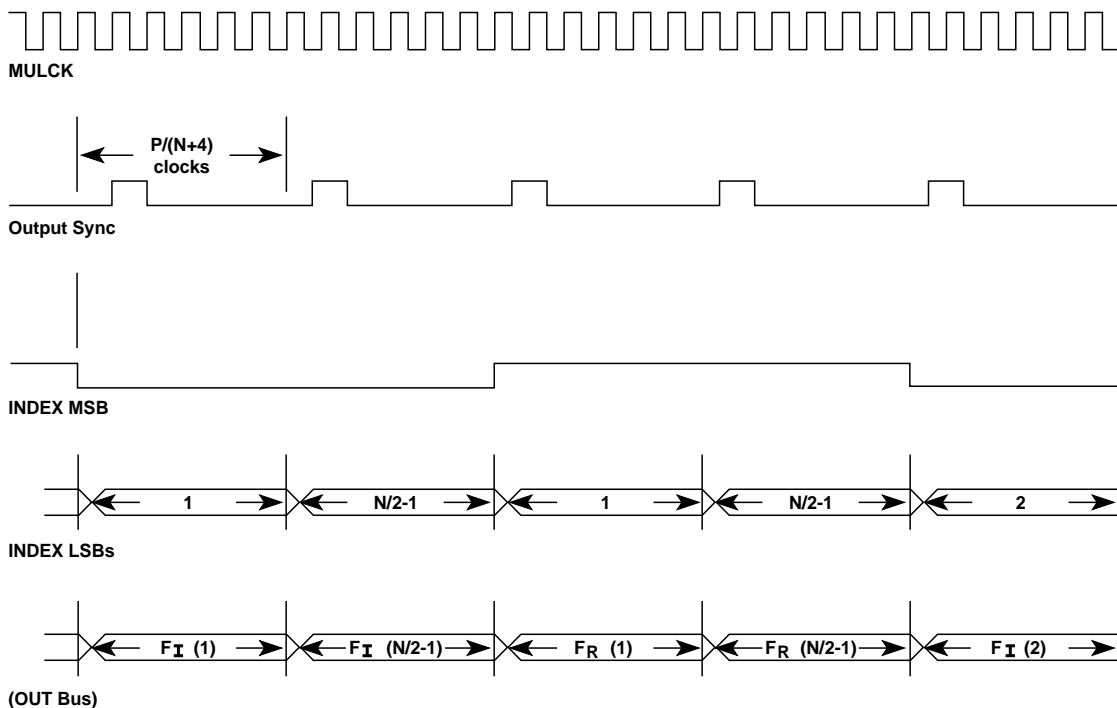
Note: All signal transitions occur on a rising clock edge.   X8157

Figure 2. Execution State – Output Timing

Ordering Information

This macro comes standard with the Xilinx CORE Generator. For additional information contact your local Xilinx sales representative, or e-mail requests to dsp@xilinx.com.

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