XC4400EX/XL HardWire™ Array Family

Advance

Product Specification

Features

- Mask-programmed versions of Programmable Logic Cell Arrays FPGA
  - Specifically designed for easy XC4000EX/XL series FPGA conversions
  - Significant cost reduction for high volume applications
  - Transparent conversion from FPGA device
  - On-chip scan-path test registers
  - High performance CMOS process
  - Meets XC4000EX series -3 speeds
  - Supports all XC4000EX/XL Select-RAM™ features
  - Low voltage versions available for 3.3 V operation
  - PCI compliant I/O
- Easy conversion with guaranteed results
  - No customer engineering resource required
  - Fully pin-for-pin compatible
  - Supports most popular package types
  - Same specifications and architecture as programmable FPGA devices
  - All nets and CLBs preserved
  - FPGA Design File used to generate production ready prototypes
  - Prototypes built on production fab line, fully tested to production specification
  - Greater than 95% fault coverage

Description

The XC4400EX/XL Series HardWire Arrays are advanced mask-programmed versions of the XC4400EX/XL programmable devices. In high-volume applications where the design is stable, the programmable FPGA devices used for prototyping and initial production can be replaced by their HardWire Array equivalents. This offers a significant cost reduction with virtually no risk or engineering resources required.

In a programmable FPGA device, the logic functions and interconnections are determined by the configuration program data, loaded and stored in internal static-memory cells. The HardWire device has the identical functional architecture as the programmed FPGA device it replaces. In the HardWire device, the logic is optimized for area but maintains the relative timing relationship.

Xilinx manufactures the HardWire device using the information from the programmed FPGA design file. Since the HardWire device is both pinout and architecturally identical to the programmable FPGA device, it is easily created without all the costly and time-consuming customer engineering activity that other semicustom solutions would require – no redesign time, no expensive and time-consuming simulation runs, no place and route, no test-vector generation. Xilinx proprietary software checks the design and maintains timing relationships as well as automatically generating test vectors.The combination of the program-

Table 1. Summary of HardWire Product Availability For Each Member of the XC4000EX Family

HardWire Device	Replacement FPGA	Speed Grade	Packages									
			PQ208	PQ240	PG299	HQ304	BG256	BG352	PG411	BG432	PG475	BG560
XH4428EX	XC4028EX	-3	√	√	√	√		√				
XH4436EX	XC4036EX	-3		√		√		√	√	√		
XH4428XL	XC4028XL	TBD	√	√	√		√	√				
XH4436XL	XC4036XL	TBD	√	√				√	√	√		
XH4444XL	XC4044XL	TBD		√				√	√	√		
XH4452XL	XC4052XL	TBD		√					√	√		√
XH4462XL	XC4062XL	TBD		√						√	√	√

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mable FPGA device and the HardWire Array offers the fastest and easiest way to get a new product to market, while ensuring low cost, low risk, and high-volume cost reduction.

The XC4400EX/XL HardWire technology further optimizes silicon area by removing all unused logic in a CLB, and removing any unused CLBs and routing resources. In fact, all unused FPGA features are eliminated in the XC4400EX/XL. However, using our DesignLock™ technology, the implementation of the CLBs (including placement and routing) are maintained. This unique conversion process also eliminates the need for timing simulation. Timing is guaranteed through our Design Review process with the aid of our proprietary software.

See The Xilinx *Data Book* for more information on the XC4000 architecture.

Interconnect

User-defined interconnect resources in the device provide routing paths to connect inputs and outputs of the I/O and logic blocks into logic networks.

The speed of the interconnect paths of the HardWire Array is significantly faster, since all interconnections are fixed metal connections.

Architectural Enhancements

Compared to older array families, XC4400EX/XL HardWire arrays provide significant enhancements. Powerful system features, as listed below, are incorporated to improve system speed, device flexibility, and ease of use.

- JTAG Boundary Scan IEEE 1149.1 Boundary-scan
- Select-RAM Memory: on chip RAM with:
  - Synchronous write option
  - Dual-port RAM option
- Configuration Emulation for system timing integrity

STARTUP

The STARTUP User Logic block is completely supported in the XC4400EX/XL. The input pins for GSR and GTS can be tied anywhere in the design. Each of these pins can also be inverted, as in the XC4000EX FPGA. Refer to Figure 1 for a detailed block diagram of the STARTUP User Logic block. Xilinx recommends the use of the STARTUP block for FPGA designs. By utilizing the GSR pin, all flip-flops in the design may be cleared. It is further recommended that the GSR input be driven directly from a device pin rather than from internal logic. This permits the design to be fully reset from an external device pin, resulting in greater testability.

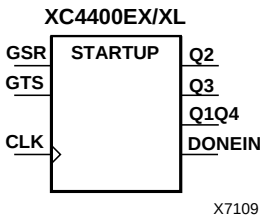

Figure 1. STARTUP User Logic Block

Similary, the GTS pin should also be connected to an external device pin so that the FPGA/HardWire may have all I/O pins at a three-state condition. This condition is often necessary for printed circuit board level manufacturing testing and is therefore a recommended design practice.

Configuration Modes

XC4000E devices have six configuration modes. XC4400EX/XL devices have the same six modes, plus an additional configuration mode. These modes are selected by a 3-bit input code applied to the M2, M1, and M0 inputs. These are three self-loading Master modes, two Peripheral modes, and a Serial Slave mode, which is used primarily for daisy-chain devices. The seventh mode, called Express mode, is an additional slave mode that allows high-speed parallel configuration of the high-capacity XC4400EX/XL devices. The coding for modes selection is shown in Table 2.

Table 2. Configuration Modes

Mode	M2	M1	M0	CCLK	Data
Master Serial	0	0	0	output	Bit-Serial
Slave Serial	1	1	1	input	Bit-Serial
Master Parallel Up	1	0	0	output	Byte-Wide, increment from 00000
Master Parallel Down	1	1	0	output	Byte-Wide, increment from 3FFFF
Peripheral Synchronous*	0	1	1	input	Byte-Wide
Peripheral Asynchronous*	1	0	1	output	Byte-Wide
Express (XC4000EX only	0	1	0	input	Byte-Wide
Reserved	0	0	1	–	–

Note: * Peripheral Synchronous can be considered byte-wide Slave Parallel

A detailed description of each configuration mode, with timing information, is included in the XC4000E data sheet. For more information on Configuration Emulation, refer to the Design Considerations section of this Data Book.

Power Distribution

Power for the HardWire Array is distributed through a grid to achieve high noise immunity and isolation between logic and I/O. Inside the device, dedicated V_{CC} and ground rings surround the logic array and provide power to the I/O drivers. An independent matrix of V_{CC} and ground lines supplies the interior logic of the device. This power distribution grid provides a stable supply and ground for all internal logic, providing the external package power pins are all connected and appropriately decoupled. Typically a 0.1-µF capacitor connected near the V_{CC} and ground pins will provide adequate decoupling.

Output buffers capable of driving the specified 12-mA/24-mA loads under worst-case conditions may be capable of driving many times that current in a best case. Noise can be reduced by minimizing external load capacitance and reducing simultaneous output transitions in the same direction. It may also be beneficial to locate heavily loaded output buffers near the ground pads. The I/O Block output buffers have a slew-limited mode which should be used where output rise and fall times are not speed critical. Slew-limited outputs maintain their dc drive capability, but generate less external reflections and internal noise. A recommended maximum total external current load for simultaneous fast-mode switching in the same direction is 100 mA per power/ground pin pair. For slew-rate limited outputs this total is four times larger.

XC4400EX/XL-Family Pin Assignments

Xilinx offers members of the XC4400EX/XL family in a variety of surface-mount package types, with pin counts from 208 to 476.

Each chip is offered in several package types to accommodate the available PC-board space and manufacturing technology. Most package types are also offered with different chips to accommodate design changes without requiring PC-board changes.

Table 3. Dedicated or Special Pins on XC4400EX/XL HardWire Array For Configuration Emulation

Pin Function		
	Configuration Emulation Mode	
Pin Name	**During Configuration**	**During Operation**
M0	M0	User Input (1,2)
M1	M1	User Output (1,2)
M2	M2	User Input (1,2)
CCLK	Master: Output, Slave; Input	HIGH - Internal Pull-up
$\overline{\text{PROGRAM}}$	$\overline{\text{PROGRAM}}$ Input	Global Reset Device - “Reconfigure”
DONE	DONE Output	HIGH - Internal Pull-up
HDC	HDC Output	User I/O
$\overline{\text{LDC}}$	$\overline{\text{LDC}}$ Output	User I/O
$\overline{\text{INIT}}$	Master: $\overline{\text{INIT}}$ Input, Slave POR Output	Open Drain
DIN	DIN Pin	User I/O
DOUT	DOUT Pin	User I/O

Notes:
1. User Pin is only accessible through special schematic I/O Macros
2. Pin does not have an associated IOB register(s)
3. DIN can also be D0-07 pins

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Unrestricted User-Programmable I/O Pins.

An I/O pin may be programmed by the user to be an Input or an Output pin following configuration. Before configuration is completed, these pins have an internal high-value pull-up resistor that defines the logic level as High.

Production Test Methodology

The Xilinx XC4400EX/XL utilizes a Production Test Methodology which permits total testability of all testable faults. This is achieved through high fault coverage vectors generated by an Automatic Test Vector Generator (ATPG). The vectors are fed via both a serial and a parallel data path for the highest degree of fault observation.

One major advantage of Xilinx's test methodology is that the customer is not required to generate any production test vectors. Since this can often consume a great deal of time, Xilinx HardWire can save valuable customer engineering resources.

The user flip-flops in the design are converted into scannable elements. All flip-flops in the dedicated logic such as Configuration Emulation or Boundary Scan are also converted into scannable elements. These elements are then combined to form full-scan chains. Up to eight chains are used in order to reduce the total required test time. By using a combination of random and deterministic fault alogrithms, high fault coverage is achieved resulting in total testability of all testable faults.

ESD Considerations

The XC4400EX/XL has similar ESD protection as the XC4000EX FPGA, and is able to withstand ESD up to 2,000 volts. The HardWire is manufactured in CMOS process technology, and appropriate Electro-Static Discharge (ESD) handling precautions should be followed.

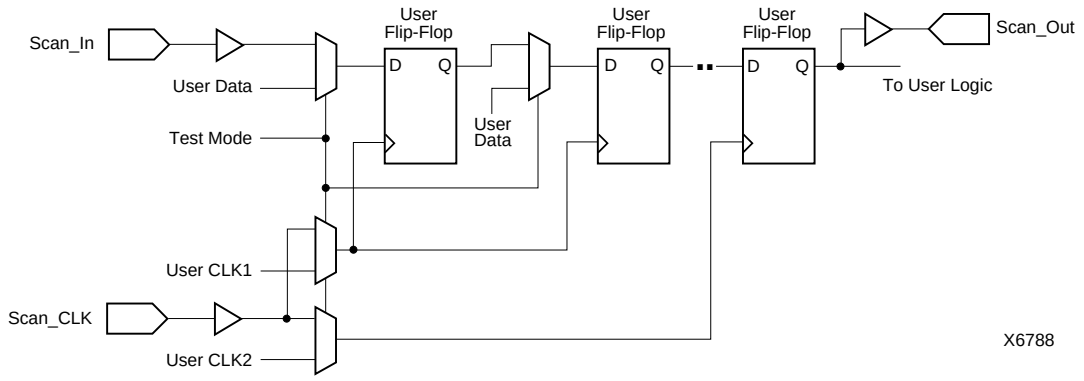

Figure 2. XC4400EX/XL Scan Chain