XC4300 Mask Options

Because HardWire Arrays emulate most of the configuration and start-up options in the programmable versions, there are various mask options that need to be specified to best emulate the programmable devices.

The options must be specified in the XC4300 HardWire Design Verification form and verified by Xilinx Applications Engineering before design signoff.

Most of these mask options are MAKEBITS program options that are specified at the time MAKEBITS is run. Use the *design.MBO* file, (the MAKEBITS option output file) as the starting point to pick the proper options.

Here are the list of options that need to be specified:

RESISTOR OPTIONS:

There are three pins with resistor options;

DONE, M1, and TDO.

The DONE pin has a PULL-UP only, if the circuit board does not have an external pull-up then the pull-up option must be ON. The start up circuitry of the HardWire devices relies on the DONE signal going high to get the start up sequence running.

The M1 pin has a PULL-UP or PULL-DOWN or NEITHER option.

The TDO (test DATA OUT) pin is a dedicated pin for Boundary Scan. This pin has a PULL-UP, PULL-DOWN or NEITHER option.

CONFIGURATION EMULATIONS OPTIONS:

The user must specify one:

1. Long Power-On-Reset

   This option emulates the complete power on reset time of the programmable devices. A typical power on delay is 11 to 33 ms for a slave device and 43 to 130 ms for a master device.

2. Short Power-On-Reset

   The power on reset time is dramatically reduced to allow for faster start-up. The device will start-up in the order of several µs with this option.

3. "Instant On"

   The HardWire device starts up immediately after power up, no configuration emulation is performed. The device goes into the start-up phase immediately.

START-UP OPTIONS:

There are three separate options to specify:

1. Start-up clock

   There is a choice of either using the configuration clock (CCLK) or a user supplied start-up clock (UCLK). The user clock option is for designs that require the start-up sequence to be synchronized with a particular system clock.

2. Sync-to-Done

   The start-up sequence can be further controlled by synchronizing it to the release of the Done pin (going high). This option can be used for designs that require synchronization of several devices starting up with one common event.

3. Start-up sequence options

   There are three events that happen during the start-up phase, each one of these can be specified to occur at a particular start-up clock cycle:

   Done pin goes active
   I/Os goes active
   Global Set/Reset gets released

   Each of these events can happen at either C1, C2, C3 or C4 if the CCLK is used for start-up. If the UCLK is used for start-up, the cycles are U1, U2, U3 or U4.