XC2318/L Mask Options

The 2318 HardWire array product has several mask options that need to be specified by the customer. Usually these options are MakeBits options in the FPGA versions.

These options must be specified in the XC2318 HardWire Design Verification Form and verified by Xilinx Applications before signing off the design.

There are a total of six mask options

1. INPUT VOLTAGE LEVELS

Just like the input buffers in the FPGA versions, the input buffers can either be TTL or CMOS. This option is on a ***global*** basis and ***not*** per input.

2. CONFIGURATION TIME INTERVAL

This option sets the time interval between initial power up condition and when the D/P-pin goes High. The 64 µs option is for designs that do not care how fast the HardWire array device powers up and becomes active. The 16 ms option emulates the initialization delay time of the FPGA device. When the device is set as "Master Mode" both of these periods are multiplied by 4 (this is to ensure that in designs containing multiple arrayss in a daisy chain, the slave mode devices will be ready before the master device is ready).

3. THERE ARE PULL-UP RESISTOR OPTIONS ON FOUR PINS

D/P-:	This option ***must*** be selected if there is **no** external pull-up on this node.
CCLK:	A pull-up can be added on the CCLK pin.
M0:	A pull-up can be added on the M0 pin.
PWRDWN:	A pull-up can be added on the PWRDWN pin.

4. HDC AND LDC OPERATION

If the FPGA version of the device is using the HDC and/or LDC signals to disable certain functions in the system, the HDC and LDC option(s) should be turned on. If the state of these pins are "don't care" or are not being used at all, then the option should be turned off.

5. DOUT DURING CONFIGURATION

The HardWire Array device has the ability to act as a Serial Master device. Although it will not swallow its own bitstream it can drive the CCLK line and pass the serial data to downstream slave devices. If the design needs this capability then pick the "DOUT = DIN" option, otherwise pick the "High Impedance" option.

6. OSCILLATOR

If the design uses the internal oscillator function, then the "Active" option should be selected.