Xilinx HardWire™ New Design Checklist

Submittal

- ☐ Customer submits all requirements for Xilinx review (drawings, packaging, processing, etc.).
- ☐ Customer completes HardWire Array Initial Design Submittal Form (page 6-3 HardWire Data Book).
- ☐ Customer checks and corrects all design rule violations (Run DRC with -I flag set to produce .XRP file).
- ☐ Customer submit .XRP file, “DRC – informational” files.
- ☐ Customer submits design files: ☐ .LCA ☐ .MBO ☐ .BIT ☐ .RBT (if available).
- ☐ Submit paper and electronic copy of schematics of .LCA DESIGN.
- ☐ Submit readable paper schematic of PC board showing the connections of FPGA on PCB.
- ☐ Send files and schematics to:

  Xilinx HardWire Product Manager
  2100 Logic Drive
  San Jose, CA 95124

- ☐ If files posted to E-mail or BBS, send backup copy via regular mail.
- ☐ Check with factory to be sure files have been received.

Verification

- ☐ Customer (name listed on submittal form) receives Xilinx Design Review Report
- ☐ Customer completes HardWire Array Design Verification Form (page 6-4 through 6-7 HardWire Data Book)
  - ☐ HardWire Options
  - ☐ Part Mark (Customer may define the last row of mark - one line only)
  - ☐ Exact version of design file to be used
- ☐ HardWire Custom Mark Request Form (page 6-8 HardWire Data Book) completed only if customer wants custom artwork, logo, or more than one mark line. Customer part number is included in Xilinx standard mark.
- ☐ HardWire Array pre-production Release Authorization Form signed if required (page 6-9 HardWire Data Book).
- ☐ Fax all forms to HardWire Marketing (408) 879-4780.
- ☐ Mail originals to HardWire Product Manager.

Proto Approval

- ☐ Customer completes HardWire Prototype Approval Form (page 6-10 HardWire Data Book).
- ☐ Fax Prototype Approval Form to HardWire Product Manager, follow-up original in mail.