HardWire™ Array Initial Design Submittal Form

Company Name _____ Date _____

Customer Name _____ E-mail _____

Address _____ City _____ State/Province _____

Country _____ Zip _____ Tel ( ) _____ Fax ( ) _____

Customer Internal Part Number _____

FPGA File Name and Revision Date (*Line 1 of .LCA file*) _____

Xilinx HardWire Array Device # _____ Temp. Grade (Check One) ☐ C ☐ I

(see cross reference table in HardWire Data Book for correct part number)

Package _____

☐ 5 V ☐ 3.3 V (Check One)

Max Clock Frequency _____

End Application For Device _____

Actual Function Performed In System _____

(information will be used for import/export purposes only)

Special Processing Requirements ☐ Yes ☐ No Customer Specification # _____

(Tape and Reel, Special Packaging, etc.)

Annual Production Volume (estimate) _____ Number of sockets using this design_____

Design Information Submitted to Xilinx:

FPGA Design File Name _____.XRP ("DRC – informational") File Name _____

Design Root Schematic/HDL Root Name _____

Timing Diagram of System I/Os _____

Design Block Diagram _____

Development Methodology Used:

Design entry method used (Check all that apply):

☐ Schematic (type) _____ ☐ X-BLOX ☐ XABEL ☐ Synthesis type

☐ VHDL ☐ Verilog ☐ Other

Simulation: ☐ Not done ☐ Done with _____

FPGA Device _____ Speed Grade _____ Package _____ Temperature Grade _____

Check all that apply:

☐ Peripherial Synchronous ☐ Master Serial ☐ Slave Serial ☐ Express™ Mode

☐ Peripherial Asynchronous ☐ Master Parallel Up ☐ Master Parallel Down

Is Configuration Emulation Needed? ☐ Yes ☐ No (INSTANT_ON ☐ Yes (NO_PROM)

Is IEEE1149.1 Boundary Scan Required? ☐ Always ☐ Only prior to configuration ☐ Never

RAM Description (Name, Size, Cycle, Time, etc.) _____

_____

For Xilinx Use Only

Marketing _____

Application Engineer _____

HPC Code _____