XC4400EX/XL, XC4400, XC5400 HardWire™ Array Design Verification Form

Company Name _____ Date _____

Customer Name _____ E-mail _____

Address _____ City _____ State/Province _____

Country _____ Zip _____ Tel ( ) _____ Fax ( ) _____

Customer Internal Part Number _____

FPGA File Name and Revision Date _____

Xilinx HardWire Array Device # _____ Temp. Grade (Check One) ☐ C ☐ I

(see cross reference table in HardWire Data Book for correct part number)

Package _____

☐ 5 V ☐ 3.3 V (Check One)

HardWire Array Options:

Configuration Mode:		*NO_PROM Required:*	
☐ Master Serial	☐ Slave Serial	☐ Master Serial	☐ Slave Serial
☐ Master Parallel Up	☐ Master Parallel Down	☐ Master Parallel Up	☐ Master Parallel Down
☐ Synchronous Peripherial	☐ Asynchronous Peripherial	☐ Synchronous Peripherial	☐ Asynchronous Peripherial
☐ Express ™ Mode	☐ INSTANT_ON	☐ Express™ Mode	☐ INSTANT_ON

Configuration Mode Emulation Needed? ☐ No ☐ Yes

Boundary Scan Needed? ☐ Always ☐ Only prior to configuration ☐ Never

Customer Special Options:

Special Processing Requirements ☐ Yes ☐ No Customer Specification # _____

(Tape and Reel, Special Packaging, etc.)

☐ Custom Marking Form Attached ☐ Standard Xilinx Marking

Customer Part Marking for Device Package (Optional - 11 Characters max.) ☐☐☐☐☐☐☐☐☐☐☐

HardWire Terms and Conditions:

Please put a check mark against the following items as applicable. All items need to be checked for a signoff.

☐ The application circuit board must have a provision for configuration program storage (i.e., XC17128, EPROM, etc.). The socket can be left unpopulated depends upon configuration mode options chosen when conversion to the HardWire device is made. The HardWire device is designed to provide a cost reduction path for existing fully debugged programmable designs.

☐ I certify that the above listed Design File and the revision date is the correct design.

☐ I have reviewed the Xilinx HardWire Review Report (including the list of potentially hazardous nets) and have determined that none of the issues raised will be a problem in the system.

☐ I authorize Xilinx to start the HardWire fabrication process.

Customer Name _____ Signature _____ Date _____

For Xilinx Use Only

Xilinx HardWire Design Center Manager: _____ Signature _____ Date _____

Xilinx Customer Service: _____ Signature _____ Date _____

NRE PO Number: _____

Xilinx Product Engineering Manager: _____

Xilinx Part Number (HPC Code): _____

Mask Set _____ Hole Mask _____

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