Synchronous DRAM Controller

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NMI Electronics Ltd.

Fountain House
Great Cornbow
Halesowen
West Midlands
B63 3BL
United Kingdom
Phone: +44 (0) 121 585 5979
Fax: +44 (0) 121 585 5764
E-mail: ip@nmi.co.uk
URL: www.nmi.co.uk

Features

- Single-chip SDRAM controller in a Xilinx XC9500 CPLD or XC4000XL FPGA
  - Separately optimized cores available for each architecture
  - XC9500 core is easy to use and modify due to predictable timing
  - XC4000XL core allows the SDRAM Controller to be integrated into much larger designs
- Designed for high speed, high performance applications
- Support for burst mode
- Utilizes auto refresh mode
- Supports multiple SDRAM types
- Available in source code format for ease of customization
- Can be customised by NMI, or the customer, with the following parameters:
  - SDRAM physical device type
  - SDRAM array width
  - Number of SDRAM banks
  - SDRAM interface timing
  - System interface

Applications

- Embedded systems in industrial, telecommunications, test or point-of-sale applications
- High performance peripheral equipment, e.g. printers

AllianceCORE™ Facts

Core Specifics[1]		
Device Family	XC4000XL	XC9500
CLBs/Macrocells	See Table 1	68[1]
IOBs Used		58[1]
System Clock f_{max}		50+ MHz[2]
Device Features Used	BUFGLS	GCLK

Supported Devices/Resources Remaining[1]		
	I/O	**CLBs**
XC4000XL	See Table 1	
XC95216-15 HQ208C[3]	108[1]	148[1]

Provided with Core	
Documentation	Design User Guide Sample files for top level module in VHDL
Design File Formats	XC9500: VHDL source XC4000XL: VHDL Source + .xnf netlist
Constraint Files	XC9500: None XC4000XL: .ucf & .ncd
Verification Tool	Viewlogic ViewSim
Schematic Symbols	None
Evaluation Model	Evaluation Board available extra
Reference designs & application notes	Application notes included in Design User Guide
Additional Items	None

Design Tool Requirements	
Xilinx Core Tools	Alliance 1.4
Entry/Verification Tool	Viewlogic Workview Office™ 7.4

Support
Support provided by NMI Electronics. 90 days e-mail and telephone support from NMI Electronics included in the Core price. Support does not cover user core modifications; please refer to “Core Modifications” section. Maintenance contracts available.

Notes (see also next page):

1. Assumes default configuration, see Functional Description.
2. Depends on device speed selected and other system device speeds. 50MHz operation has been verified with the i486DX4™ / XC95216-15 pairing and the i486DX4™ / XC4013XL-2 pairing. Speed in excess of 70MHz are possible with XC-9500-7 speed grades.

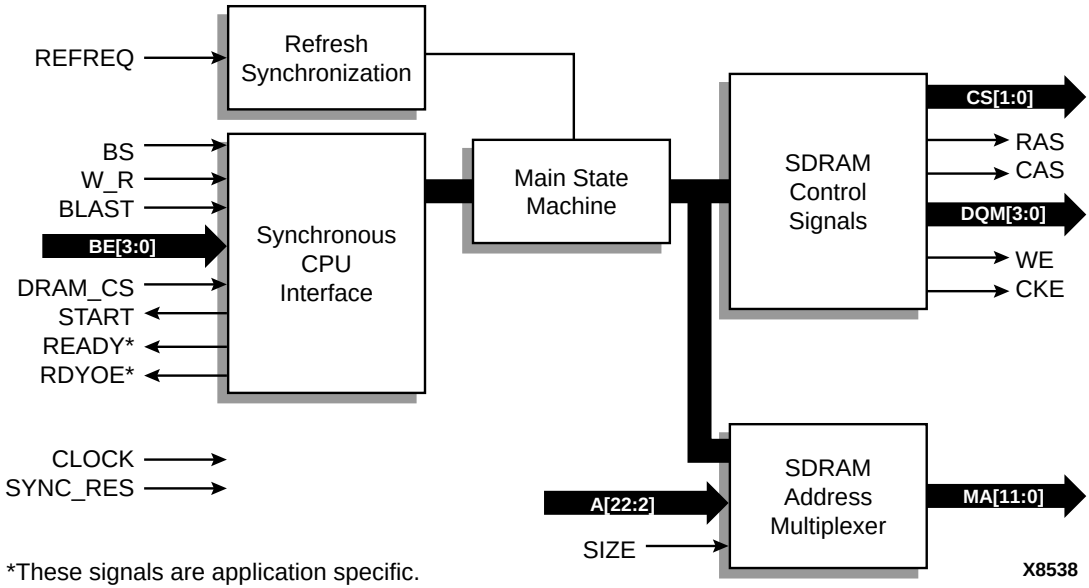

Figure 1: SDRAM Controller Block Diagram

Table 1: Example FPGA Core Implementations

	Example #1	Example #2	Example #3
System Interface	i486™	i486™	i486™
Number of SDRAM types	2	1	1
Number of SDRAM banks	2	2	1
Device	XC4013XL PQ240	XC4013XL PQ240	XC4013XL PQ240
CLB's Used	47	44	41
IOB's Used	58	55	54
CLB's Remaining	529	532	535
IOB's Remaining	134	137	138
System Clock fmax (-2)*	50 MHz	53 MHz	55 MHz
System Clock fmax (-09)*	63 MHz	66 MHz	70 MHz

* Performance figures verified using the Xilinx Timing Analyser

Notes (cont.):
3. The core has been proven in these devices but will work in similar devices with sufficient resources.

General Description

The SDRAM Controller is extremely flexible and can be configured to be used with most SDRAM types, most microprocessors and many other applications (see Core Modifications).

Functional Description

The SDRAM Controller is supplied as a single, VHDL source code module. Additional netlist and constraint files are provided with the FPGA core in order to guarantee design performance. The functional blocks shown in Figure 1 are for descriptive purposes only.

The default configuration of the SDRAM Controller is as follows:

- i486™-like CPU interface, including 4 word burst mode
- Two bank, 32 bit wide SDRAM array
- Support for typical 4M and 16M bit deep SDRAM's in x16 organizations

Synchronous CPU Interface

In order to achieve maximum performance the SDRAM Controller utilizes a fully synchronous interface to its host CPU or control logic. This does not, however, prevent the user from adding extra logic to create an asynchronous interface.

Main State Machine

The SDRAM Controller is state machine driven. The state machine, along with the input clock frequency, controls the timing of the SDRAM signals.

Refresh Synchronization

Refresh requests are not automatically generated by the SDRAM Controller as these can often be generated using other, lower frequency clocks which are available in many typical system designs. Due to this fact, the SDRAM Controller fully supports asynchronous refresh request inputs.

SDRAM Control Signals

The SDRAM control signals CS, RAS, CAS, DQM, WE and CKE are synchronously generated from the state machine outputs. Burst mode is supported and refresh utilizes CBR (auto) refresh.

SDRAM Address Multiplexer

The SDRAM address multiplexer can be configured to support most SDRAM sizes and organizations. The Design User Guide describes this process in detail.

Core Modifications

As supplied, the SDRAM Controller is designed for optimum performance in the 40MHz to 66MHz range, using "-15" SDRAM's. The system interface is i486™-like.

Many system designs will require that the core be modified before it can be used, especially with regard to the system interface. For this reason the core is supplied in source code format, and has been written with modification in mind. Furthermore, NMI will configure the FPGA version of the core to a customer specification and provide the necessary files to guarantee design performance.

The Design User Guide supplied with the core describes in detail how the core can be modified for different system interfaces, different clock speeds and different SDRAM types and speeds.

Please note that NMI support does not cover user core modifications. NMI offers design services, including core modifications, for additional cost.

Pinout

The pin functions of the SDRAM Controller core in its default configuration are shown in Table 2. The pinout is not fixed to any specific FPGA or CPLD I/O, and in many cases can be modified to suit the user's application.

Signal names are provided in the block diagram shown in Figure 1, and described in Table 2.

Verification Methods

Both functional and timing simulation have been carried out using ViewSim under Viewlogic Workview Office™. Simulation vectors used for verification are provided with the core in the form of ViewSim command files.

The core has been extensively tested on target hardware using an NMI developed evaluation card that is available for purchase separately.

Recommended Design Experience

Users should be familiar with VHDL and Xilinx design flows. Experience with microprocessor or similar system design is recommended. The core can easily be integrated into hierarchical VHDL designs.

Available Support Products

NMI has developed a Xilinx core evaluation card and this is available at additional cost.

Ordering Information

To make further enquiries or purchase the SDRAM Controller Core, please contact NMI directly at the location detailed on the front page. NMI also offers core integration and design services, the latter covering not only CPLD and FPGA design but also complete systems design.

NMI cores are purchased under a Licence Agreement, copies of which are available on request. NMI retains the right to make changes to these specifications at any time, without notice. *All trademarks, registered trademarks, or servicemarks are the property of their respective owners*

Table 2: Core Signal Pinout

Signal	Signal Direction	Description
System Interface Signals		
CLOCK	Input	Primary system clock; rising edge triggered
BS[1]	Input	Bus cycle start signal; active High. One CLOCK period wide. Identical to inverse of i486™ ADS signal.
W_R[1]	Input	System read or write cycle indicator. Cannot change state during whole bus cycle, or during a complete burst sequence; 0=read, 1=write.
BLAST[1]	Input	Burst last indicator. Active High for last bus cycle in a burst sequence.
BE[3:0] [1]	Input	Byte enable signals for default, 32 bit configuration. Writes are gated by state of byte enables; however all reads return 32 bit data; active Low.
DRAM_CS[1]	Input	Select signal for SDRAM Controller; active High. Must be active while BS is active for SDRAM Controller to respond to a bus cycle. Usually driven by an address decode.
A[22:2][1]	Input	System address lines for default, 32 bit configuration; active High.
START	Output	Indicates that a System access to SDRAM is pending
READY	Output	System Ready output; active High. Default configuration is for i486™ microprocessor. Output is usually system host specific.
RDYOE	Output	System Ready 3-state enable output; active High. Default configuration utilizes a 3-state driver for System Ready. Output is usually system host specific.
SDRAM Interface Signals		
CS[1:0]	Output	SDRAM CS (chip select) outputs; active Low
RAS	Output	SDRAM RAS output; active Low
CAS	Output	SDRAM CAS output; active Low
DQM[3:0]	Output	SDRAM DQM outputs; active Low.
WE	Output	SDRAM WE output; active Low
CKE	Output	SDRAM CKE output; active high
MA[11:0]	Output	Multiplexed row and column address outputs; active High. Multiplexing scheme determined by state of SIZE input.
Other Signals		
REFREQ	Input	Refresh request input; active High. May be asynchronous to CLOCK, and is rising edge triggered. Typical period is 15.625 microseconds maximum.
SIZE	Input	SDRAM module size selection input. This should not be changed during normal system operation. For default configuration this is: 0 - 4 MBit SDRAM's 1 - 16 MBit SDRAM's
SYNC_RES[1]	Input	System reset, synchronous to CLOCK; active High.

Note:
1. These signals must be applied synchronously to CLOCK.

Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
URL: www.xilinx.com

For general Xilinx literature, contact:

Phone: +1 800-231-3386 (inside the US)
+1 408-879-5017 (outside the US)
E-mail: literature@xilinx.com

For AllianceCORE™ specific information, contact:

Phone: +1 408-879-5381
E-mail: alliancecore@xilinx.com
URL: www.xilinx.com/products/logicore/alliance/tblpart.htm