XF-RSENC Reed Solomon Encoder

March 23, 1998 | Product Specification

Memec Design Services

Maria Aguilar, Project Coordinator
1819 S. Dobson Rd., Suite 203
Mesa, AZ 85202
Phone: +1 888-360-9044 (USA)
+1 602-491-4311 (outside the USA)
Fax: +1 602-491-4907
E-mail: info@memecdesign.com
URL: www.memecdesign.com

Features

- High Speed Reed-Solomon Encoder Core
- Core design can be customized for any encoder using the following parameters:
  - Primitive polynomial
  - Generator polynomial
  - Symbol size
  - Number of parity symbols
- Message block length configured by end user
- Cores can be concatenated to build extended codes
- Supports symbol rates greater than 60MHz
- All registers clock by single clock
- All registers enabled by single clock enable allowing ease of interface to larger system

Applications

- DTV/HDTV broadcast
- Data communication channels
- Data storage systems (i.e. CD-ROM or hard disk)

AllianceCORE™ Facts

Core Specifics[1]	
Device Family	XC4000E
CLBs Used	See Table 1
IOBs Used	
System Clock f_{max}	
Device Features Used	ROMs
Supported Devices/Resources Remaining[1]	
See Table 1	
Provided with Core	
Documentation	Core Documentation
Design File Formats	XNF netlist VHDL or Verilog RTL
Constraint Files	VHDL or Verilog Testbench
Verification Tool	None
Schematic Symbols	None
Evaluation Model	None
Reference designs & application notes	Example Implementation in VHDL or Verilog
Additional Items	Warranty by MDS
Design Tool Requirements	
Xilinx Core Tools	XACTstep 5.2.1/6.0.1 or Alliance 1.2
Entry/Verification Tool	VHDL or Verilog
Support	
Memec Design Services warrants that the design delivered by Memec Design Services will conform to the design specification. This warranty expires 3 months from the date of delivery of the design database. Contact Memec Design Services for the Design License Agreement with complete Terms and Conditions of Sale.	

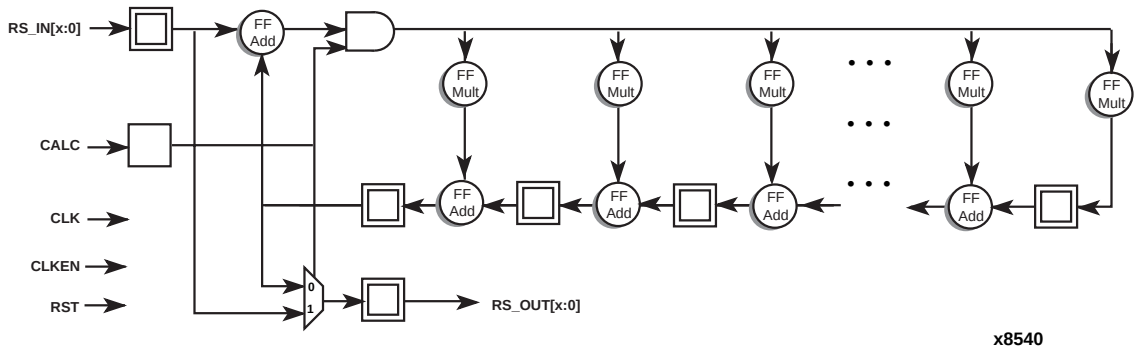

Figure 1: Reed Solomon Encoder Functional Block Diagram

General Description

The XF-RSENC is a Reed-Solomon Encoder for use in communication or data storage systems requiring forward error correction capabilities. The core is optimized to the Xilinx XC4000 family of FPGAs for speed and area. Table 1 shows implementation statistics of example cores.

The XF-RSENC core is delivered as an XNF netlist, or as VHDL or Verilog RTL code. Each core is customized to the needs of the user's application.

Table 1: Example Implementations

	Example #1	Example #2
Parity Symbols	16	8
Bits/Symbol	8	8
Device	XC4003E-1	XC4003E-1
CLBs	84	45
CLBs Remaining	16	55
IOBs	19	19
IOBs Remaining	42	42
CLKIOBs	1	1
Max Symbol Rate	60MHz	63MHz

Functional Description

The functional block diagram of the XF-RSENC is shown in Figure 1. The design is modular in structure and can be configured to implement any number of parity symbols.

All registers are driven by common clock, clock enable and reset (async.) signals. This provides ultimate flexibility for larger systems. The registers are clocked on the rising edge.

A single input controls whether the core is calculating the parity (high) or shifting out the calculated parity (low). Logic external to the core is required to generate this control signal. This allows the user to vary the message block length as required. Examples of the external logic are provided with the core.

FFADD Block

This block performs the Finite Field modulo addition over the appropriate Galois Field.

FFMULT Block

This block performs the Finite Field Multiplication, over the appropriate Galois Field, of a constant and the input symbol value. The constant corresponds to a coefficient determined from the Generator and Primitive Polynomials.

Core Modifications

Memec Design Services will customize a deliver a Xilinx netlist version of this core that meets your requirements. To do so, fax or email the following information to MDS directly:

- Your name, company name, address, phone number and email ID
- Primitive Polynomial (e.g. $x^8 + x^4 + x^3 + x^2 + 1$)
- Generator Polynomial (e.g. $(x+a^1)(x+a^2)$...)
- Number of errors corrected

Pinout

The pinout of the XF-RSENC core has not been fixed to specific FPGA I/O, allowing flexibility with a user's application. The signal names are provided in Figure 1 and Table 2.

Table 2: Core Signal Pinout

Signal	Signal Direction	Description
RS_IN[*x*:0]	Input	Input data symbol
CALC	Input	Parity calculate/shift
CLK	Input	System clock
CLKEN	Input	Clock enable; active high
RST	Input	System Reset; active high
RS_OUT[*x*:0]	Output	Output data symbol

Verification Methods

Basic functional simulation has been performed on the XF-RSENC using Verilog or VHDL. (Simulation vectors used for verification are provided with the core).

Recommended Design Experience

A basic understanding of Reed-Solomon encoding will help in using this core. Users should be familiar with Verilog or VHDL synthesis and simulation as well as Xilinx design flows.

Ordering Information

The XF-RSENC Core is customized for your application (see Core Modifications). The core is provided under license from Memec Design Services for use in Xilinx programmable logic devices and Xilinx HardWire™ gate arrays. To purchase or make further inquiries about this or other Memec Design Services' products, contact MDS directly.

Information furnished by Memec Design Services is believed to be accurate and reliable. Memec Design Services reserves the right to change specifications detailed in this data sheet at any time without notice, in order to improve reliability, function or design, and assumes no responsibility for any errors within this document. Memec Design Services does not make any commitment to update this information.

Memec Design Services assumes no obligation to correct any errors contained herein or to advise any user of this text of any correction, if such be made, nor does the Company assume responsibility for the functioning of undescribed features or parameters. Memec Design Services will not assume any liability for the accuracy or correctness of any support or assistance provided to a user.

Memec Design Services does not represent that products described herein are free from patent infringement or from any other third-party right. No license is granted by implication or otherwise under any patent or patent rights of Memec Design Services.

Memec Design Services products are not intended for use in life support appliances, devices, or systems. Use of a Memec Design Services product in such application without the written consent of the appropriate Memec Design Services officer is prohibited.

Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
URL: www.xilinx.com

For general Xilinx literature, contact:

Phone: +1 800-231-3386 (inside the US)
+1 408-879-5017 (outside the US)
E-mail: literature@xilinx.com

For AllianceCORE™ specific information, contact:

Phone: +1 408-879-5381
E-mail: alliancecore@xilinx.com
URL: www.xilinx.com/products/logicore/alliance/tblpart.htm