



YCrCb2RGB Color Space Converter

March 23, 1998

Product Specification



Perigee, LLC

Donwood Office Park
 Suite 213
 135 Old Cove Road
 Liverpool, NY 13090 USA
 Phone: +1 315-453-7842
 Fax: +1 315-453-7917
 E-mail: info@PerigeeLLC.com
 URL: www.PerigeeLLC.com

Features

- Converts digital component video (YCrCb) to digital RGB
- Optimized for XC4000E/XL architecture
 - Low CLB count/MIPS ratio
- Supports two NTSC video streams (square pixel) in slowest XC4000E FPGA
 - Up to 90 MHz operation
 - One conversion per clock cycle
- All outputs properly rounded and saturated
 - No external logic needed to handle these conditions
- Low latency
- Fully relationally placed for consistent performance
 - Supports Xilinx XACTstep 5.2.1/6.0 and M1 development tools

Applications

- Real-time component video to RGB graphics conversion

AllianceCORE™ Facts		
Core Specifics¹		
Device Family	XC4000E	
CLBs Used	175	
IOBs Used	48 ¹	
CLKIOBs Used	1	
System Clock f_{max}	80 MHz	
Device Features Used	SelectRAM™, Fast Carry Logic, RPM	
Supported Devices/Resources Remaining¹		
	I/O	CLBs
XC4010E-1	118 ¹	225
Provided with Core		
Documentation	Core Design Document	
Design File Formats	.xnf, .ngo netlist ViewDraw Source available extra	
Constraint Files	None	
Verification Tool	ViewSim	
Schematic Symbols	ViewDraw	
Evaluation Model	None	
Reference designs & application notes	None	
Additional Items	None	
Design Tool Requirements		
Xilinx Core Tools	XACTstep 5.2.1/6.0 Alliance M1.3	
Entry/Verification Tool	Viewlogic	
Support		
Support provided by Perigee, LLC.		

Note:

1. Assuming all core signals are routed off-chip.

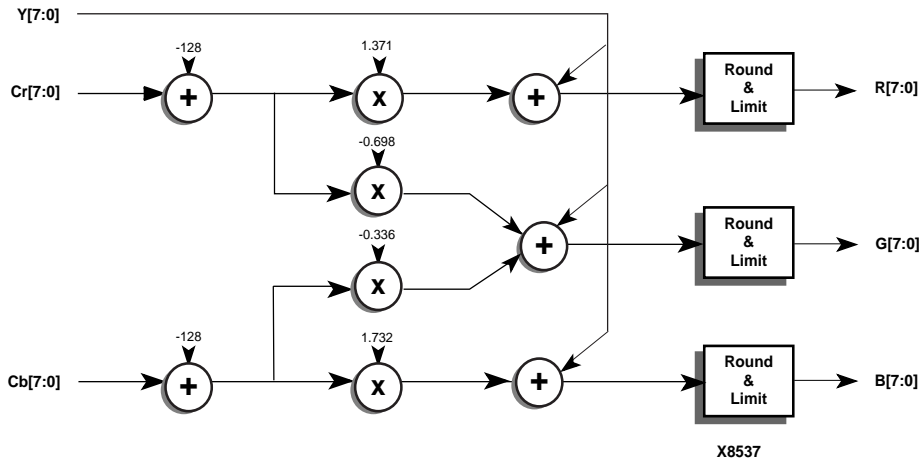


Figure 1: YCrCb2RGB Color Space Converter Block Diagram

General Description

Luminance and color difference coded signals (YCrCb) are generated by many component video systems. Conversion to RGB is necessary to feed a display device requiring RGB input. Figure 1 shows the converter block diagram.

Functional Description

The YCrCb to RGB color space converter is designed to perform the following equations:

$$R' = Y + 1.371(Cr - 128)$$

$$G' = Y - 0.698(Cr - 128) - 0.336(Cb - 128)$$

$$B' = Y + 1.732(Cb - 128)$$

The conversion is complete in 6 clock cycles and both input and output are registered for consistent routing and timing.

Multipliers

The multipliers are constant-coefficient and are optimized for the Xilinx architecture.

Rounding and Limiting

Intermediate calculations are performed at greater bit widths. The limiting function protects against both positive and negative overflow conditions. The rounder correctly rounds to an 8-bit result. The aggregate of these two func-

tions produces an 8-bit result that is sufficiently conditioned for downstream processing or D/A conversion for video display.

Core Modifications

The core, as described in this data sheet, is available free from Perigee. Modified version of this core or similar cores are available for purchase. Examples include:

- YCrCb2RGB variants, including lower performance versions that use fewer CLBs
- Adjusting color channel bit widths
- RGB2YCrCb color space correctors
- Gamma-correctors

Contact Perigee directly for more information.

Pinout

The pinout of the color space converter has not been fixed to specific FPGA I/O, allowing flexibility with a user's application. Signal names are shown in Table 1.

Verification Methods

The core has been tested with in-house developed test vectors that are provided with the core.

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
Y[7:0]	Input	Luminance
Cr[7:0]	Input	Color Red
Cb[7:0]	Input	Color Blue
CLK	Input	Clock; uses one FPGA CLKIOB pin.
R[7:0]	Output	Red
G[7:0]	Output	Green
B[7:0]	Output	Blue

Recommended Design Experience

Users should be familiar with video systems and Xilinx development tools.

Ordering and Company Information

The product, as described, is available free directly from Perigee, LLC. Perigee, LLC is a technology company specializing in new product development. Perigee's focus is electronic system design, partitioning and development. They are committed to leveraging the ever-growing size of programmable logic without sacrificing time-to-market. To this goal, Perigee offers IP cores as well as customization, FPGA/CPLD design and integration services. Their design solutions range from proof of concept designs through final product solutions.

Perigee offers services and contract engineering for varying levels of development from logic design to system level embedded and bus-based products. These services include:

- IC design, VHDL or schematic based
- Turnkey hardware/software/firmware development

- System design
- Board design
- DSP and image processing
- Embedded firmware
- GUI and Application software

Perigee's particular area of expertise is in digital video and digital signal processing applications. For more information on Perigee, their products and services, contact them directly.

Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
URL: www.xilinx.com

For general Xilinx literature, contact:

Phone: +1 800-231-3386 (inside the US)
+1 408-879-5017 (outside the US)
E-mail: literature@xilinx.com

For AllianceCORE™ specific information, contact:

Phone: +1 408-879-5381
E-mail: alliancecore@xilinx.com
URL: www.xilinx.com/products/logiccore/alliance/tbpart.htm