XF9128 Video Terminal Logic Controller

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Product Specification

Maria Aguilar, Project Coordinator
Memec Design Services
1819 S. Dobson Rd., Suite 203
Mesa, AZ 85202
Phone: +1 888-360-9044 (USA)
+1 602-491-4311
Fax: +1 602-491-4907
E-mail: info@memecdesign.com
URL: www.memecdesign.com

Features

- Software & function compatible with Industry Standard CRT 9128
- Built-in oscillator (XC3190A only)
- Built-in video shift register
- External character generator in LCA configuration ROM
- Bi-directional smooth scroll capability
- Visual attributes include reverse video, intensity control, underline and character blank
- Separate HSYNC, VSYNC and VIDEO outputs
- Composite Sync (RS170 compatible) output
- Absolute (RAM address) cursor addressing
- Software enabled non-scrolling 25th data row available with 25 data row/page display
- Non-interlace display format
- Separate display memory bus eliminates contention problems
- Fill (erase) screen capability
- Standard 8-bit microprocessor data bus interface
- Wide graphics with six independently addressable segments per character space
- Thin graphics with four independently addressable segments per character space
- Single +5V supply
- TTL or CMOS compatible I/O
- Additional optional video parameters (contact MDS for details and availability):
  - Dots per character block (6-8)
  - Raster scans per data row (6-12)
  - Characters per data row (32, 48, 64, 80)

AllianceCORE™ Facts

Core Specifics		
Device Family	XC3190A	XC4005E
Macrocells Used	287	190
IOBs Used	62[1]	61[1]
System Clock fmax	14MHz[2]	14MHz[2]
Device Features Used	Internal oscillator	None

Supported Devices/Resources Remaining		
	I/O	**CLBs**
XC3190A-5PC84C[3]	8[1]	33
XC4005E-4PQ100C[3]	16[1]	6

Provided with Core	
Documentation	Core schematics Implementation instructions
Design File Format	ViewLogic Workview Office
Verification Tool	Simulation vectors for ViewLogic's ViewSim or Workview Office
Schematic Symbols	ViewLogic
Constraint Files	None
Evaluation Model	None
Reference designs & application notes	None
Additional Items	Warranty by MDS

Design Tool Requirements	
Xilinx Core Tools	XACTstep 6.0.1 for the XC3190; Alliance 1.3 for the XC4005E
Entry/Verification Tool	ViewLogic PRO series or Workview Office

Additional Information
The Video Terminal Controller Logic Core is provided under license from Memec Design Services for use in Xilinx programmable logic devices and Xilinx HardWire™ gate arrays

Support
Support provided by Memec Design Services

Notes:
1. Assuming all core signals are routed off-chip.
2. 4MHz maximum recommended clock speed to meet industry standard specifications.
3. Specific devices are minimum size and speed recommended - the core will work in any larger or faster devices from the same families.

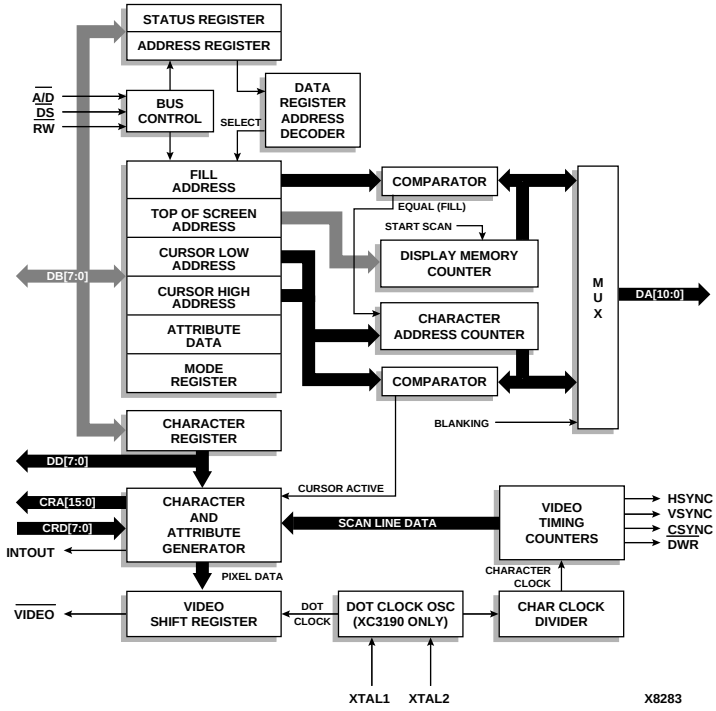

Figure 1: XF9128 Block Diagram

- Data rows per page (8, 10, 12, 16, 20, 24, or 25)
- Horizontal blanking (8-64 characters)
- Horizontal sync front porch (0-7 characters)
- Horizontal sync duration (1-64 characters)
- Horizontal sync polarity
- Two values of vertical blanking
- Two values of vertical sync duration (1-16 scan lines)
- Vertical sync polarity
- External 128-character 5x8-dot font
- Character/cursor underline position
- Scan row and column for thin graphics entity segments
- Scan rows and columns for wide graphics entity elements).

Applications

- ASCII terminal controllers
- Replacement for obsolete Video Terminal Logic Controllers
- Integration of video terminal control logic into an FPGA with other system logic

General Description

The XF9128 Video Terminal Logic Controller (VTLC) Core is a programmable video display controller that combines video timing, video attributes, alphanumeric and graphics generation, smooth scroll, and screen buffer interface functions.

The XF9128 VTLC incorporates many of the features required in building a low-cost, yet versatile, display interface. An external programmable 128-character font provides a full-ASCII character set. Wide graphics allow plotting and graphing capabilities while thin graphics and visual attributes can make the display of forms straight-forward.

The VTLC Core regulates the data flow with data strobe (DS-) and read/write (R/W) enable signals for use with the 6500, Z80®, 68000, and similar microprocessors and microcomputers. The VTLC provides two independent data buses; one bus that interfaces to the processor, and one that interfaces to the display memory. Data is transferred to the display memory from the processor through the XF9128, eliminating contention problems and the need for a separate row buffer.

An internal crystal oscillator is included in the XC3190A version of the VTLC Core, therefore requiring only an external crystal to operate. Pre-programmed constants for critical video timing simplify programming, operation, and improve reliability. A separate non-scrolling status line (enabled or disabled by the processor) is available for displaying system status.

Functional Description

The XF9128 is partitioned into numerous functional blocks as shown in Figure 1, and described below.

XF9128 VTLC Internal Registers

Addressing of the XF9128 internal data registers is accomplished through use of the A/D- and R/W- select inputs qualified by the DS- strobe.

Address Register

Writing to a byte to the ADDRESS register will select the specified register the next time the processor writes to or reads the VTLC data registers.

Status Register

When reading the STATUS register, the DONE bit (DB7 of STATUS Register) will represent the current status of the CHARACTER register.

Data Registers

- FILADD (Fill Address): This register contains the RAM address of the character following the last address to be billed.
- TOSADD (Top of Screen Address): This register contains the RAM address of the first character displayed at the top of the video monitor screen.
- CURLO (Cursor Low): This register contains the eight lower order address bits of the RAM cursor address.
- CURHI (Cursor High): This register contains the three higher address bits of the RAM cursor address (DA10, DA9, DA8).
- ATTDAT (Attribute Data): This register specifies the visual attributes of the video data and the cursor presentation.
- MODE: The AUTO INCREMENT bit in this register specifies whether or not the display memory character address is automatically incremented by the VTLC after every read/write of the CHARACTER register. Note: the visible cursor position is not affected.
- CHARACTER: This register allows access to the display memory for both type transfers and FILL operations.
- CHARACTER SET: Using the DB7-DB0 data bus I/O pins and the MOD SEL bit in the ATTDAT register, the user can address 128 characters, a six segment “wide graphics” and a four segment “thin graphics” entity.

Bus Control

The Bus Control block decodes the control signals from the microprocessor to direct data to/from the registers in the VTLC.

Character and Attribute Generator

This block modifies character cells as directed by the attribute data associated with each character.

Video Shift Register

This block is simply the high-speed shift register that generates the serial video stream.

Video Timing Counters

These counters generate horizontal sync, vertical sync, and composite sync. It also generates the Write Timing for the display memory.

Display Memory Counter

This counter is initialized from the Top Of Screen Address register and counts through a full screen of data.

Cursor Active Comparator

This comparator compares the Cursor Address registers to the Display Memory Counter and informs the Character and Attribute Generator block when the Display Memory Counter is equal to the Cursor Address register.

Fill Address Comparator

This comparator is used to define the boundaries of the area in memory to be filled with a particular character.

Character Address Counter

This counter is used in conjunction with the Display Memory Counter to generate the address for the Display Memory.

DOT Clock Divider

This is the primary scaler for the crystal frequency which generates DOT Clock.

Character Clock Divider

This is the divider which counts the number of dots per character to generate Character Clock.

MUX

The MUX controls the source of address to the display memory.

Core Modifications

The XF9128 is designed to meet or exceed the AC Specifications of the Stand Microsystems Corporation's CRT 9128. However, in most cases the Timespecs can be tightened significantly. In all cases, post-route timing analysis should be performed to verify performance. Implementation and other customizing are available through Memec Design Services.

Pinout

The XF9128 may be implemented internally with the users design or as stand-alone logic with the pinout (XC3190A only) that is provided with the Core. Signal names are provided in the block diagram shown in Figure 1 and in Table 1.

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
A/D-	Input	**Register Select**: state of this pin determines if data is being read from, or written to address or status register, or a data register.
DS-	Input	Causes data to be strobed into or out of VTLC from microprocessor data bus depending on state of R/W signal.
R/W-	Input	**Read/Write Select**: determines whether processor is reading data from or writing data into VTLC (high for read, low for write).
DB[7:0]	In/Out	**Processor or Data Bus**: 8-bit bi-directional processor data bus.
DD[7:0]	In/Out	8-bit bi-directional data bus to display memory.
CRA[15:0]	Output	Address to external character ROM.
CRD[7:0]	Input	Data from external character ROM.
XTAL1,2 (XC3190A) XTAL1 (XC4005E)	Input	**External Crystal**: external TTL level clock may be used to drive XTAL1 (in which case XTAL2 is left floating). Note: 4005E has no XTAL2 connection.
DA[10:0]	Output	11-bit address bus to display memory
HSNYC	Output	Horizontal sync signal or monitor.
VSNYC	Output	Vertical sync signal or monitor.
CYSNYC	Output	Used to generate RS170 compatible composite VIDEO signal for output to a composite VIDEO monitor.
DWR-	Output	**Display Write:** Write strobe to display memory.
INTOUT	Output	intensity level modification attribute bit (synchronized with video data output).
VIDEO-	Output	**Video Output**: digital TTL waveform used to develop VIDEO and composite VIDEO signals to monitor. Signal polarity is: HIGH = BLACK LOW = WHITE

Core Assumptions

The character generator ROM and the ROM that contains the VTLC macro bitstream are the same ROM. The FPGA loads itself from the ROM using master-parallel mode and then the VTLC macro uses the same ROM for the character look-up table.

Verification Methods

Basic functional simulation has been performed on the XF9128 using ViewSim. (Simulation vectors used for verification are provided with the core). This design was also physically tested in one application using the XC3190A without any problem.

Recommended Design Experience

Users should be familiar with ViewLogic PRO series or Workview Office schematic entry and with Xilinx FPGAs. Users should also have experience with microprocessor systems using video system controllers.

Ordering Information

The XF9128 Video Terminal Logic Controller Core is provided under license from Memec Design Services for use in Xilinx programmable logic devices and Xilinx HardWire gate arrays. Please contact Memec for pricing and more information.

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Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
URL: www.xilinx.com

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Phone: +1 800-231-3386 (inside the US)
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For AllianceCORE™ specific information, contact:

Phone: +1 408-879-5381
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