Low-Speed USB Function Controller

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Inventra™

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Features

- Fully compliant to USB 1.0 specification
- 100% programmable single-chip solution with customizable back-end functionality
- Pre-defined implementation for predictable timing in Xilinx FPGA or HardWire™
  - Push button scripts to place and route, and generate Xilinx bit files
  - Xilinx-optimized place and route constraint and guide files
- Fully verified design
  - Simulated using Inventra USB Simulation Model
  - Hardware-proven in a Xilinx FPGA at USB-IF sponsored interoperability workshop
  - Complete synchronous design
- Provides a high level interface that shields the firmware from USB protocol details
- Complete device configuration
- Compatible with both OpenHCI and Intel UHCI standards
- Supports low-speed (1.5 Mbps) functions
- Endpoint 0 is Control endpoint
  - Maximum packet capacity is 8 Bytes
- IN Endpoint for Interrupt data transfers
  - Maximum packet capacity for In Endpoint is user selectable from 1-8 Bytes
- Automatic Data Retry, Error recovery, and Data Toggle synchronization performed in hardware
- Includes the following error handling capabilities
  - CRC errors
  - Response Time Out
- ID error
- External interface to Phillips *IPDIUSBP11* USB transceiver

AllianceCORE™ Facts

Core Specifics		
Device Family	XC4000E	
CLBs Used	600	
IOBs Used	29[1]	
System Clock f_{max}	6MHz[2]	
Device Features Used	RAM, 3-state buses, carry logic	
Supported Devices/Resources Remaining		
	I/O	**CLBs**
XC4025E-4 HQ240	164[1]	304
Provided with Core		
Documentation	XC4000E/CX5215 Datasheets Core documentation Sample files for top level module in Verilog HDL	
Design File Formats	XNF Netlist Verilog Source RTL Available	
Constraint Files	Timespec, .cst, .tnm files	
Verification Tool	Verilog	
Schematic Symbols	Viewlogic, ORCAD	
Evaluation Model	Evaluation Board available extra	
Reference designs & application notes	None	
Additional Items	Firmware for microcontroller available for nominal cost	
Design Tool Requirements		
Xilinx Core Tools	XACTstep 5.2.1/6.0.1	
Entry/Verification	Verilog RTL	
Support		
Support provided by Inventra		

Notes:

1. Assuming all core signals are routed off-chip.
2. For 10-15% of design, remaining logic operates at 1/4 max clock.

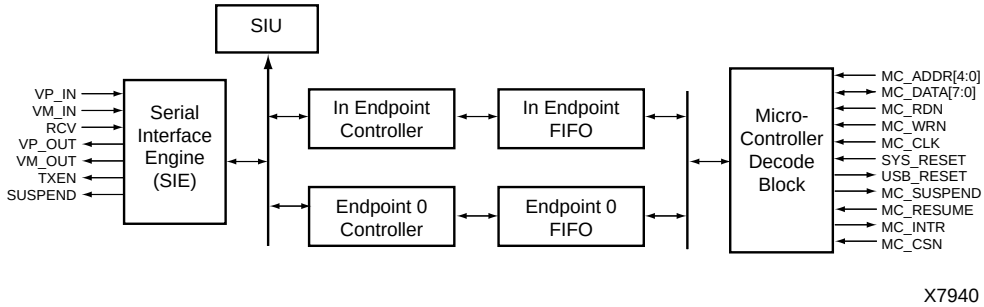

Figure 1: Low-Speed USB Function Controller Block Diagram

Applications

- Low speed (1.5 Mbps) functions requiring a microcontroller interface
- Embedded applications in telecommunication, industrial, medical or point-of-sale systems

General Description

The Low-Speed USB Function Controller is flexible, and has been optimized for a variety of low-speed, microcontroller-based applications. It includes all functionality for a complete function controller interface using one Xilinx FPGA plus an external Phillips IPDIUSBP11 USB transceiver.

Functional Description

The USB Function Controller core is partitioned into six modules as shown in Figure 1 and described below. A sample top-level Verilog RTL file is provided so the user can instantiate the netlist for synthesis and simulation environments.

Serial Interface Engine (SIE)

The SIE handles NRZI decoding/encoding, CRC generation and checking, bit-stuffing and timeout. The SIE generates the PID, deciphers packets, and transmits and receives packets from the host. The SIE uses a 6 MHz clock for data and clock extraction. It also provides the interface signals for the Phillips IPDIUSBP11 USB transceiver.

Serial Interface Unit (SIU)

This block handles endpoint address decoding for USB packets.

Endpoint 0 Controller

The Endpoint 0 controller handles control transfers.

In Endpoint Controller

The IN Endpoint controller handles TX data transfer between host and function. The IN Endpoint is configured as an interrupt endpoint.

FIFO

The core has a bi-directional 8-Byte Endpoint 0 FIFO to handle control transfers. It also has an IN Endpoint FIFO with a maximum 8-Byte capacity to handle interrupt data from the microcontroller.

Microcontroller Decode Block

The microcontroller interface is generic, with Address and Data bus interfaces, and Read and Write control signals. It generates an interrupt to the micro controller when data is ready, and when data has been successfully transmitted. The core performs hardware retries and data buffering. This improves performance by reducing the burden on the microcontroller. The microcontroller does address decoding for internal registers (i.e. FIFO Data Register).

This interface is asynchronous. All signals (MC_WRN, MC_RDN) are synchronized internally. MC_WRN and MC_RDN are active low.

Core Modifications

The Low-Speed USB Function Controller Core is modular in design, making modifications relatively simple. If you are interested in obtaining a version of the core that differs from this product description, then contact Inventra directly. Inventra can provide custom versions of the core, including support for the following:

- Changing Endpoint FIFO depths.
- Flexible interfaces for Mitsubishi 37690, Zilog Z80 and Atmel 89C51 microcontrollers.
- Modification for audio- or video-specific applications.
- Support for full-speed functions is provided by the Full-Speed Function Controller Core, also available from Inventra. A similar product description for that function is available from both Inventra and Xilinx.

Pinout

The pinout of the Low-Speed USB Function Controller has not been fixed to specific FPGA I/O, allowing flexibility with a users application. Signal names are provided in the block diagram shown in Figure 1 and Table 1 below.

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
Transceiver Interface Signals		
VP_IN	Input	D+ input from XCVR
VM_IN	Input	D- input from XCVR
RCV	Input	Differential data from XCVR
VP_OUT	Output	D+ output from XCVR
VM_OUT	Output	D- output from XCVR
TXEN	Output	Enable for XCVR, active low
SUSPEND	Output	Suspend signal, puts XCVR into suspend mode
Microprocessor Interface Signals		
MC_ADDR [4:0]	Input	Microcontroller Address bus
MC_DATA [7:0]	In/Out	Microcontroller Data bus
MC_RDN	Input	Read Strobe, active low
MC_WRN	Input	Write Strobe, active low
MC_CLK	Input	6 MHz microcontroller clock input
SYS_RESET	Input	System Reset, active high
USB_RESET	Output	USB Reset, active low
MC_SUSPEND	Output	Interrupt signal generated during SUSPEND signal on USB, active high; provided as dedicated bit in Power Mgmt register
MC_RESUME	Output	Interrupt signal generated during RESUME signal on USB, active high
MC_INTR	Output	Microcontroller Interrupts, active low
MC_CSN	Input	Acts as a Block Select to microcontroller address, active low

Table 2: Microcontroller I/O Timing

Signal	Setup	Hold
MC_ADDR	3 ns	0 ns
MC_DATA	3 ns	0 ns
MC_WRN	3 ns	0 ns
MC_RDN	3 ns	0 ns

Verification Methods

The Low-Speed USB Function Controller core has been tested with products from over 30 system manufacturers at USB-IF sponsored compliance workshops. The Xilinx-based implementation of the core passed all interoperability testing with numerous host, BIOS and peripheral products.

The core has undergone extensive testing using Inventra's USB Simulation Model that includes a host controller, function controller and protocol analyzer. This model is available separately from Inventra.

Recommended Design Experience

Knowledge of the USB specification is required. The user must be familiar with HDL design methodology as well as installation of Xilinx netlists in a hierarchical design environment.

Available Support Products

Inventra supplies a complete line of hardware and software products designed to aid integration of this core into your application. These are available for additional cost. Contact Inventra for more information.

- USB Function Evaluation Board
- USB Simulation Model

Ordering Information

This product is available from the AllianceCORE™ partner listed on the first page. Please contact the partner for pricing and more information.

Related Information

Universal Serial Bus Implementor's Forum

The USB-IF publishes USB specifications and related documents:

- USB Specification, Rev. 1.0
- USB Compliance Checklist
- USB Device Class Definitions for Human, Audio, Video and Mass Storage devices

Contact:
USB Implementor's Forum
URL: www.usb.org

Philips Semiconductor

For additional information on the Philips *IPDIUSBP11* USB transceiver chip, contact:

Philips Semiconductors
URL: www.semiconductors.philips.com

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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