



Full-Speed USB Function Controller

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Product Specification



The Power to Create

Inventra™

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Features

- Fully compliant to USB 1.0 specification
- 100% programmable single-chip solution with customizable back-end functionality
- Pre-defined implementation for predictable timing in Xilinx FPGA or HardWire™
 - Push button scripts to place and route, and generate Xilinx bit files
 - Xilinx-optimized place and route constraint and guide files
- Fully verified design
 - Simulated using Inventra USB Simulation Model
 - Xilinx FPGA-proven in hardware at USB-IF Plug-Fest workshop
 - Complete synchronous design
- Provides a high level interface that shields the firmware from USB protocol details
- Complete device configuration
- Compatible with both OpenHCI and Intel UHCI standards
- Supports full-speed (12 Mbps) functions
- Support for 3 Endpoints (0, In and Out)
 - On-chip Endpoint FIFOs
 - Each can handle Bulk, Interrupt/Status Change and Isochronous data transfers
 - Endpoints interface to a microcontroller
 - Maximum packet capacity for Endpoint 0 is 8-Bytes
 - Packet capacity for In/Out Endpoints is selectable at 8-, 16- or 32-Bytes
- Flexible interface for Mitsubishi 37690, Zilog Z80 or Atmel 89C51 microcontrollers
 - Automatic Data Retry, Error recovery, and Data Toggle synchronization performed in hardware.

AllianceCORE™ Facts		
Core Specifics		
Device Family	XC4000E	
CLBs Used	720 ¹	
IOBs Used	29 ²	
System Clock f _{max}	48 MHz ³	
Device Features Used	RAM, 3-state buses, carry logic	
Supported Devices/Resources Remaining		
	I/O	CLBs
XC4025E-3 HQ240	164 ²	304
Provided with Core		
Documentation	XC4000E Datasheet Core documentation Sample files for top level module in Verilog HDL	
Design File Formats	XNF Netlist Verilog Source RTL Available	
Constraint Files	Timespec, .cst and .tnm files	
Verification Tool	Verilog	
Schematic Symbols	Viewlogic, ORCAD	
Evaluation Model	Evaluation Board available extra	
Reference designs & application notes	None	
Additional Items	Firmware for microcontroller available for nominal cost	
Design Tool Requirements		
Xilinx Core Tools	XACTstep 5.2.1/6.0.1	
Entry/Verification Tools	Verilog RTL	
Support		
Support provided by Inventra		

Notes:

1. CLB utilization for configuration with 3 endpoints, on-chip FIFOs and 32-Bytes per in/out endpoints
2. MAX I/O with on-chip FIFOs, assuming all core signals are routed off-chip; 51 IOBs if using external DMA.
3. For 10-15% of design, remaining logic operates at 1/4 max clock rate

- Includes the following error handling capabilities:
 - CRC errors

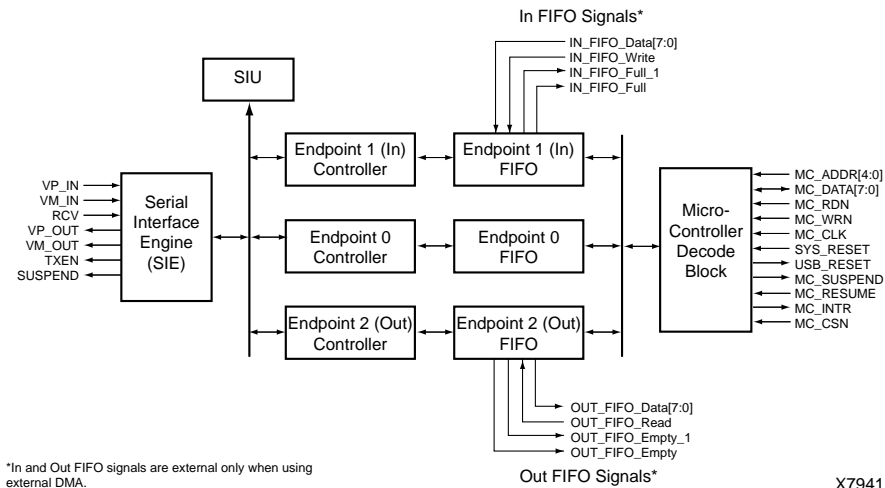


Figure 1: Full-Speed USB Function Controller Block Diagram

- Response Time Out
- ID errorNotes

Applications

- High-end computer peripheral equipment such as laser printers, plotters and high-speed telecommunications equipment.
- Embedded applications in telecommunication, industrial, medical or point-of-sale systems.

General Description

The Full-Speed USB Function Controller is flexible and can be used in a variety of applications. It includes all functionality for a complete function controller interface using one Xilinx FPGA plus an external Philips IPDIUSBP11 USB transceiver. The user can assign control of any endpoint to a microcontroller or external logic.

Functional Description

The USB Function Controller core is partitioned into modules as shown in and described below. Xilinx netlists are provided for each module.

Serial Interface Engine (SIE)

This block handles NRZI decoding/encoding, CRC generation and checking and bit-stuffing. It also provides the interface signals for an external Philips IPDIUSBP11 USB transceiver.

SIU

This block handles endpoint address decoding for USB packets.

Endpoint 0 Control

The Endpoint 0 Controller handles control transfers.

Endpoint 1 Control

The Endpoint 1 Controller is configured as an In Endpoint and handles TX data transfers between host and function. It can be configured to handle either Bulk, Isochronous or Interrupt/Status data transfers.

Endpoint 2 Control

The Endpoint 2 Controller is configured as an Out Endpoint. It can be configured to handle either Bulk, Isochronous or Interrupt/Status data transfers.

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
Transceiver Interface Signals		
VP_IN	Input	D+ input from XCVR
VM_IN	Input	D- input from XCVR
RCV	Input	Differential data from XCVR
VP_OUT	Output	D+ output for XCVR
VM_OUT	Output	D- output for XCVR
TXEN	Output	Enable for XCVR, active low
SUSPEND	Output	Suspend signal, puts XCVR into suspend mode
Microprocessor Interface Signals		
MC_ADDR [4:0]	Input	Microcontroller Address bus
MC_DATA [7:0]	In/Out	Microcontroller Data bus
MC_RDN	Input	Read Strobe, active low
MC_WRN	Input	Write Strobe, active low
MC_CLK	Input	48 MHz microcontroller clock input
SYS_RESET	Input	System Reset, active high
USB_RESET	Output	USB Reset, active low
MC_SUSPEND	Output	Interrupt signal generated during SUSPEND signal on USB, active high; provided as dedicated bit in Power Mgmt register
MC_RESUME	Output	Interrupt signal generated during RESUME signal on USB, active high
MC_INTR	Output	Microcontroller Interrupts, active low
MC_CSN	Input	Acts as a Block Select to microcontroller address, active low

FIFOs

The core has a bidirectional 16 Byte Endpoint 0 FIFO that handles standard and class specific descriptors. It interfaces to the microcontroller, which handles descriptor decoding and specified descriptor actions.

The In and Out FIFOs are 32-Bytes deep and uni-directional for TX and RX data transfers, respectively. The maximum packet size for In and Out tokens is register-selectable at 8/16/32-Bytes.

The In and Out FIFOs can be interfaced either to the microcontroller or to an external DMA channel. When using external DMA, the microcontroller writes to an internal register bit that disables microcontroller access to the registers and enables external access.

Signal	Signal Direction	Description
FIFO Interface Signals (used only when interfacing to external DMA)		
IN_FIFO_Data [7:0]	Input	TX data input to In FIFO
IN_FIFO_WRT	Input	In FIFO write strobe
IN_FIFO_FULL	Output	Indicates In FIFO is full
IN_FIFO_FULL_1	Output	Indicates In FIFO can accept only one more Byte
OUT_FIFO_Data [7:0]	Output	RX data received from the host
OUT_FIFO_RD	Output	Out FIFO read strobe
OUT_FIFO_EMPTY	Output	Indicates Out FIFO is empty
OUT_FIFO_EMPTY_1	Output	Indicates only one Byte is available in Out FIFO

Endpoint FIFOs are implemented using XC4000E Select RAM™. For applications that need larger FIFOs, the FIFO can be off-chip. Inventra will customize the core for users.

Microcontroller Decode Block

The microcontroller interface is generic, with Address and Data bus interfaces, and Read and Write control signals. It generates an interrupt to the microcontroller when data is ready, and when data has been successfully transmitted. The core performs hardware retries and data buffering. This improves performance by reducing the burden on the microcontroller. The microcontroller does address decoding for internal registers (i.e. FIFO Data Register).

This interface is asynchronous. All signals (MC_WRN, MC_RDN) are synchronized internally. MC_WRN and MC_RDN are active low.

This block is not required if the outputs of the FIFOs are connected directly to a DMA controller.

Table 2: Microcontroller I/O Timing

SIGNAL	Setup	Hold
MC_ADDR	3 ns	0 ns
MC_DATA	3 ns	0 ns
MC_WRN	3 ns	0 ns
MC_RDN	3 ns	0 ns

Core Modifications

The Full-Speed USB Function Controller Core is modular in design, making modifications relatively simple. If you are interested in obtaining a version of the core that differs from

this product description, then contact Inventra directly. Inventra can provide custom versions of the core, including support for the following:

- Changing Endpoint FIFO depths.
- Modification for audio- or video-specific applications.
- Support for low-speed functions is provided by the Low-Speed Function Controller Core, also available from Inventra. A similar product description for that function is available from both Inventra and Xilinx.

Pinout

The pinout of the Full-Speed USB Function Controller has not been fixed to specific FPGA I/O, allowing flexibility with a users application. Signal names are shown in the block diagram in Figure 1, and in Table 1.

Verification Methods

The Full-Speed USB Function Controller core has been tested with products from over 30 system manufacturers at USB-IF sponsored compliance workshops. The Xilinx-based implementation of the core passed all interoperability testing with numerous host, BIOS and peripheral products.

The core has undergone extensive testing using Inventra USB Simulation Model that includes a host controller, function controller and protocol analyzer. This model is available separately from Inventra.

Recommended Design Experience

Knowledge of the USB specification is required. The user must be familiar with HDL design methodology as well as instantiation of Xilinx netlists in a hierarchical design environment.

Available Support Products

Inventra supplies a complete line of hardware and software products designed to aid integration of this core into your application. These are available for additional cost. Contact Inventra for more information.

- USB Function Evaluation Board
- USB Simulation Model

Ordering Information

This product is available from the AllianceCORE™ partner listed on the first page. Please contact the partner for pricing and more information.

Related Information

Universal Serial Bus Implementor's Forum

The USB-IF publishes USB specifications and related documents:

- USB Specification, Rev. 1.0
- USB Compliance Checklist
- USB Device Class Definitions for Human, Audio, Video and Mass Storage devices

Contact:

USB Implementor's Forum

URL: www.usb.org

Philips Semiconductor

For additional information on the Philips *IPDIUSBP11* USB transceiver chip, contact:

Philips Semiconductors

URL: www.semiconductors.philips.com

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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URL: www.xilinx.com/products/logiccore/alliance/tblpart.htm