3-Port USB Hub Controller

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Inventra™

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Features

- Fully compliant to USB 1.0 specification
- 100% programmable single-chip solution
- Pre-defined implementation for predictable timing in Xilinx FPGA or HardWire™
  - Push button scripts to place and route, and generate Xilinx bit files
  - Xilinx-optimized place and route constraint and guide files
- Fully verified design
  - Simulated using Inventra USB system simulation model
  - Hardware-proven in a Xilinx FPGA at USB-IF sponsored interoperability workshop
- Compatible with both OpenHCI and Intel UHCI standards
- Pre-configured with 1 up-stream and 3 down-stream ports
- Expandable down-stream ports
- Fault detection for up-stream traffic
- Detects control and status change endpoints
- Supports Suspend and Resume signaling
- Handles all Hub Class device descriptors
- Capable of handling remote wake-up
- Supports down-steam power control
- Supports a mixture of full- and low-speed ports
- Provides an ideal compound-device solution when coupled with either low- or full-speed Function Controller cores, also available from Inventra
- Xilinx-based hub evaluation board is available from Inventra
- External interfaces to Philips *IPDIUSBP11* USB transceivers

AllianceCORE™ Facts

Core Specifics		
Device Family	XC4000E	
CLBs Used	960	
IOBs Used	53[1]	
System Clock f_{max}	48Mhz[2]	
Device Features Used	RAM, Carry Logic	
Supported Devices/Resources Remaining		
	I/O	**CLBs**
XC4025E-3 HQ240	140	64
Provided with Core		
Documentation	XC4000E Datasheets Core documentation Sample files for top level module in Verilog HDL	
Design File Formats	XNF Netlist Verilog Source RTL Available	
Constraint Files	Timespec, .cst, .tnm files	
Verification Tool	Verilog	
Schematic Symbols	Viewlogic, ORCAD	
Evaluation Model	Prototype board to implement Hub controller	
Reference designs & application notes	None	
Additional Items	Firmware for microcontroller available for nominal cost	
Design Tool Requirements		
Xilinx Core Tools	XACTstep 5.2.1/6.0.1	
Entry/Verification Tools	Verilog RTL	
Support		
Support provided by Inventra		

Notes:
1. Assuming all core signals are routed off-chip.
2. For 10-15% of design, remaining logic operates at 1/4 max clock rate.

Applications

- Compound Devices, with multiple functionality
- Telecommunication, PC peripheral, embedded applications

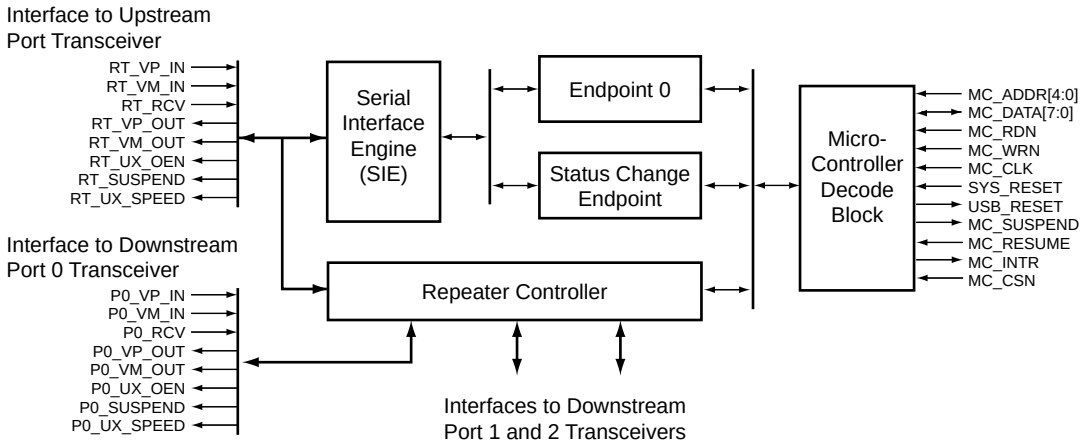

Figure 1: 3-Port USB Hub Controller Block Diagram

Functional Description

The USB Hub Controller core is partitioned into modules as shown in and described below.

Serial Interace Engine (SIE)

This block handles NRZI decoding/encoding, CRC generation and checking and bit-stuffing. It also provides the interface signals for an external Philips IPDIUSBP11 USB transceiver.

Endpoint 0

This block handles standard and hub class specific descriptors. The micro controller decodes the descriptors, and sets appropriate control bits in the repeater.

Status Change Endpoint

This block maintains the port connectivity of each down-stream port, and notifies the host controller if a device is connected or disconnected from any of the downstream ports.

Repeater Controller

This block controls traffic to and from the ports. The micro-controller sets the different states of the repeater as specified by the USB Specification. The repeater block handles:

- Detection of low-/full-speed devices connected.
- Low-speed signaling to & from down stream ports
- Suspend and Reset signaling from the root port to the down stream ports
- Resume signaling from the down stream functions to the Host.

Microcontroller Interface

This block interfaces to any standard 8 Bit micro controller. The microcontroller is used for descriptor decoding, and also adds compound device capabilities to the hub.

Core Modifications

Inventra will provide core modifications to add or remove downstream ports, or to provide a compound device.

Pinout

The pinout of the USB Hub Controller has not been fixed to specific FPGA I/O, allowing flexibility with a user's application. Signal names are provided in the block diagram shown in Table 1 and Figure 1.

Verification Methods

The USB Hub Controller core has been tested with products from over 30 system manufacturers at USB-IF sponsored compliance workshops. The Xilinx-based implementation of the core passed all interoperability testing with numerous host, BIOS and peripheral products.

The core has undergone extensive testing using Inventra's USB Simulation Model that includes a host controller, function controller and protocol analyzer. This model is available separately from Inventra.

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
Upstream Port Root Signals		
RT_VP_IN	Input	D+ input from the XCVR
RT_VM_IN	Input	D- input from the XCVR
RT_RCV	Input	Differential data from XCVR
RT_VP_OUT	Output	D+ output to the XCVR
RT_VM_OUT	Output	D- Output to the XCVR
RT_UX_OEN	Output	Enable for XCVR, active low
RT_SUSPEND	Output	Suspend signal, puts XCVR into suspend mode
RT_UX_SPEED	Output	Selects signaling speed on USB
Downstream Port Interface Signals		
P[0:2]_VP_IN	Input	D+ input from the XCVR
P[0:2]_VM_IN	Input	D- Input from the XCVR
P[0:2]_RCV	Input	Differential data from XCVR
P[0:2]_VP_OUT	Output	D+ output to the XCVR
P[0:2]_VM_OUT	Output	D- output to the XCVR
P[0:2]_UX_OEN	Output	XCVR Enable
P[0:2]_SUSPEND	Output	SUSPEND signal monitor
P[0:2]_UX_SPEED	Output	Selects signaling speed on USB
Microprocessor Interface Signals		
MC_ADDR [4:0]	Input	Microcontroller Address bus
MC_DATA [7:0]	In/Out	Microcontroller Data bus
MC_RDN	Input	Read Strobe, active low
MC_WRN	Input	Write Strobe, active low
MC_CLK	Input	48 MHz microcontroller clock input
SYS_RESET	Input	System Reset, active high
USB_RESET	Output	USB Reset, active low
MC_SUSPEND	Output	Interrupt signal generated during SUSPEND signal on USB, active high; provided as dedicated bit in Power Mgmt register
MC_RESUME	Output	Interrupt signal generated during RESUME signal on USB, active high
MC_INTR	Output	Microcontroller Interrupts, active low
MC_CSN	Input	Acts as a Block Select to microcontroller address, active low

Related Information

Universal Serial Bus Implementor's Forum

The USB-IF publishes USB specifications and related documents:

- USB Specification, Rev. 1.0
- USB Compliance Checklist
- USB Device Class Definitions for Human, Audio, Video and Mass Storage devices

Contact:

USB Implementor's Forum
URL: www.usb.org

Philips Semiconductor

For additional information on the Philips *IPDIUSBP11* USB transceiver chip, contact:

Philips Semiconductors
URL: www.semiconductors.philips.com

Recommended Design Experience

Knowledge of the USB specification is required. The user must be familiar with HDL design methodology as well as instantiation of Xilinx netlists in a hierarchical design environment.

Available Support Products

Inventra supplies a complete line of hardware and software products designed to aid integration of this core into your application. These are available for additional cost and are described below. Contact Inventra for more information.

- USB Simulation Model
- Hub Controller Evaluation Board

Ordering Information

This product is available from the AllianceCORE™ partner listed on the first page. Please contact the partner for pricing and more information.

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
URL: www.xilinx.com

For general Xilinx literature, contact:

Phone: +1 800-231-3386 (inside the US)
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For AllianceCORE™ specific information, contact:

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URL: www.xilinx.com/products/logicore/alliance/tblpart.htm