XF-TWSI Two-Wire Serial Interface

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Features

- Multi-master operation with arbitration and clock synchronization
- Support for reads, writes, burst reads, burst writes, and repeated start
- User-defined timing and clock frequency
- Fast mode and standard mode operation
- Compatible with popular protocols

Applications

- Embedded microprocessor boards
- Consumer and professional audio/video
- Home and automotive radio

General Description

The XF-TWSI is an industry standard two-wire serial interface supporting multiple masters.

AllianceCORE™ Facts

Core Specifics		
Device Family	XC4000E	XC5200
CLBs Used	137	64
IOBs Used	32[1]	32[1]
System Clock f_{max}	10+ MHz[2]	
Device Features Used	Tbufs, global clock buffers	

Supported Devices/Resources Remaining		
	I/O	**CLBs**
XC4005E-4[3] PC84C	29[1]	59
XC5202PC84-5[3]	33[1]	0

Provided with Core	
Documentation	Core schematics Implementation instructions
Design File Formats	ViewLogic schematic files Live hierarchical tree LCA Files
Schematic Symbols	ViewLogic
Verification Tool	Machine-readable simulation vectors for ViewLogic ViewSim
Constraint Files	None
Evaluation Model	None
Reference designs & application notes	None
Additional Items	Warranty by MDS

Design Tool Requirements	
Xilinx Core Tools	XACTstep 6.0.0
Entry/Verification Tools	ViewLogic PROcapture 6.1 or Workview Office

Support

Memec Design Services warrants that the design delivered by Memec Design Services will conform to the design specification. This warranty expires 3 months from the date of delivery of the design database. Contact Memec Design Services for the Design License Agreement with complete Terms and Conditions of Sale.

Notes:
1. Assuming all core signals are routed off-chip.
2. Minimum guaranteed speed.
3. Specific devices are minimum size and speed recommended - the core will work in any larger or faster devices from the same families.

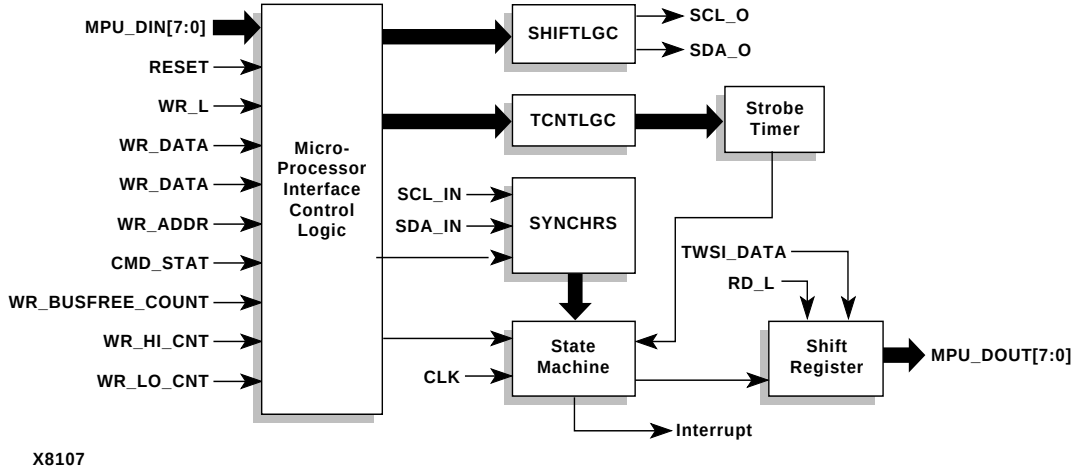

Figure 1: XF-TWSI Block Diagram

Functional Description

The XF-TWSI is partitioned into modules as shown in Figure 1 and described below.

Microprocessor Interface Control Logic

There are three registers used to interface to the host: the Data Register, the Address Register, and the Command Register. The strobes WR_DATA, WR_ADDR, and WR_CMD are directly connected to the clock pins of these register flip-flops for ease of interface.

There is a single parallel in, parallel out, serial in, serial out shift register called NUPSHIFT, which performs the shifting of data for address cycles, write cycles, and read cycles. The parallel output drives MPU_DOUT[7:0] which is used to return read data to the host**.**

Command Register: The Command Register consists of three bits: the READ bit (bit 0), the STOP bit (bit 1), and the REPEATED START bit (bit 2). These three bits control the operation performed on the serial interface.

The READ bit determines if the operation will be a read (high), or a write (low). The STOP bit will determine if the cycle will stop at the end of the data cycle, or continue on to a burst. The REPEATED START bit will cause the generation of a repeated start protocol.

To generate a single read cycle, the Address register is written with the desired address and the Command Register is written with B011 (binary 011, REPEATED START=0, STOP=1, READ=1) to perform the operation and stop. When the operation is completed (or aborted due to error) the Interrupt pin will go active and the data may be read on MPU_DOUT[7:0].

To generate a single write cycle, the Address Register is written first, followed by the Data Register, and the Command Register is written with B010 to perform the operation and stop.

A burst read operation is performed in the same manner as a single read, except that the Command Register is written with the STOP bit de-asserted (B001). At the end of the operation an interrupt is generated to the host and the SCL clock line is stretched. When the host has read the data it can write a B011 to the Command Register to perform one more read followed by a stop, or it can write a B001 to perform another read in anticipation of further bursting. Note that there is only one address cycle for a burst read cycle. Also, it is not permitted to follow a read operation or burst read operation with a write operation without first performing a repeated start or a stop.

A burst write operation is performed by setting up the Address and Data Registers, and writing the Command Register with B000. When an interrupt is detected, the next data item is written to the Data Register followed by either a B010 (last data written) or B000 (more data will follow).

The repeated start operation is used to directly follow a read with a write, or a write with a read, without a stop in-between. Some devices require this for the generation of a second address within the serial bus itself.

Any read or write operation may be followed by a repeated start by resetting the STOP bit and setting the REPEATED START bit when writing to the Command Register. For example, to perform a write cycle followed by a repeated start and a read, the Command Register is written with B100 to perform the write operation. An interrupt will be generated, as always, at the end of the write. Also at the

end of the write the clock line (SCL) will be stretched until the new command is written. If a single read is desired the Command Register is written with B011.

Timing: The primary clock, CLK, may be operated from 8 to 16 MHz by changing the timing dividers on BUSFREE_COUNT, HI_COUNT, and LO_COUNT core pins. These three bussed pins are used to define the timing for the part by attaching the appropriate divider values. These divider values are multiplexed into a counter which is used to time the low and high width of the SCL clock, the setup time and hold times, and the “bus free” time for arbitration purposes.

The BUSFREE_COUNT value is used to set the bus free time in terms of CLK periods. The XF-TWSI must see both the SDA and SCL pins in a high state for the bus free period before it issues a start or repeated start command on the bus. Note that this value must be set greater than the longest SCL high period in the system for arbitration to function properly. For Standard mode devices this should be set to at least 5 microseconds. For Fast mode devices this should be set to at least 1.5 microseconds.

The HI_COUNT value is used to define the low period of the SCL clock and the setup time for a repeated start command (rising edge of SCL to falling edge of SDA). This value is generally set to 4.7 microseconds for Standard mode and 1.3 microseconds for Fast mode.

The LO_COUNT value is used to define the high width of the SCL clock, the setup time for a stop command (rising edge of SCL to rising edge of SDA), as well as the start command hold time (falling edge of SDA to falling edge of SCL). This value is generally set to 4.0 microseconds for Standard mode and .6 microseconds for Fast mode.

The values can be added to busses attached to these pins as a series of VCCs and GNDs.Note that the actual values obtained from these dividers will be slightly larger due to state machine overhead.

SYNCHRS Block

The SDA and SCL inputs are passed through this module that performs a dual-rank synchronization and glitch filtering when enabled by the FILTER_EN signal. The synchronized versions of the SDA and SCL signals are used in all core modules.

The XF-TWSI core treats both the SDA and SCL lines as data lines. The SDA line is actually sampled some number of clocks after the rising edge of SCL is detected. This allows for greater noise immunity and more robust operation.

State Machine Block

The control for the serial interface comes from the TWSI_SM state machine. This state machine controls the loading and enabling of all shift registers and counters, and is responsible for implementing the basic interface protocol.

Arbitration: Before the XF-TWSI issues either a start or repeated start command it samples the synchronized versions of SDA and SCL for BUSFREE_COUNT x clock periods of high values. If at any time either of these pins is detected in a low (driven) state then the count starts over (it assumes that another master is on the bus). The automatic retrying to obtain the serial bus only occurs until the start command is issued. After that the responsibility of the retry is left to software, since cycles may be of infinite length.

After a start is issued and while the address or data is being written to the slave, the core samples the data on the SDA pin while SCL is high. If a data mismatch is detected then the operation is aborted with an interrupt and a BUSLOSS status. This can also occur during burst reads whenever a NACK is intended to be issued and an ACK is detected instead.

Performing Basic Cycles: The interface between the host and the XF-TWSI is interrupt-based. The host sets up the Address and Data Registers, writes the Command Register to initiate the desired operation, and performs other operations until the interrupt is generated by the core. Alternatively, if polled operation is desired, the Status Register may be read to see if the interrupt line is active.

Upon receiving the interrupt the host must read the Status Register to see if either of the two error conditions is present. Bit 2 in the Status Register is BUSLOSS, which occurs if the interface lost the bus to another master before completion of the cycle. Bit 1 in the Status Register is STATUS TIMEOUT, which occurs if the slave does not respond with an acknowledge when required. For either of these error conditions the host must retry the current cycle up until the last interrupt. Note that for burst operations the host is responsible for writing the incremented address into the Address Register before retrying the operation.

After the host receives the interrupt and determines the status, it sets up the registers again and writes the Command Register to start the next cycle. The act of writing the Command Register clears out the current interrupt.

Shift Logic (SHIFTLGC)

The basic cycle on theXF-TWSI serial interface consists of an address cycle followed by a data cycle. The address consists of seven bits and the read/write bit (the LSB). The MSB is always transmitted first on the SDA line. The data cycle can either be a read or a write. For a write operation the XF-IIC shifts the data from the Data Register onto the SDA line. For a read operation the core captures the data into the shift register. The data cycle can end in three different ways:

1. A stop can be generated which terminates the current cycle.
2. Another data cycle can take place (a burst).
3. A repeated start can be generated by the interface.

There is always one interrupt generated for each data cycle independent of the type of cycle. For example, for a burst read cycle an interrupt will be generated for each byte read. For a burst write cycle an interrupt will be generated when each byte transfer is completed.

A repeated start is used to turn the bus around; when a read cycle must be followed directly by a write cycle without a stop in-between. Since the READ bit is a part of the address, if a read followed by write is desired without a stop command, a second address must be issued following the data cycle. The sequence of events in a repeated start cycle is: start, address cycle, data cycle, repeated start, address cycle, data cycle, stop. Each of the data cycles can be repeated if bursting is desired, and the stop cycle could actually be another repeated start, if desired.

External Crystal Support

This core does not support connection of a crystal directly to the device. The XC4000 will require a clock input.

Table 1: Available Command Sequences

Operation	Subcycle	Command Register Contents		
		Repstart	Stop	Read
Single Read	Single Read	0	1	1
Single Write	Single Write	0	1	0
Burst Read	Burst Read Start	0	0	1
	Burst Read Continue	0	0	1
	Last Burst Read	0	1	1
Burst Write	Burst Write Start	0	0	0
	Burst Write Continue	0	0	0
	Last Burst Write	0	1	0
Read with Repeated Start followed by Burst Write	Read with RepStart	1	0	1
	Burst Write Start	0	0	0
	Burst Write Continue	0	0	0
	Last Burst Write	0	1	0
Write with Repeated Start followed by Burst Read	Write with RepStart	1	0	0
	Burst Read Start	0	0	1
	Burst Read Continue	0	0	1
	Last Burst Read	0	1	1
Illegal Sequence	Burst Read	0	0	1
	Burst Write	0	0	0
Illegal Sequence	Burst Write	0	0	0
	Burst Read	0	0	1

Pinout

The XF-TWSI may be implemented as stand-alone logic using the provided pinout or may be implemented internally with the users design. Both versions are included with the Core deliverables. Signal names are provided in the block diagram shown in Figure 1, and Table 2.

Table 2: Core Signal Pinout

Signal	Signal Direction	Description
CLK	Input	Primary clock used for all circuits.
RESET	Input	Reset, active high.
RD_L	Input	When active “0” with proper read buffer/register selected allows reads on the MPU_DOUT[7:0].
TWSI_DATA	Input	When active “1” with a RD_L allows reads on MPU_DOUT{7:0].
WR_L	Input	Rising edge of this signal registers data in internal registers when addressed.
MPU_DIN[7:0]	Input	Microprocessor Data In lines used to program Data, Address, and Command Registers.
WR_DATA	Input	When active “1” with a WR_L strobes 8-bits of data from MPU_DIN[7:0] into Data Register for serial bus write cycle.
WR_ADDR	Input	When active “1” with a WR_L strobes least significant 7 bits of data on MPU_DIN[7:0] lines into Address Register for all Serial Bus Operations
CMD_STAT	In/Out	When active “1” with a WR_L strobes least significant 3 bits of data from MPU_DIN[7:0] lines into Command Register and initiates serial bus cycle; also clears Interrupt line at this time. When active “1” with a RD_L reads Status Register.
WR_HI_CNT	Input	When active “1” with a WR_L strobes 8-bits of data from MPU_DIN[7:0] into HI_COUNT Register used to set number of CLK clock periods for low period of SCL and setup time for a repeated start operation.
WR_LO_CNT	Input	When active “1” with a WR_L strobes 8-bits of data from MPU_DIN[7:0] into LO_COUNT Register used to set number of CLK clock periods for high count of SCL, hold time for start command, and setup time for stop command.
WR_BUSFREE_COUNT	Input	When active “1” with WR_L strobes 8-bits of data from MPU_DIN[7:0] into BUSFREE_COUNT register used to set bus free period.
INTERRUPT	Output	Interrupt line set upon completion or abort of serial cycle. It is cleared by writing to Command, active high.
MPU_DOUT[7:0]	Output	Returns read data after activation of Interrupt pin and error free status.
SDA_IN	In	Serial Data In.
SDA_O	Out	Serial Data Out.
SCL_IN	In	Serial Clock In.
SCL_O	Out	Serial Clock Out.

Core Modifications

The XF-TWSI meets or exceeds the industry standard. However, in most cases the Timespecs can be tightened significantly. Successful operation with 120ns bus cycles has been achieved. In all cases, a post-route timing analysis should be performed to verify performance. Implementation beyond 10MHz and other customizing is available through Memec Design Services.

Verification Methods

Complete functional and timing simulation has been performed on the XF-TWSI using Viewsim. (Simulation vectors used for verification are provided with the core.) The README.TXT file has a short description of the top level CMD files used to simulate the design. These CMD files include descriptions and comments.

Recommended Design Experience

Users should be familiar with ViewLogic PROcapture or Office schematic entry and Xilinx design flows. Users should also have experience with microprocessor systems and peripherals.

Ordering Information

The XF-TWSI Two-wire Serial Interface Core is provided under license from Memec Design Services for use in Xilinx programmable logic devices and Xilinx HardWire™ gate arrays. To purchase or make further inquiries about this or other Memec Design Services products, contact MDS directly at the location listed on the front page.

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