LogiCORE™ Scaled By 1/2 Accumulator

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Features

- Drop-in modules for the XC4000E, EX, XL, XV and Spartan families
- Uses fast carry for high speed
- Data widths from 2 to 30 bits
- Clock-Enable for internal registers
- High performance and density guaranteed through Relational Placed Macro (RPM) mapping and placement technology
- Available in Xilinx CORE Generator

Functional Description

This macro accepts a N-bit signed input value, sign extends it to N+1 bits, and adds it to the Carry-In and the scaled feedback data. The feedback data is shifted right by one bit and sign extended two bits. (The LSB is discarded.) The shifting of the feedback is equivalent to dividing its value by 2. The Carry-In pin (CI) is treated as a 1-bit binary value.

The LOAD input, L, is used to bypass the adder and load the value on the B input directly into the accumulator's output register. The Truth Table for this function is shown in Table 1.

Since the output port S is 1-bit wider than the input port B, the MSB of S is assigned the MSB of B (i.e. S is sign extended) when a load operation is performed.

A typical application for this module is a bit-serial multiplier. Data is processed from LSB to MSB and each successive bit has twice the binary weight of its predecessor. The LSB of the output can be discarded for a single precision output, or registered in a serial-to-parallel register to maintain a double precision output.

Table 1: Truth Table

LOAD	CE	C	S
X	X	0	No Change
X	0	_/‾	No Change
0	1	_/‾	1/2S + B + CI
1	1	_/‾	B

Pinout

Port names for the schematic symbol are shown in Figure 1 and described in Table 2.

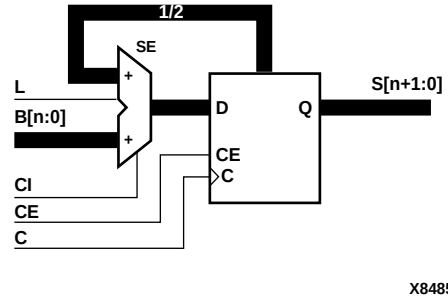

Figure 1: Core Schematic Symbol

Table 2: Core Signal Pinout

Signal	Signal Direction	Description
L	Input	LOAD – active high signal bypasses the adder and loads the value on B directly into the output register.
B[n:0]	Input	B data input – data is added to 1/2 the binary weight of the current contents of the register.
CI	Input	CARRY IN – treated as a 1-bit binary input and added to the sum of the B input and the feedback value.
CE	Input	CLOCK ENABLE - active high signal used to enable the transfer of data from the adder or the B input to the output register.
C	Input	CLOCK - with the exception of asynchronous control inputs (where applicable), control and data inputs are captured, and new output data forms on rising clock transitions.
S[n+1:0]	Output	SUM DATA OUTPUT – the registered output of the adder. Note: 1-bit wider than input operand B.

CORE Generator Parameters

The CORE Generator parameterization window for this macro is shown in Figure 2. The parameters are as follows:

- **Component Name**: Enter a name for the output files generated for this module.
- **Input Width**: Select an input bit width from the pull-down menu. The valid range is 2-30. The output size will be the input width plus one.

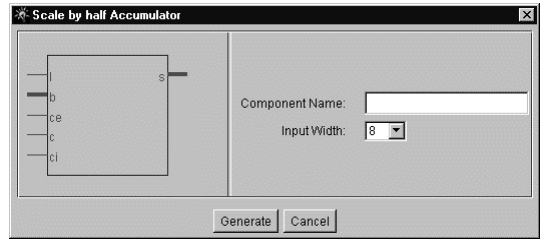

Figure 2: Parameterization Window

Core Resource Utilization

Table 2 shows the number of CLBs required for each available bit width.

Ordering Information

This macro comes free with the Xilinx CORE Generator. For additional information contact your local Xilinx sales representative, or e-mail requests to coregen@xilinx.com.

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Table 2: Bit Width versus CLB Count

Bit Width	CLB Count
2	2
3	2
4	3
5	3
6	4
7	4
8	5
9	5
10	6
11	6
12	7
13	7
14	8
15	8
16	9
17	9
18	10
19	10
20	11
21	11
22	12
23	12
24	13
25	13
26	14
27	14
28	15
29	15
30	16

Parameter File Information

Parameter Type	Type	Notes
Component_Name	String	
Input_Width	Integer	2 - 30