LogiCORE™ Registered Adder

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Features

- Two data bus inputs: 2 to 30 bits wide
- Supports both 2's complement signed and unsigned data
- Drop-in modules for the XC4000E, EX, XL, XV and Spartan families
- Registered output
- Clock Enable for output register
- Asynchronous Clear for output register
- Uses Fast Carry logic for high speed
- High performance and density guaranteed through Relational Placed Macro (RPM) mapping and placement technology
- Available in Xilinx CORE Generator

Functional Description

The Registered Adder module accepts two input buses, **A** and **B**, and a carry-input (**CI**) adds them, and registers the sum, **S**. The input data buses can be in either 2's complement signed or unsigned numbers.

The output bus is 1-bit wider than the input operands to accommodate any carry-out that may be generated when adding the MSBs.

Pinout

Port names for the schematic symbol are shown in Figure 1 and described in Table 1.

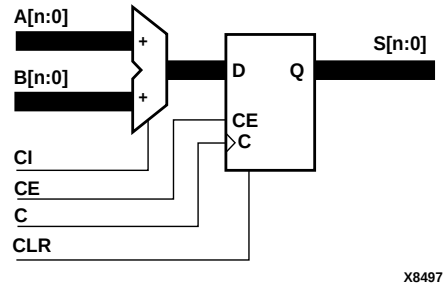

Figure 1: Core Schematic Symbol

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
A[n:0]	Input	A data input – value is added to B data and Carry Input (CI).
B[n:0]	Input	B data input – value is added to A data and Carry Input (CI).
CI	Input	CARRY IN – carry input. Treated as a 1-bit binary number and added to A and B.
CE	Input	CLOCK ENABLE – active high signal used to enable the transfer of data from the adder to the output register.
C	Input	CLOCK – with the exception of asynchronous control inputs (where applicable), control and data inputs are captured, and new output data formed on rising clock transitions.

Signal	Signal Direction	Description
S[n+1:0]	Output	SUM DATA OUTPUT – the registered output of the adder. Note: 1-bit wider than input operands, A and B.
CLR	Input	ASYNCHRONOUS CLEAR - resets the output register. Overrides Clock and Clock Enable. Level sensitive.

CORE Generator Parameters

The CORE Generator parameterization window for this macro is shown in Figure 2. The parameters are as follows:

- **Component Name**: Enter a name for the output files generated for this module.
- **Input Width**: Select an input bit width from the pull-down menu. The valid range is 2-30. The same data width is applied to both the A and B inputs. The output size is automatically set to the input width plus one.
- **Sign**ed: Select Signed or Unsigned.

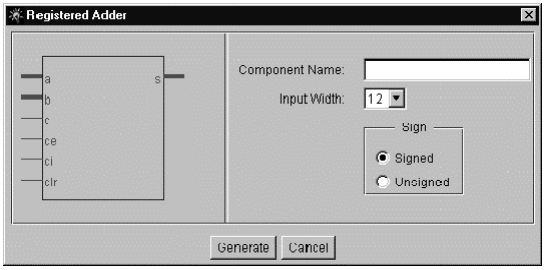

Figure 2: Parameterization Window

Core Resource Utilization

Table 2 shows the number of CLBs required for each available bit width.

Table 2: Bit Width versus CLB Count

Bit Width	CLB Count
2	2
3	2
4	3
5	3
6	4
7	4
8	5
9	5
10	6
11	6
12	7
13	7
14	8
15	8
16	9
17	9
18	10
19	10
20	11
21	11
22	12
23	12
24	13
25	13
26	14
27	14
28	15
29	15
30	16

Ordering Information

This macro comes free with the Xilinx CORE Generator. For additional information contact your local Xilinx sales representative, or e-mail requests to coregen@xilinx.com.

Parameter File Information

Parameter Name	Type	Notes
Component_Name	String	
Input_Width	Integer	2 - 30
Signed	Boolean	True/False