LogiCORE™

Registered Scaled Adder

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XILINX®

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Features

- Drop-in modules for the XC4000E, EX, XL, XV and Spartan families
- Two data bus inputs: 2 to 29 bits wide
- The size of the output data bus is adjustable from the input bus width plus two, up to 31 bits
- Supports 2's complement signed data
- Registered output
- Clock Enable for output register
- Uses Fast Carry logic for high speed
- High performance and density guaranteed through Relational Placed Macro (RPM) mapping and placement technology
- Available in Xilinx CORE Generator

Functional Description

The Registered Scaled Adder module accepts two input buses, **A** and **B**, and a carry input **CI**, adds them, and registers the sum, **S**. The input data buses are 2's complement signed numbers. While the **B** input is assumed to have a LSB bit weighting of 1, the **A** and **CI** bit weightings may be assigned arbitrarily. The **A** and **B** inputs must be the same bit-width, but to achieve the desired weighting of the **A** and **CI** inputs, the module sign extends the **B** input, and pads the LSB-end of the **A** Input with zeros. The difference between the input width and the output width determines how far **A** is shifted with respect to **B**, and therefore defines the bit-weighting of the **A** and **CI** inputs. The actual function performed by this module is:

$$(A + CI) \times 2^{P} + B$$

where

P = output_width - input_width - 1.

See Figure 1 next page.

A typical use for this module is in a multiplier adder tree. The result from a multiplier is often formed by adding together the partial products developed during the multiplication. Since each partial product has twice the weighting of its neighbor, an adder tree constructed of scaled adders would be appropriate.

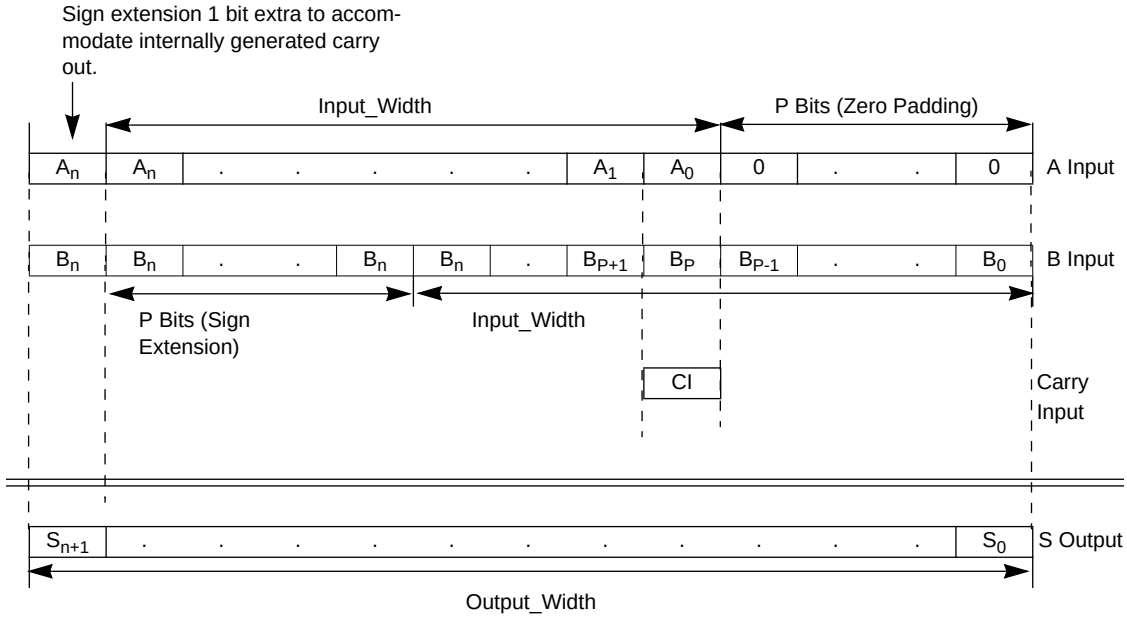

Figure 1: Illustration of Arithmetic Function Performed by Registered Scaled Adder Module

Pinout

Port names for the schematic symbol are shown in Figure 2 and described in Table 1.

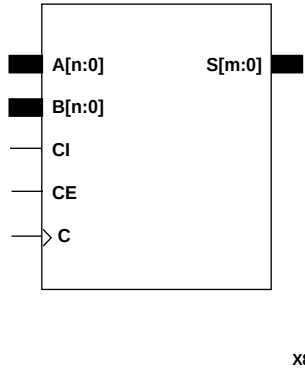

Figure 2: Registered Scaled Adder Schematic Symbol

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
A[n:0]	Input	A data input – LSB bit weighting of 2^P.
B[n:0]	Input	B data input – LSB bit weighting of 1.
CI	Input	CARRY IN – the Carry-In is scaled to the bit weighting of the A Data LSB, which equates to a left-shift of P bits with respect to the B data.
CE	Input	CLOCK ENABLE – active high signal used to enable the transfer of the result into the internal register.
C	Input	CLOCK – with the exception of asynchronous control inputs (where applicable), control and data inputs are captured, and new output data is formed on rising clock transitions.
S[m:0]	Output	SUM DATA OUTPUT – the registered output of the adder.

CORE Generator Parameters

The CORE Generator parameterization window for this macro is shown in Figure 3. The parameters are as follows:

- **Component Name**: Enter a name for the output files generated for this module.
- **Input Width**: Select an input bit width from the pull-down menu. The valid range is 2-29. The same data width is applied to both the A and B inputs.
- **Output Width**: Select an output bit width from the pull-down menu. The valid range is 4-31.

Core Resource Utilization

The number of CLBs required depends on both the Input and Output data widths. The equation is:

# of CLBs = floor((Input_width+2)/2) + 1 +
floor((Output_width-Input_width-2)/2)

Ordering Information

This macro comes free with the Xilinx CORE Generator. For additional information contact your local Xilinx sales representative, or e-mail requests to coregen@xilinx.com.

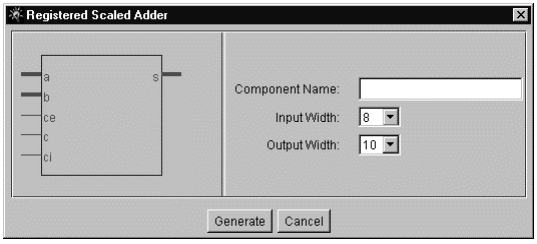

Figure 3: Parameterization Window

Parameter File Information

Parameter Name	Type	Notes
Component_Name	String	
Input_Width	Integer	2 - 29
Output_Width	Integer	4 - 31