LogiCORE™

Registered Serial Adder

XILINX®

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Features

- Drop-in modules for the XC4000E, EX, XL, XV and Spartan families
- Clock Enable for internal registers
- High performance and density guaranteed through Relational Placed Macro (RPM) mapping and placement technology
- Available in Xilinx CORE Generator

Functional Description

This macro accepts up to 32 1-bit serial data pairs and performs a bit-serial add on each pair. The incoming data is composed of bit-serial data, presented LSB first. When the CLEAR CARRY-IN (CLRCI) signal is not asserted, the input data A(n) is added to B(n) along with the Carry-Out that was stored from the previous addition. The resulting sum and Carry-Out are registered internally, and the sum presented to the output. When the CLRCI is asserted, the input data A(n) is added to B(n), with the Carry-Out from the previous addition set to zero. The resulting sum, and carry are registered, and the carry is used on the next cycle.

The data is added from LSB to MSB. The CLRCI signal must be asserted during the LSB add. See Figure 2, Timing Diagram.

Table 1: Truth Table

CLRCI	CE	A[n], B[n]	C	SD[n]
X	0	X	_/‾	No Change
0	1	A[n], B[n]	_/‾	A[n]+B[n]+CO[n]
1	1	A[n], B[n]	_/‾	A[n]+B[n]

Pinout

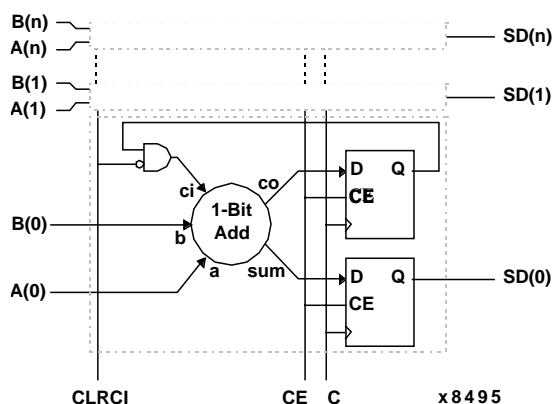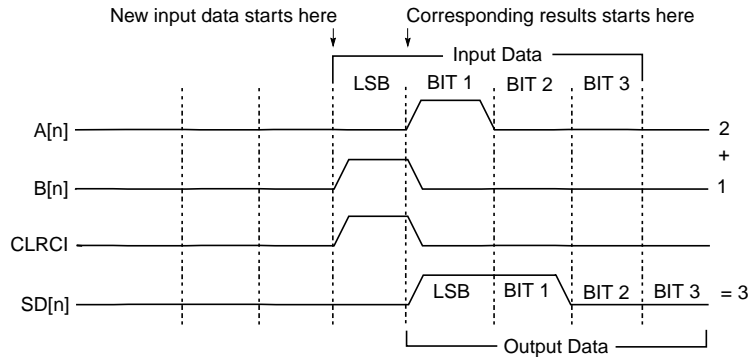Port names for the schematic symbol are shown in Figure 1 and described in Table 2.

Figure 1: Core Schematic Symbol

New input data starts here   Corresponding results starts here

Figure 2: Timing Diagram

Table 2: Core Signal Pinout

Signal	Signal Direction	Description
A[n:0]	Input	A DATA INPUT – N serial data inputs.
B[n:0]	Input	B DATA INPUT - N serial data inputs.
CLRCI	Input	CLEAR CARRY IN – Initializes the internal ripple carry logic to zero. This input should be asserted when LSB data is presented on the A and B inputs.
CE	Input	CLOCK ENABLE – active high signal used to enable the module's two internal registers.
C	Input	CLOCK - with the exception of asynchronous control inputs (where applicable), control and data inputs are captured, and new output data formed on rising clock transitions.
SD[n:0]	Output	SUM DATA REGISTERED OUTPUT – N serial data outputs SD[x] corresponds with addition of data presented on A[x] and B[x] inputs.

CORE Generator Parameters

The CORE Generator parameterization window for this macro is shown in Figure 2. The parameters are as follows:

- **Component Name**: Enter a name for the output files generated for this module.

- **Port Width**: Select a bit-width for the A, B and SD ports. Choosing a bit-width of, say n, implies the creation of n, 1-bit serial adders.
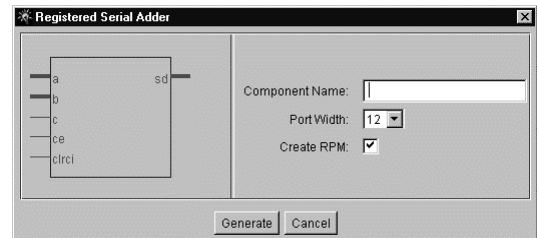- **Create RPM**: When checked, a columnar Relational Placed Macro is created.

Figure 2: Parameterization Window

Core Resource Utilization

The relationship between the Bit_Width and the number of CLBs required by the module is give thus: CLB Count = Bit-width number of CLBs required for each available bit width.

Ordering Information

This macro comes free with the Xilinx CORE Generator. For additional information contact your local Xilinx sales representative, or e-mail requests to coregen@xilinx.com.

Parameter File Information

Parameter Name	Type	Notes
Component_Name	String	
Port_Width	Integer	2 - 32
Create_RPM	Boolean	True/False