LogiCORE™ Integrator

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Features

- Multiply-free response computation
- Fractional 2's complement data format
- Input data widths from 2 to 30 bits
- Output data widths from 2 to 30 bits
- Single delay feedback
- Registered output
- Clock Enable for internal register
- Can be used as a general purpose parameterized accumulator for building a parallel MAC or an NCO
- Uses Fast Carry logic for high speed
- Drop-in modules for the XC4000E, EX, XL, XV and Spartan families
- High performance and density guaranteed through Relational Placed Macro (RPM) mapping and placement technology
- Available in Xilinx CORE Generator

Functional Description

The ideal integrator transfer function $H_I(z)=1/(1-z^{-1})$, has a pole at f=0. It is ideal in the sense that its response to an impulse is a step function, and its response to a step function (i.e., a dc input) is a linear ramp whose slope is proportional to step size. The Integrator is highly susceptible to overflow and adequate word growth of the accumulator register must be provided.

Integrators can be cascaded by simply connecting the output of one stage to the input of the next. Interstage scaling and truncation of data can alleviate overflow problems.

High order, multiplier-free decimation and interpolation filters can be implemented with cascaded stages of Ideal Integrators and Comb Filters [1].

With periodic clearing of the accumulator register, an “integrate and dump” accumulator is realized. This versatile device can serve as a low-pass or averaging filter per se, as the output stage of a polyphase filter, or, in conjunction with a single multiplier, as a minimal FIR filter [2].

1. E. B. Hogenauer, *“An Economical Class of Digital Filters for Decimation and Interpolation,”* IEEE Trans. on Acoustics, Speech, and Signal Processing, Vol. ASSP-29, April 1981, pp. 155-162.
2. D. F. Elliott, *“Handbook of Digital Signal Processing,”* 1987, Academic Press, pp. 245-252.

Pinout

Port names for the schematic symbol are shown in Figure 1 and described in Table 1.

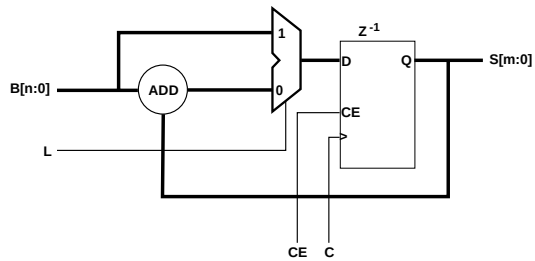

Figure 1: Block Diagram

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
B[n:0]	Input	SIGNED INPUT data.
C	Input	CLOCK - with the exception of asynchronous control inputs (where applicable), control and data inputs are captured, and new output data formed on rising clock transitions.
CE	Input	CLOCK ENABLE – active high signal used to enable the transfer of data from the adder or the B input to the output registers.
L	Input	LOAD – active high signal bypasses the adder and directly loads the B data into the output register.

Signal	Signal Direction	Description
S[m:0]	Output	INTEGRATOR output.

CORE Generator Parameters

The CORE Generator parameterization window for this macro is shown in Figure 2. The parameters are as follows:

- **Component Name**: Enter a name for the component.
- **Input Width**: Select an input bit width from the pull-down menu. The valid range is 2 to 30.
- **Output Width**: Select an output bit width from the pull-down menu. The valid range is 2 to 30.

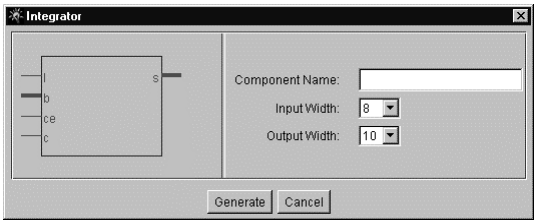

Figure 2: Parameterization Window

Core Resource Utilization

Table 2 shows the number of CLBs required for some available bit widths.

Table2: Bit Width versus CLB Count

Output Bit Width	CLB Count
4	3
8	5
12	7
16	9
20	11

Ordering Information

This macro comes free with the Xilinx CORE Generator. For additional information contact your local Xilinx sales representative, or e-mail requests to coregen@xilinx.com.

Parameter File Information

Parameter Name	Type	Notes
Component_Name	String	
Input_Width	Integer	2 - 30
Output_Width	Integer	3 - 30