LogiCORE™ Constant Coefficient Multiplier

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XILINX®

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Features

- Drop-in modules for the XC4000E, EX, XL, XV and Spartan families
- Fully combinatorial construction
- Multiplies a variable **A** times a constant **B**
- The **A** value can range from 4 to 32 bits
- The **B** value can range from 2 to 26 bits
- Independent **A** and **B** word size
- Independent selection of signed and unsigned for each operand
- Full precision output
- Supports 2's complement signed and unsigned number formats
- High performance and density guaranteed through Relational Placed Macro (RPM) mapping and placement technology
- Available in Xilinx CORE Generator

Functional Description

This parameterized module multiplies an N-bit wide variable times an M-bit fixed coefficient and produces an N+M bit result. The coefficient and multiplication tables are stored in distributed ROM-based look-up tables (LUTs), taking advantage of the FPGA look-up table architecture. It is an efficient, high speed, parallel implementation.

The variable and constant bit widths can be set independently, allowing the user to multiply different word widths together. The module automatically adjusts the signed and unsigned data to properly handle difference in bit widths.

The variable and constant can be independently selected to be 2's complement signed or unsigned magnitude-only values. Note that the module will automatically handle a signed times an unsigned number, two signed numbers, or two unsigned numbers.

The Constant Coefficient Multiplier (KCM) is used where the value of an incoming variable needs to be multiplied by a number that does not change, a constant. This is often the case in scaling functions, FIR filters, IIR filters, etc.

Pinout

Port names for the schematic symbol are shown in Figure 1 and described in Table 1.

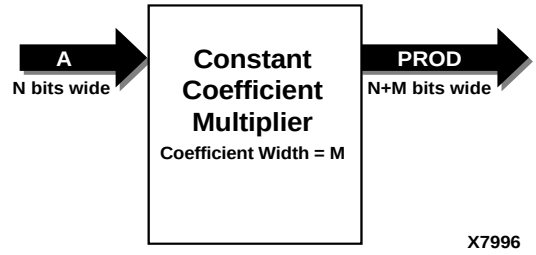

Figure 1: Block Diagram

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
A[n:0]	Input	PARALLEL DATA IN – an operand.
PROD[m+n:0]	Output	PARALLEL DATA OUT - product result.

CORE Generator Parameters

The CORE Generator parameterization window for this macro is shown in Figure 2. The parameters are as follows:

- **Component Name**: Enter a name for the component.
- **A_Width**: Select an input bit width from the pull-down menu for the variable width. The valid range is 4 to 32.
- **Signed Input Data**: Set the sign of the variable to Signed or Unsigned.
- **Coefficient Width**: Select an input bit width from the pull-down menu for the constant width. The valid range is 2 to 26.
- **Coefficient**: Enter the value of the desired constant.
- **Signed Coefficient**: Set the sign of the constant to Signed or Unsigned.

- **Radix**: Hexadecimal or Decimal representation of the constant.

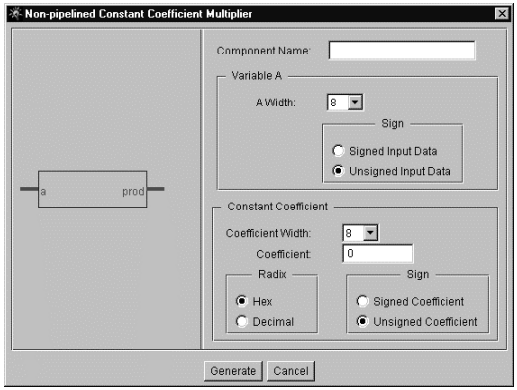

Figure 2: Parameterization Window

Core Resource Utilization

Table 2 shows the number of CLBs required for some available bit widths.

Table 2: Bit Width versus CLB Count

A Bit Width	B Bit Width	CLB Count
4	2	3
4	17	11
4	26	15
5	5	10
6	6	14
7	7	17
8	8	19
9	10	31
10	10	39
12	8	32
13	13	62
14	13	65
15	15	72
16	16	75
17	11	69
20	20	114
22	20	126
24	24	163
27	26	207
28	26	207
32	2	62
32	26	242

Ordering Information

This macro comes free with the Xilinx CORE Generator. For additional information contact your local Xilinx sales representative, or e-mail requests to coregen@xilinx.com.

Parameter File Information

Parameter Name	Type	Notes
Component_Name	String	
A_Width	Integer	4 - 32
Coefficient_Width	Integer	2 - 26
Signed_Input_Data	Boolean	True/False
Signed_Coefficient	Boolean	True/False
Coefficient	Integer	