# LogiCORE

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# **Features**

- · Pipelined construction for increased throughput
- Multiplies a variable A times a constant B
- The A value can range from 4 to 32 bits
- The B value can range from 2 to 26 bits
- Independent A and B word size
- Independent selection of signed and unsigned data format for each operand
- · Full precision output
- Supports 2's complement signed and unsigned magnitude numbers
- The inputs are not registered, but the outputs are registered
- Drop-in modules for the XC4000E, EX, XL, XV and Spartan families
- High performance and density guaranteed through Relational Placed Macro (RPM) mapping and placement technology
- Available in Xilinx CORE Generator

# **Functional Description**

This parameterized module multiplies an N-bit wide variable times an M-bit fixed coefficient and produces an N+M bit result. The coefficient multiplication tables are stored in distributed ROM-based look-up tables (LUTs), taking advantage of the FPGA look-up table architecture. It is an efficient, high speed, parallel implementation.

The variable and constant bit widths can be set independently, allowing the user to multiply different word widths together. The module automatically adjusts the signed and unsigned data to properly handle different sizes.

The variable and constant can be independently selected to be 2's complement signed or unsigned magnitude-only values. Note that the module will automatically handle a

## **Constant Coefficient Multiplier** (Pipelined)

**Product Specification** 

signed times an unsigned number, two signed numbers, or two unsigned numbers.

The Constant Coefficient Multiplier (KCM) is used where the value of an incoming variable needs to be multiplied by a number that does not change, a constant. This is often the case in scaling functions, FIR filters, IIR filters, etc.

#### **Pinout**

Port names for the schematic symbol are shown in Figure 1 and described in Table 1.

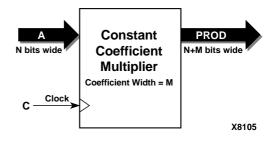


Figure 1: Block Diagram

#### **Table 1: Core Signal Pinout**

Signal	Signal Direction	Description
A[n:0]	Input	PARALLEL DATA IN – A op- erand.
С	Input	CLOCK – with the exception of asynchronous control in- puts (where applicable), con- trol and data inputs are captured, and new output data formed on rising clock transitions.
PROD[m+n:0]	Output	PARALLEL DATA OUT - product result.

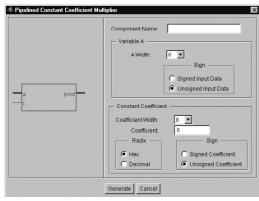
## **CORE Generator Parameters**

The CORE Generator parameterization window for this macro is shown in Figure 2. The parameters are as follows:

- Component Name: Enter a name for the component.
- A Width: Select an input bit width from the pull-down

menu for the variable width. The valid range is 4 to 32.

- **Signed Input Data**: Set the sign of the variable to Signed or Unsigned.
- **Coefficient Width**: Select an input bit width from the pull-down menu for the constant width. The valid range is 2 to 26.
- Coefficient: Enter the value of the desired constant.
- **Signed Coefficient**: Set the sign of the constant to Signed or Unsigned.
- Radix: Hexadecimal or Decimal representation of the constant.



**Figure 2: Parameterization Window** 

## **Multiplier Latency**

The total latency (number of clocks required to get the first output) is a function of the width of variable **A**. Table 2 shows the latency for the possible bit widths of **A**.

#### Table 2: Multiplier Latency

A Data Width	Latency (# Clocks)	
4 to 5 bits	1	
6 to 10 bits	2	
11 to 17 bits	3	
18 to 32 bits	4	

## **Core Resource Utilization**

Table 3 shows the number of CLBs required for some available bit widths.

#### Table 3: Bit Width versus CLB Count

A Bit Width	B Bit Width	CLB Count
4	2	3
4	17	11
4	26	15
5	5	10
6	6	16
7	7	19
8	8	21
9	10	34
10	10	42
12	8	44
13	13	68
14	13	73
15	15	80
16	16	83
17	11	77
20	20	154
22	20	169
24	24	197
27	26	244
28	26	244
32	2	86
32	26	266

## **Ordering Information**

This macro comes free with the Xilinx CORE Generator. For additional information contact your local Xilinx sales representative, or e-mail requests to coregen@xilinx.com.

#### **Parameter File Information**

Parameter Name	Туре	Notes
Component_Name	String	
A_Width	Integer	4 - 32
Coef_Width	Integer	2 - 26
Signed_Input_Data	Boolean	True/False
Signed_Coefficient	Boolean	True/False
Coefficient	Integer	