LogiCORE™ Parallel Multipliers – Area Optimized

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XILINX®

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Features

- Parallel Multipliers with parameterizable data widths
- Area optimized design
- Independently adjustable input variable widths from 6 to 32 bits
- Full precision outputs
- Two's complement signed and unsigned data formats
- Registered inputs and outputs
- Drop-in modules for the XC4000E, EX, XL, XV and Spartan families
- Pipelined design for increased throughput
- Clock Enable - freezes internal pipeline operation
- High performance and density guaranteed through Relational Placed Macro (RPM) mapping and placement technology
- Available in Xilinx CORE Generator

Functional Description

This parameterized module is a high-speed parallel implementation that multiplies an N-bit wide variable by an M-bit variable and produces an N+M bit result.

An area-efficient, high-speed algorithm is used to give an efficient, tightly packed design. Each stage is pipelined for maximum performance.

A clock-enable is available with which each internal pipelined stage may be halted. Partially completed results are not effected when CE is taken low, and the multiplier resumes normal operation when CE returns high.

Pinout

Port names for the schematic symbol are shown in Figure 1 and described in Table 1.

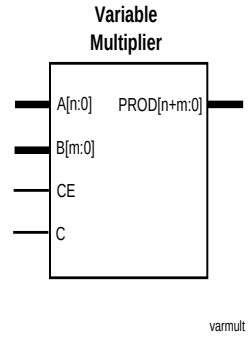

Figure 1: Core Schematic Symbol

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
A[n:0]	Input	PARALLEL DATA IN - A operand.
B[m:0]	Input	PARALLEL DATA IN - B operand.
C	Input	CLOCK - with the exception of asynchronous control inputs (where applicable), control and data inputs are captured, and new output data formed on rising clock transitions.
CE	Input	CLOCK ENABLE - when active high, allows data to propagate between internal pipeline stages. When inactive all activity within the module ceases.
PROD[m+n:0]	Output	PARALLEL DATA OUT - product.

CORE Generator Parameters

The CORE Generator parameterization window for this macro is shown in Figure 2. The parameters are as follows:

- **Component Name**: Enter a name for the component.
- **A Width**: Select an input bit width from the pull-down menu for the input A. The valid range is 6 to 32.
- **B Width:** Select an input bit width from the pull-down

menu for the input B. The valid range is 6 to 32.

- **Signed:** Representation for both input variables.

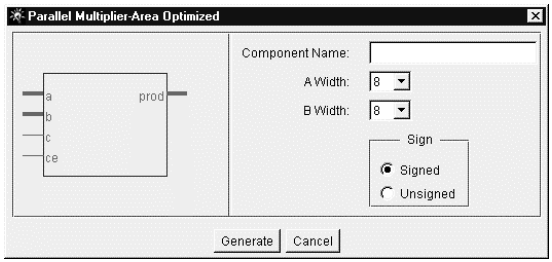

Figure 2: Parameterization Window

Module Layout

Figure 3 shows the organization of CLBs in a 12x12 multiplier. This module fits in an array of 144 CLBs organized as a matrix of 12 rows by 12 columns. The module uses 130 CLBs. The white squares represent the unused CLBs, demonstrating the efficiency with which the matrix is utilized. The unused CLBs are available for use in other parts of the system design.

Data enters the module from the left side (A) and the bottom left side (B). The resulting product is available on the right side (O). If any of the 24 outputs are not connected to the next stage of the design, the Xilinx implementation software eliminates all unused CLBs.

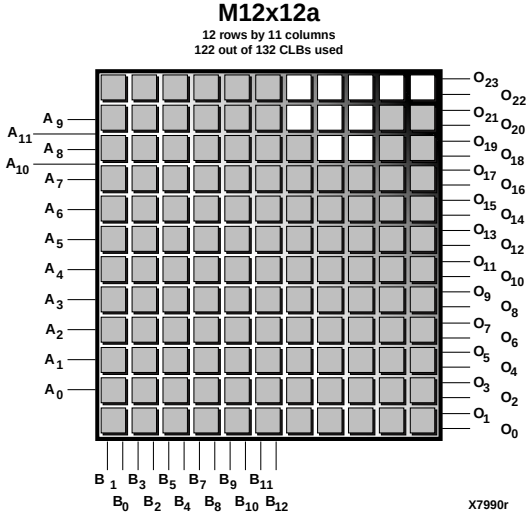

Figure 3: CLB Organization for Module

All of the area efficient series of modules can be built in a rectangular format. For example, an 8-bit by 12-bit multiplier will fit in a rectangular matrix of 8 rows by 12 columns.

Figure 4 shows a 12x12 multiplier in place in an XC4005E chip. The 4005E contains 196 CLBs, of which 130 are used by the 12x12 multiplier and 66 are available for other functions.

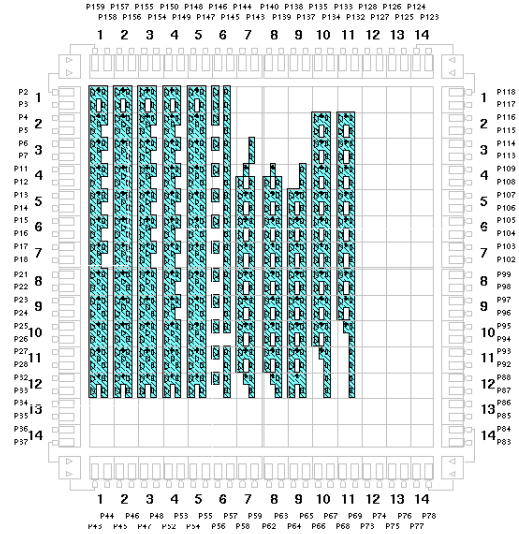

Figure 4: Xilinx Floorplanner View of XC4005E with a 12x12 multiplier

Core generator modules contain relative placement information that allow the Xilinx place and route software to consistently produce the same high performance. CLB relative placement information (R-LOCs) speeds up the routing place and route time by a significant factor, thus permitting rapid design changes.

Multiplier Latency

Data is buffered on the input and output of the multiplier cores. The total latency (number of clocks required to get the first output) is a function of the width of the **B** variable only.

Table 2: Multiplier Latency

B Data Width	Latency (# Clocks)
6 to 8 bits	4
9 to 16 bits	5
17 to 31 bits	6

Core Resource Utilization

Tables 3 to 8 show the number of CLBs required for some of the available bit widths. The maximum speed is for XC4000E-1 devices.

All the variable multipliers are built to fit in a rectangular or square matrix of N rows by M (or M-1) columns.

Table 3: Bit Width versus CLB Count for A = 8 bits

A Bit Width	B Bit Width	CLB Count	4000E-1 MHz	4000E-3 MHz
8	6	44	86	54
8	8	54	83	53
8	10	86	86	53
8	12	96	78	46
8	14	111	77	45
8	16	124	74	44
8	20	180	71	43
8	24	211	68	41
8	32	282	60	35

Table 4: Bit Width versus CLB Count for A = 10 bits

A Bit Width	B Bit Width	CLB Count	4000E-1 MHz	4000E-3 MHz
10	6	53	81	51
10	8	65	77	49
10	10	100	78	47
10	12	113	77	47
10	14	133	70	42
10	16	146	72	44
10	20	209	65	39
10	24	238	62	38
10	32	330	57	34

Table 5: Bit Width versus CLB Count for A = 12 bits

A Bit Width	B Bit Width	CLB Count	4000E-1 MHz	4000E-3 MHz
12	6	61	75	47
12	8	75	72	46
12	10	116	70	42
12	12	130	67	41
12	14	153	65	40
12	16	167	65	39
12	20	238	63	38
12	24	274	59	36
12	32	371	51	31

Table 6: Bit Width versus CLB Count for A = 16 bits

A Bit Width	B Bit Width	CLB Count	4000E-1 MHz	4000E-3 MHz
16	6	79	64	41
16	8	98	63	39
16	10	148	61	37
16	12	165	59	36
16	14	192	56	35
16	16	213	58	35
16	20	299	56	34
16	24	349	51	33
16	32	473	49	31

Table 7: Bit Width versus CLB Count for A = 20 and 24 bits

A Bit Width	B Bit Width	CLB Count	4000E-1 MHz	4000E-3 MHz
20	6	98	56	36
20	8	120	55	35
20	12	202	55	34
20	16	259	50	31
20	20	358	50	30
24	6	116	50	32
24	8	142	50	32
24	12	238	46	28
24	16	305	45	28
24	20	425	45	28

Table 8: Bit Width versus CLB Count for Other Widths of A

A Bit Width	B Bit Width	CLB Count	4000E-1 MHz	4000E-3 MHz
6	6	37	96	60
9	9	94	81	49
11	11	121	74	45
13	13	161	61	38
14	14	173	62	37
15	15	203	58	36
17	17	293	55	33
18	18	308	53	32
19	19	343	52	32
32	6	151	41	27
32	8	187	41	27
32	12	309	41	26

Multiplier Trade-offs

Two different implementations of parallel multipliers trade area for speed. The area efficient designs consume about one-fourth less CLB resources than the high speed designs in the 4000E family.

The additional routing resources in the 4000EX and 4000XL families will increase the performance for the area efficient designs. In addition, both structures will benefit from the overall performance increase derived from the 4000XL .35 micron process technology.

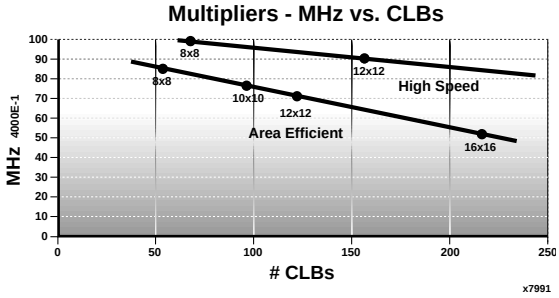

Figure 5: Trade-offs of Area Versus Speed Optimization for Multipliers

Ordering Information

This macro comes free with the Xilinx CORE Generator. For additional information contact your local Xilinx sales representative, or e-mail requests to coregen@xilinx.com.

Parameter File Information

Component Name	Type	Notes
Component_Name	String	
A_Width	Integer	6 - 32
B_Width	Integer	6 - 32
Signed	Boolean	True/False