LogiCORE™ Square Root

March 16, 1998 Product Specification

XILINX®

Xilinx Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
E-mail: coregen@xilinx.com
URL: www.xilinx.com

Features

- Input data widths from 4 to 64 bits
- Pipelined construction for increased throughput
- Performs one square-root function per clock cycle
- Output data widths from 4 to 64 bits
- Clock enable for entire pipeline
- User can determine the accuracy of the result by selecting the desired output width
- Drop-in modules for the XC4000E, EX, XL, XV and Spartan families
- High performance and density guaranteed through Relational Placed Macro (RPM) mapping and placement technology
- Available in Xilinx CORE Generator

Functional Description

The Square Root module derives the square root of the given input value.

The default output bit-width equals one-half the input bit-width. If higher accuracy is desired, choose a higher output width, up to the value of the input width. The decimal point in the result is always at the input_width/2 bit position.

Pinout

Port names for the schematic symbol are shown in Figure 1 and described in Table 1.

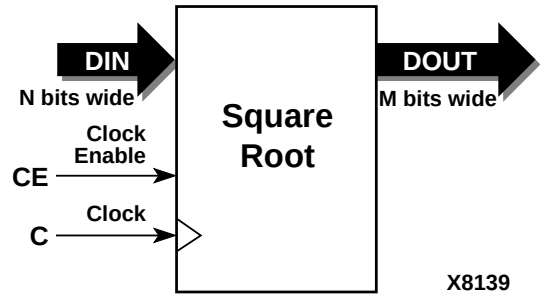

Figure 1: Block Diagram

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
DIN [n:0]	Input	INPUT DATA
C	Input	CLOCK with the exception of asynchronous control inputs (where applicable), control and data inputs are captured, and new output data formed on rising clock transitions.
CE	Input	CLOCK ENABLE – active high
DOUT [m:0]	Output	OUTPUT DATA

CORE Generator Parameters

The CORE Generator parameterization window for this macro is shown in Figure 2. The parameters are as follows:

- **Component Name**: Enter a name for the component.
- **Input Width**: Select an input bit width from the pull-down menu. The valid range is 4 to 64.
- **Output Width**: Select an output bit width from the pull-down menu. The valid range varies with the size of input data width.

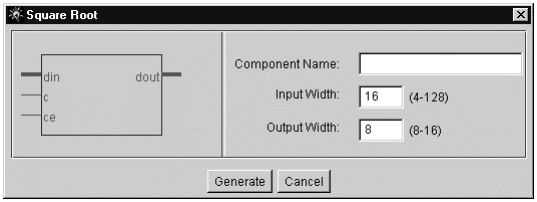

Figure 2: Parameterization Window

Latency

The latency equals the output width +1.

Core Resource Utilization

The number of CLBs required depends on the size of the input and output data widths selected in the CORE Generator parameterization window.

If output_width = input_width/2:

$$CLBs = (input\_width/2 + 1)^2$$

If output_width > input_width/2:

$$CLBs = (input\_width/2 + 1)(output\_width + 1) + (output\_width - input\_width/2) * (output\_width - input\_width/2 + 1)/2$$

Table 2 shows the number of CLBs required for some available bit widths.

Table 2: Bit Width versus CLB Count

Input Bit Width	Output Bit Width	CLB Count
4	4	18
8	4	25
12	12	112
16	8	81
32	16	289

Ordering Information

This macro comes free with the Xilinx CORE Generator. For additional information contact your local Xilinx sales representative, or e-mail requests to coregen@xilinx.com.

Parameter File Information

Parameter Name	Type	Notes
Component_Name	String	
Input_Width	Integer	4 - 64
Output_Width	Integer	4 - 64