LogiCORE™ Synchronous FIFO

March 16, 1998 Product Specification

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Features

- Supports data width from 4 to 80 bits
- Supports depths from 16 to 256 words
- Uses SelectRAM™ for high density and performance
- Registered output
- Drop-in modules for the XC4000E, EX, XL, XV and Spartan families
- High performance and density guaranteed through Relational Placed Macro (RPM) mapping and placement technology
- Available in Xilinx CORE Generator

Functional Description

The synchronous First-In, First-Out Memory module has a single clock port for both data-read and data-write operations. Data presented at the module's data-input port (D) is written into the next available empty memory location on a rising clock-edge when the write-enable input (WE) is High. The memory-full status output (FULL) indicates that no more empty locations remain in the module's internal memory, and that further data-writes must be avoided until the FULL output returns Low. Data can be read-out of the FIFO via the module's data-output port (Q) in the order in which it was written by asserting the read-enable input (RE) prior to a rising clock edge. The memory-empty status output (EMPTY) indicates that no more data resides in the module's internal memory, and that further data-reads should be avoided until the EMPTY output returns to LOW.

The internal read and write counters that maintain the FIFO status can be reset by asserting the RESET input prior to a rising clock edge. This effectively empties the FIFO, discarding any data that may have been stored in the module but which had not been read-out. Note that RESET has priority over RE and WE.

The FIFO provides two additional outputs - BUFCTR_CE and BUFCTR_UPDN - that may be used to control an external up/down counter such that the counter's output indicates the number of data words that are currently stored in the FIFO. See Figure 1. This may be useful in applications where more information about the FIFO's empty/full status is required - such as half-full, for example.

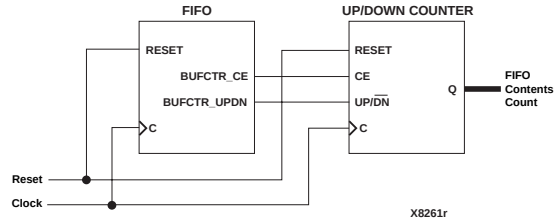

Figure 1: Connections for Up/Down Counter

The FIFO offers the designer the choice of implementing its internal memory with single- or dual-port SelectRAM™. Single-port memory is the most area efficient, but has the restriction that data may not be written and read at the same time. (I.e. WE = High and RE = High is illegal - and will be ignored - when single-port memory is used.) Dual-port memory permits simultaneous data-read and data-write operations, but incurs a higher area cost. See Figures 3 and 4.

The FIFO's internal state machine masks attempts to write data into a full FIFO (i.e. WE = High when FULL = High) and attempts to read data from an empty FIFO (i.e. RE = High when Empty = High). Either of these erroneous situations will be ignored by the FIFO, although no error flag is generated to indicate that the requested operation has not occurred.

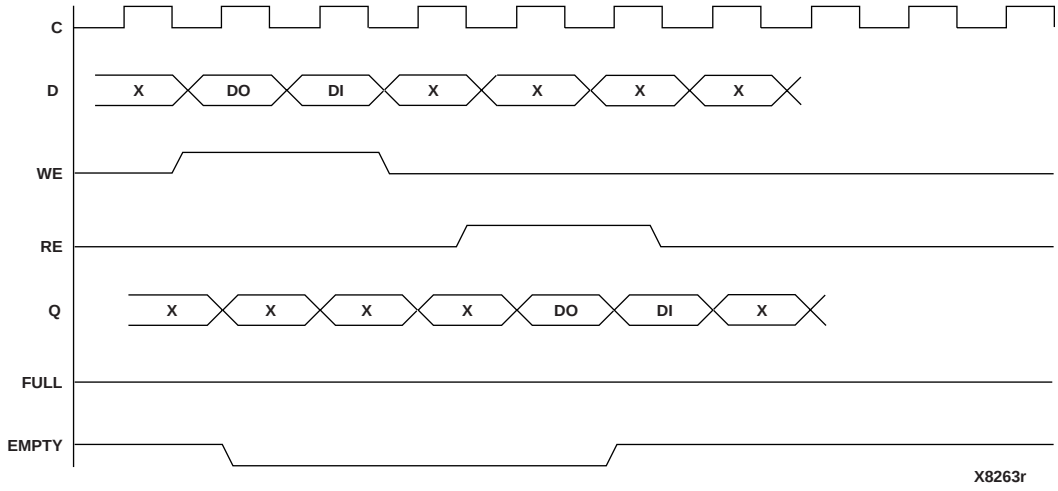

Figure 3: Timing Diagram for Single and Dual Ports

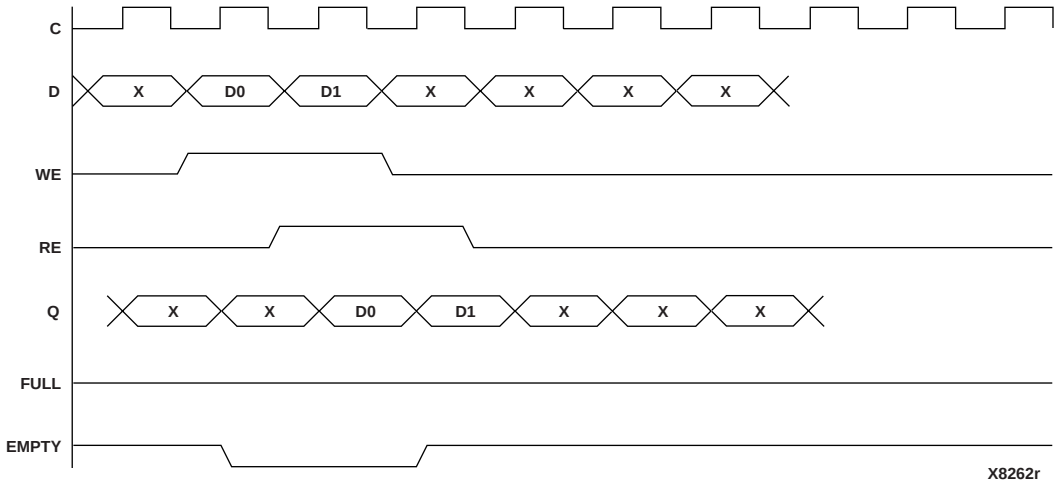

Figure 4: Timing Diagram for Dual Ports - Simultaneous Read and Write

Pinout

Port names for the schematic symbol are shown in Figure 2 and described in Table 1. Timing diagrams for the single and dual ports FIFO are shown in Figures 3 and 4.

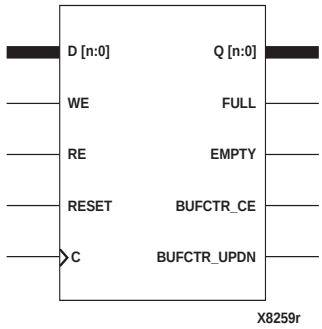

Figure 2: Core Schematic Symbol

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
D [n:0]	Input	DATA INPUT –port through which data is written into the FIFO.
WE	Input	WRITE ENABLE – active high signal used to allow the transfer of data from the input data port into the FIFO.
RE	Input	READ ENABLE – active high signal used to allow the transfer of data from the FIFO onto the output data pins.
RESET	Input	SYNCHRONOUS RESET – clears the FIFO
C	Input	CLOCK – with the exception of asynchronous control inputs (where applicable), control and data inputs are captured, and new output data formed on rising clock transitions.
Q [n:0]	Output	REGISTERED DATA OUT – the registered output of the FIFO.
FULL	Output	FULL – this signal is asserted when the FIFO is full.
EMPTY	Output	EMPTY – this signal is asserted when the FIFO is empty.
BUFCTR_CE	Output	Optional connect to the clock enable of an external up-down counter.
BUFCTR_UPDN	Output	Optional connect to the up-down pin of an external up-down counter.

CORE Generator Parameters

The CORE Generator dialog box for this macro is shown in Figure 5. The parameters are as follows:

- **Component Name**: Enter a name for the output files generated for this module.
- **Port Width**: Select an input bit width from the pull-down menu. The valid range is 4-80.
- **Depth**: Select the number of words in the FIFO from the pull-down menu. The valid range is 16-256 in multiples of 16.
- **Dual Port**: Select either Single Port or Dual Port RAMs.
- Internal Memory: You must choose Dual Port if simultaneous read/write operations are required.

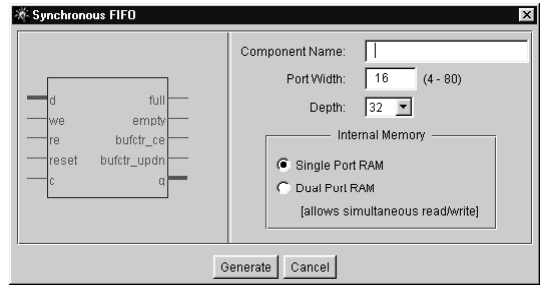

Figure 5: Parameterization Window

Core Resource Utilization

Table 2 shows the number of CLBs required for a sample of the available depths and bit widths.

Ordering Information

This macro comes free with the Xilinx CORE Generator. For additional information, contact your local Xilinx sales representative or e-mail requests to coregen@xilinx.com.

Table 2: CLB Utilization for Example FIFO Implementations

Depth	Ports[1]	CLB Counts for Example Data Word Widths						
		4-bit	8-bit	16-bit	32-bit	48-bit	64-bit	80-bit
16	Single	14	16	20	28	36	44	52
	Dual	14	18	26	42	58	74	90
32	Single	17	21	29	45	61	77	93
	Dual	22	34	58	106	154	202	250
48	Single	24	32	48	80	112	144	176
	Dual	28	44	76	140	204	268	332
64	Single	27	35	51	83	115	147	179
	Dual	32	48	80	144	208	272	336
96	Single	34	46	70	118	166	214	262
	Dual	42	66	114	210	306	402	498
128	Single	40	56	88	152	216	280	344
	Dual	52	84	148	276	404	532	660
256	Single	66	98	162	290	418	546	674
	Dual	94	158	286	542	798	1054	1310

Note 1: Describes construction of internal memory

Parameter File Information

Parameter	Type	Notes
Port_Width	Integer	4 - 80