LogiCORE™ Registered ROM

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XILINX®

Xilinx Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
E-mail: dsp@xilinx.com
URL: www.xilinx.com

Features

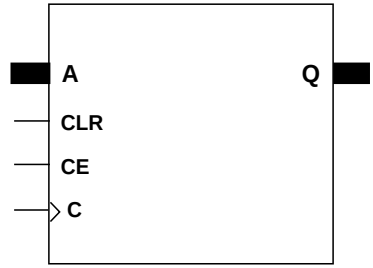
- Registered ROM with data width from 2 to 31 bits
- Registered output
- Clock Enable for output register
- Asynchronous clear of the output register
- Drop-in modules for the XC4000E, EX, and XL families
- High performance and density guaranteed through Relational Placed Macro (RPM) mapping and placement technology
- Available in Xilinx CORE Generator

Functional Description

This macro creates a ROM whose size is determined by the data width and depth variables in the dialog box. The output data is read from the ROM and registered. Data is read from the address selected on the A address pins. Access of the ROM is accomplished on the rising edge of the Clock signal with the CE pin asserted (HIGH). A CLR signal can be used to clear the register asynchronously.

Pinout

Signal names for the schematic symbol are shown in Figure 1 and described in Table 1.



X8166

Figure 1: Core Schematic Symbol

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
A	Input	ROM ADDRESS – the address of a particular ROM location.
CLR	Input	CLEAR – asynchronous clear of the register.
CE	Input	CLOCK ENABLE – active high signal used to allow the transfer of ROM data from the output data pins of the ROM into the output register.
C	Input	CLOCK – clocks the output register on the rising edge.
Q[N-1, 0]	Output	REGISTERED OUTPUT DATA – the registered output of the ROM.

CORE Generator Parameters

The core generator dialogue box for this macro is shown in Figure 2. The parameters are as follows:

- **Component Name**: Enter a name for the output files generated for this module.
- **Address Width**: The number of bits needed to address all of the words in the ROM.
- **Depth**: Select the number of words in the ROM from the pull-down menu. The number must be a multiple of 16.
- **Data Width**: Select an input bit width from the pull-down menu. The valid range is 2-31.
- **Load Init Values**: Specifies the file that contains the initial values for each address.
- **Show Init Values**: Display the initial values after they have been loaded.
- **coe file**: Displays the name of the coefficient file. This field is read-only.

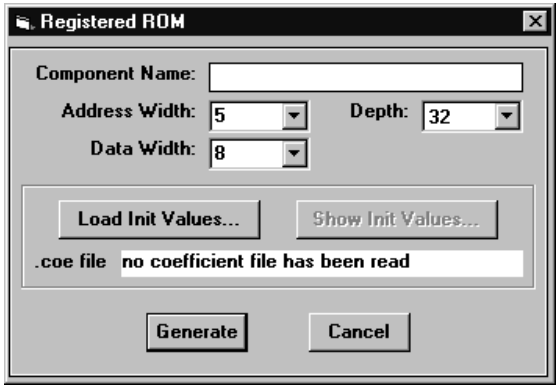


Figure 2: CORE Generator Dialog Box

Core Resource Utilization

The number of CLBs required depends on the values of the depth and data width fields selected in the CORE Generator dialog box.

Table 2 shows the equations to calculate the maximum number of CLBs required for selected depths and data widths.

Table 2: Bit Width versus CLB Count

Depth	Data Width	CLB Count
16	2N	N
16	2N+1	N
32	N	N
48	N	2N
>=64	2N	(Depth/16) (N+1)
>=64	2N+1	(Depth/16) (N+1)

Ordering Information

This macro comes free with the Xilinx CORE Generator. For additional information contact your local Xilinx sales representative, or e-mail requests to dsp@xilinx.com.