TX400 Series RISC CPU Cores

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T7L Technology, Inc.

220 Duncanmill Road
Suite 307
North York, Ontario
Canada, M3B 3J5
Phone: +1 416-445-4783
Fax: +1 416-445-5741
E-mail: t7linfo@t7l.com
URL: www.t7l.com

Features

- Scalable RISC CPU cores for embedded controller applications
- Compact RISC-oriented opcode design makes the core very small and requires less program size
- 26 different configurations, depending on application requirements
  - 8 - 32 bit data width
  - 8 - 32 bit data address width
  - 10 - 24 bit instruction length
  - 10 - 24 bit program address width
  - 1K - 16M bit maximum program size
- Function generator based logic structure and fully optimized for Xilinx FPGA physical architecture
- Up to 33Mhz operation
- Three stage, fully-balanced pipeline machine for prefetch/branch, instruction decode and execution
- Built-in hardware stack unit for instant program switching and low latency interrupt dispatching
- Debug version with snoop capability provided with each production core
- Ships with integrated development toolkit for CPU core embedding and run-time debugging
  - Support for high-level programming languages
  - Symbolic Assembler/Debugger
  - C Compiler

AllianceCORE™ Facts

Core Specifics	
Device Family	XC4000E, EX, XL
CLBs Used	See Table 1
IOBs Used	
System clock fmax	
Device Features Used	Select RAM
Supported Devices/Resources Remaining	
See Table 1	
Provided with Core	
Documentation	Design Manual H/W & S/W, Compiler, Assembly & C
Design File Formats	EDIF, .xnf, .ngo netlists
Constraint Files	N/A
Verification Tool	Development Software
Schematic Symbols	Foundation
Evaluation Model	Design base board
Reference designs & application notes	Music Panel sample design in VHDL and Schematics
Additional Items	PC Windows-based Debugger, assembly compiler and vector generator; Debug Version of core
Design Tool Requirements	
Xilinx Core Tools	Alliance/Foundation 1.3
Entry/Verification Tool	VHDL or Schematic
Support	
Support provided by T7L Technology, Inc.	

Applications

- Microcontroller Unit (MCU)
- Real-time Digital Signal Processor
- Dedicated Communication Processor
- Integrated Embedded System
- Programmable Peripheral Controller

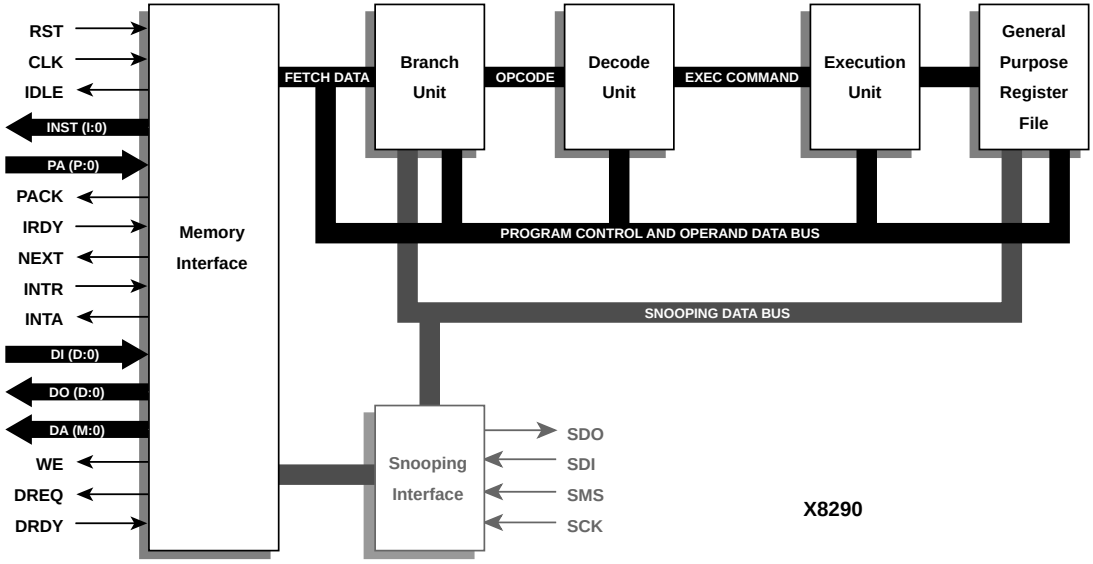

Figure 1: TX400 Block Diagram

General Description

The TX400 series RISC CPU core are a compact designs, optimized for Xilinx XC4000 FPGAs. T7L provides a full hardware development platform and software development tools that allow the user to integrate their unique logic with the core.

Functional Description

The TX400 core is based on a scalable 3-stage pipeline RISC CPU architecture. Separate instruction and data bus structures allow concurrent operations between program fetching and data transfer. A three-stage pipeline mechanism speeds up the system clock rate and simplifies the CPU state machine design.

The TX400 is partitioned into blocks as shown in Figure 1, and described below.

Memory Interface

This block interfaces with external system devices through the CPU bus. It transfers data to and from Data Memory Space, fetches instructions from Program Memory Space Convey and acknowledges external interrupt requests.

Snooping Interface

This block contains a serial data interface to an external snooping controller. It transfers data to and from CPU internal registers and modifies data memory contents.

Branch Unit

This performs program flow and interrupt control functions and generates next instruction prefetch address. It includes a built-in hardware stack for call and interrupt services.

Decode Unit

This decodes instructions and generates execution commands; compiles and exports source and target register addresses; provides data flow control command for execution.

Execution Unit

This executes data path commands and updates result to target operand; communicates with data bus for load/store operations.

General-purpose Register File

This is a dual-port register file for storing operand data. The register file supports simultaneous read and write operations.

Core Modifications

T7L offers 26 versions of the TX400 CPU core as fixed function Xilinx netlists. This broad selection should meet the vast majority of customer requirements. If you need a configuration that is not listed in Table 2, then contact T7L to discuss the possibility of supplying either a custom netlist or source code to meet your need.

Pinout

A simple handshake protocol is employed in the CPU bus interface. Signals can be selected as either active high or active low and are fully synchronous to either the rising or falling edge of the CPU clock input.

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
System Signals		
RST	Input	CPU Reset; force CPU into initial known state for bootstrapping when reset is released.
CLK	Input	CPU Clock; synchronizes all internal logic and function units.
IDLE	Output	CPU Idle; indicates CPU is waiting for new instruction.
Instruction Bus		
INST (I:0)	Input	Instruction Input; fetches instruction words from program memory space, qualified by IRDY during normal operation and by INTA for importing interrupt address during interrupt acknowledgment.
PA (P:0)	Output	Program Address; fetches instructions from program memory space, aligned with instruction word length ‘I’.
PACK	Output	Prefetch Acknowledge that instruction word has been latched.
IRDY	Input	Instruction Ready for fetching.
NEXT	Output	Next Program Location; used for continuous burst access in program memory space for instruction fetching with location next to previous cycle.
INTR	Input	Interrupt Request for any asynchronous event. signal is.
INTA	Output	Interrupt Acknowledge; informs external logic to present interrupt address on instruction input bus; ends acknowledgment cycle.
Data Bus		
DI (D:0)	Input	Data Input bus for load data from data memory space, qualified by DRDY.
DO (D:0)	Output	Data Output bus for store data; output data lines held until CPU receives DRDY from external memory controller. No endian rule required.
DA (M:0)	Output	Data Address bus for data memory operations, qualified by DREQ; address lines held until CPU receives DRDY from external memory controller. M = data memory size.
WE	Output	Write Enable control for current data bus transaction once exported.
DREQ	Output	Data Request; initiates bus cycle in Data Bus and waits for DRDY.
DRDY	Input	Data Ready; acknowledgment signal from external memory controller for both read and write operations.
Snooping Bus (On Debug Versions Only)		
SDO	Output	Snoop Data Out; serial data out signal during CPU snooping cycle, qualified by SCK.
SDI	Input	Snoop Data In; serial data input signal during CPU snooping cycle, qualified by SCK.
SMS	Input	Snoop Mode Select; controls snoop mode; 0 for command mode, 1 for snooping data transfer.
SCK	Input	Snoop Data Clock to perform serial data shift in and out from CPU core.

There are four groups of signals (All scalable variables arezero basis).

- System Signals - for overall CPU control and status information
- Instruction Bus - for fetching instruction words from Program Memory Space
- Data Bus - for load or store of data into Data Memory & IO Space as requested by program

Snooping Bus - signals for reading or modifying CPU internal registers and data memory contents. These signals are on the debug versions of the cores only.

The pinout is not fixed to any specific device I/O. Signal names are provided in the block diagram shown in Figure 1, and described in Table 1.

Verification Methods

Test vectors generated by the V-System V4.4J from Model Technology have been used to test every instruction, instruction combination and interrupt event for these cores. They have also been silicon proven in Xilinx XC4000 FPGAs using the T7L Design Base Board, which is available separately from T7L.

Selecting the Right Core

There are 26 pre-implemented versions of the TX400, divided into seven groups. The characteristics of each are shown in Table 2. Each version is purchased and shipped separately. Each core comes with Xilinx netlists for a debug version that includes snooping circuitry and I/O, and a production version without snoop capability. The implementation statistics shown in Table 3 are for the production version of each core.

- ***Group 1 TX401*** - Microcontroller type CPU cores for embedded applications, and requires a small instruction set. Sizes range from 8 to 10-bit data and 10 to 12-bit instruction length.
- ***Group 2 TX402*** - Standard RISC CPU cores for embedded controller applications. Its size ranges from 8 to 10-bit data and 12 to 16-bit instruction length.
- ***Group 3 TX403*** - Compact RISC CPU cores for embedded system applications and requires a small instruction set. Its size ranges from 12 to 16-bit data and 12 to 16-bit instruction length.
- ***Group 4 TX404*** - Mid-size RISC CPU cores for embedded system applications. Its size ranges from 12 to 16-bit data and 12 to 16-bit instruction length.
- ***Group 5 TX405*** - Mid-size RISC CPU cores for DSP system applications. Its size ranges from 12 to 16-bit data and 12 to 16-bit instruction length.
- ***Group 6 TX406*** - Powerful RISC CPU cores for embedded system applications. Its size ranges from 24 to 32-bit data and 16 to 24-bit instruction length.
- ***Group 7 TX407*** - Powerful RISC CPU cores for DSP system applications. Its size ranges from 24 to 32-bit data and 16 to 24-bit instruction length.

Recommended Design Experience

To integrate a TX-400 core in an embedded system with a Xilinx XC4000 FPGA requires a simple design flow. The core is supplied in the form of Xilinx .ngo, EDIF, .xnf netlists and schematic symbol. Users include the core by either capturing into the top-level schematic or declaring/instantiating as a component in the top-level VHDL model.

Users should be familiar with RISC processors, processor code development environments and embedded system design.

Available Support Products

T7L offers 26 versions of the TX400 RISC CPU core along with hardware tools for integrating them into Xilinx FPGAs. T7L also supplies a complete software development environment. Products include:

- SDP Design Base Board (with Xilinx XC4000 FPGA) - $295
- Windows95 based assembler, debugger, monitor and vector generator (provided with core)
- C-Compiler (provided with core)

Ordering Information

There are 26 different cores in the TX400 family. Specifications for each are detailed in Table 2. Each comes with Xilinx netlists for production and debug versions. VHDL source is available for additional cost. For more information on these or other T7L products, contact T7L Technology directly.

Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
URL: www.xilinx.com

For general Xilinx literature, contact:

Phone: +1 800-231-3386 (inside the US)
+1 408-879-5017 (outside the US)
E-mail: literature@xilinx.com

For AllianceCORE™ specific information, contact:

Phone: +1 408-879-5381
E-mail: alliancecore@xilinx.com
URL: www.xilinx.com/products/logicore/alliance/tblpart.htm

Table 2: TX400 Series RISC CPU Selector Guide

Core	Data Bits (D)	Data Address Bits (M)	Max Data Bytes	Instruction Length Bits (I)	Program Address Bits (P)	Max Program Bits	General Registers	Special Registers	Stack Unit Level	No. of Instruction
Group 1										
TX401A	8	8	256	10	10	1K	4	3	16	47 +
TX401B	8	8	256	12	12	4K	8	3	16	47 +
TX401C	10	10	1K	10	10	1K	4	3	16	47 +
TX401D	10	10	1K	12	12	4K	8	3	16	47 +
Group 2										
TX402E	8	10	1K	12	12	4K	4	3	16	80 +
TX402F	8	12	4K	16	16	64K	16	3	32	80 +
TX402G	10	12	4K	12	14	16K	4	3	32	80 +
TX402H	10	14	16K	16	16	64K	16	3	32	80 +
Group 3										
TX403I	12	12	4K	12	14	16K	8	3	16	47 +
TX403J	12	14	16K	16	16	64K	16	3	32	47 +
TX403K	16	14	16K	12	14	16K	8	3	32	47 +
TX403L	16	16	64K	16	18	1M	16	3	32	47 +
Group 4										
TX404M	12	12	4K	12	14	16K	4	3	32	80 +
TX404N	12	16	64K	16	16	64K	16	3	32	80 +
TX404O	16	16	64K	12	14	16K	4	3	32	80 +
TX404P	16	16	64K	16	18	1M	16	3	32	80 +
Group 5										
TX405Q	12	12	4K	12	14	16K	4	3	32	140 +
TX405R	12	14	16K	16	16	64K	16	3	32	140 +
TX405S	16	16	64K	12	14	16K	4	3	32	140 +
TX405T	16	16	64K	16	18	1M	16	3	32	140 +
Group 6										
TX406U	24	24	16M	16	18	1M	16	3	32	80 +
TX406V	32	32	4G	16	18	1M	16	3	32	80 +
TX406W	32	32	4G	24	24	16M	256	3	32	80 +
Group 7										
TX407X	24	24	16M	16	18	1M	16	3	32	140 +
TX407Y	32	32	4G	16	18	1M	16	3	32	140 +
TX407Z	32	32	4G	24	24	16M	256	3	32	140 +

Table 3: Example Xilinx Device Utilization Statistics

Device	Statistic	TX400 Series Core			
TX402		**E**	**F**	**G**	**H**
XC4000E	CLBs	150	200	200	250
	IOBs	61	71	69	77
TX403		**I**	**J**	**K**	**L**
XC4000E	CLBs	130	180	180	220
	IOBs	73	81	83	93
TX404		**M**	**N**	**O**	**P**
XC4000E	CLBs	200	230	260	300
	IOBs	73	83	85	93