RISC CPU Core Design Base Board

December 15, 1997 | Product Specification

T7L Technology, Inc.

220 Duncanmill Road
Suite 307
North York, Ontario
Canada, M3B 3J5
Phone: +1 416-445-4783
Fax: +1 416-445-5741
E-mail: t7linfo@t7l.com
URL: www.t7l.com

Features

- Xilinx FPGA-based development board for use with T7L RISC processor cores
  - Supplied with XC4010EPC84
  - Higher pin count packages accommodated through extra daughter card
  - Supports Xilinx X-Checker cable
- Use in conjunction with T7L Scalable Development Platform software
  - Develop and debug code for working FPGA version of processor
- Built in 2 Mbits FLASH ROM for programming firmware
- Built in 1 Mbits FLASH ROM for configuring Xilinx FPGA
- Sockets for up to 2 Mbits of data memory in asynchronous SRAM
- On-board 24-key input device with dedicated scan decode circuitry
- On-board standard parallel port interface for debugging

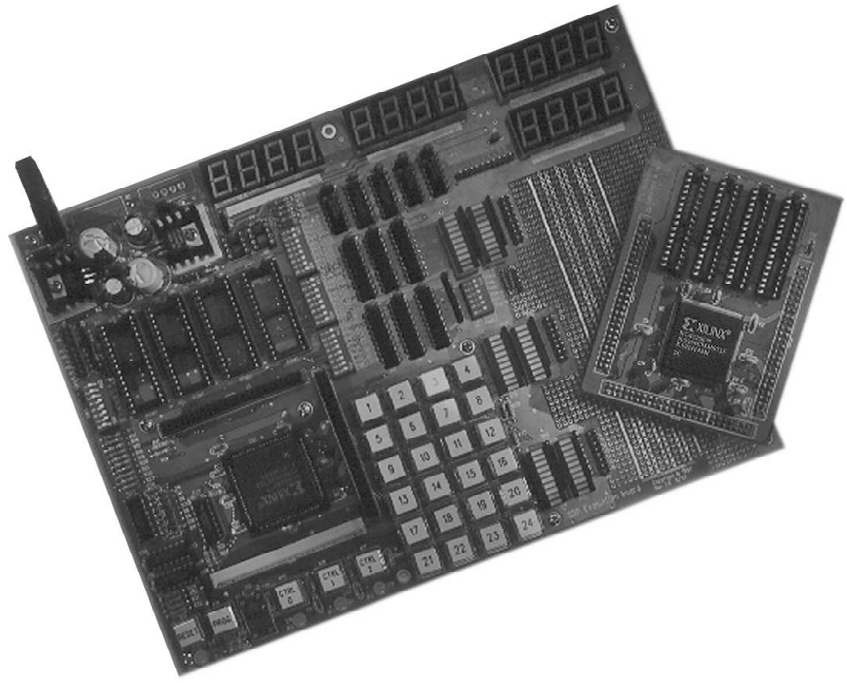

Figure 1: T7L RISC CPU Design Base Board

and downloading
- 48 user definable, general purpose I/O lines with 48 individual status LEDs
- 16 seven-segment LED display with dedicated decode circuitry

General Description

The T7L Scalable Development Platform (SDP) design base board is offered as part of the design kit for building prototypes of embedded systems using TX400 RISC CPU cores. It comes with a Xilinx XC4010EPC84 chip and some basic I/O devices.

The user is only required to glue together the CPU core, on board peripherals and application-specific I/O logic through either schematic capture or by creating a top-level VHDL model. With help of Xilinx place-and-route software, the system will then quickly be converted into physical configuration bitstream. Once the data file is downloaded into the on-board FPGA, the development board becomes a hardware prototype of the system running at speed for real-time software development, evaluation and debug.

Functional Description

The RISC CPU Core Design Base Board contains everything you need to develop and debug a RISC processor based FPGA design.

FPGA Chip

Basic on-board FPGA device is an XC4000E chip in a PLCC-84 package, upgradable to any XC4000E/EX/XL device in larger packages by means of a daughter board. Configuration data is downloaded from a PC system via standard parallel port.

Program Memory

There are two Flash ROMs for user's firmware program and initial data items. It supports 2 Mbits of program memory space. On-board programming utility for firmware codes is provided in the T7L SDP software tools.

Data Memory

There are two IC sockets for program data in asynchronous SRAM. It supports up to 1 Mbits of data memory space. Each IC socket is for any 32-pin DIP package static memory device, such 61 series fast SRAM devices.

Configuration Memory

There is one Flash ROM for user's Xilinx FPGA configuration. It supports 1 Mbits of FPGA configuration data, upgradable for 2 Mbits. On-board programming utility for FPGA configuration bit image is provided in the T7L SDP software tools.

Control Keys

There are seven input keys designed for control functions:

- *Reset*: User-defined reset input for FPGA and/or on board devices
- *Program*: To initialize the FPGA and wait for re-load of configuration data
- *Init*: To hold the FPGA and wait for re-load of configuration data via JTAG port.
- *User Control*: Four user-defined control input keys with external latching functions.

Keypad Matrix

A 24-key input device is provided on board. It is organized in a 3 x 8 matrix array. Scan decoding is supported externally by a TTL chip that saves a lot of I/O pins to the FPGA device.

LED Display

Total 16 seven-segment LED display units on board. They are time multiplexed and shared data lines. It is supported by an external TTL decoder in order to save I/O pins to and from an FPGA device.

User I/O Ports

There are 48 general-purpose I/O lines for user-defined logic functions, grouped into three 16-bit I/O ports. These can be connected to off-board peripheral device using cables. Each I/O line is supported by a status LED for real time logic debugging.

Download Port

An interface is provided to download configuration data and perform JTAG boundary scan testing. It supports the Xilinx X-Checker cable and software utility.

Parallel Port

An on-board 25-pin connector is built for CPU real-time hardware debugging, configuration data downloading and JTAG boundary scan testing. Hardware debug facilities for T7L CPU core is provided in the T7L SDP software tools.

Available Support Products

T7L also offers 26 versions of the TX400 RISC CPU core along with a development software. When used with the design base board, the customer has a complete development environment for integrating and testing T7L RISC cores in Xilinx FPGAs.

Ordering Information

The Design Base Board lists for $295 directly from T7L Technology. For more information on this or associated products, contact T7L directly.

Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
URL: www.xilinx.com

For general Xilinx literature, contact:

Phone: +1 800-231-3386 (inside the US)
+1 408-879-5017 (outside the US)
E-mail: literature@xilinx.com

For AllianceCORE™ specific information, contact:

Phone: +1 408-879-5381
E-mail: alliancecore@xilinx.com
URL: www.xilinx.com/products/logicore/alliance/tblpart.htm