C2910A Microprogram Controller

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Features

- Based on the AMD2910A device
- Pre-defined implementation for predictable timing
- Verified against a hardware model of the original device
- 12-bit data width that addresses up to 4,096 words
- Internal loop counter - pre-settable 12-bit down-counter for repeating instructions and counting loop interactions
- Four address sources
  - Microprogram counter
  - Branch address bus
  - 9-level push/pop stack
  - Internal holding register
- 16 powerful microinstructions
- Output Enable Controls for three branch address sources
- Positive-edge-triggered registers

Applications

The C2910A core is used in high speed bit slice designs.

General Description

The C2910A microprogram controller core is an address sequencer that controls the sequence of execution for the microinstructions stored in microprogram memory. The core can sequentially access the microinstructions, and it provides conditional branching to any microinstructions within the 4,096-microword range. In addition, a nine-deep LIFO stack provides a microsubroutine return linkage and looping capability.

AllianceCORE™ Facts

Core Specifics		
Device Family	Spartan	XC4005XL
CLBs Used	185	185
IOBs Used	38[1]	38[1]
System Clock f_{max}	27.7 MHz	34.5 MHz
Device Features Used	Global Buffers	

Supported Devices/Resources Remaining		
	I/O	**CLBs**
XC4005XL-09	75[1]	11
XCS10-3	75[1]	11

Provided with Core	
Documentation	Core Documentation
Design File Formats	XNF Netlist VHDL Source RTL
Constraint Files	NCF
Verification Tool	Test Bench Test Vectors
Schematic Symbols	Viewlogic
Evaluation Model	VHDL behavioral model
Reference designs & application notes	None
Additional Items	None

Design Tool Requirements	
Xilinx Core Tools	M1.3
Entry/Verification Tool	1076 compliant VHDL Simulator

Support
Support provided by CAST, Inc.

Notes:
1. Assuming all core signals are routed off-chip.

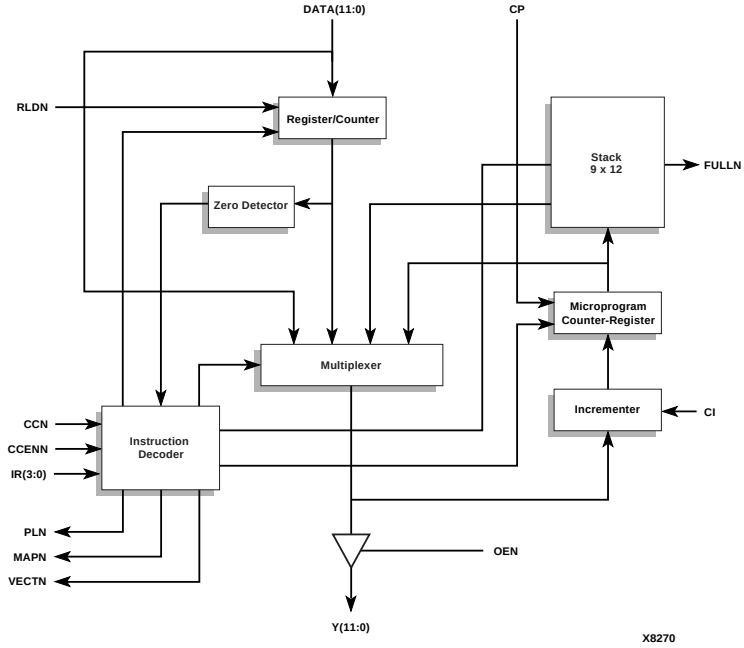

Figure 1: C2910A Microprogram Controller Block Diagram

Functional Description

The C2910A core is partitioned into modules as shown in Figure 1 and described below. Xilinx netlists are provided for each module.

Multiplexer

The four-input multiplexer is used to select either the register/counter, direct input, microprogram counter, or stack as the source of the next microinstruction address.

Register Counter

This block consists of 12 D-type, edge-triggered flip-flops, with a common enable. When its load control, RLDN is low, new data is loaded on a positive clock transition. The output of the register/counter is available to the multiplexer as a source for the next microinstruction address. The direct input furnishes a source of data for loading the register/counter.

Microcontroller Counter/Register (µPC)

This block consists of a 12-bit incrementer followed by a 12-bit register. The mPC can be used in either of two ways: When the carry-in to the incrementer is high, the microprogram register is loaded on the next clock cycle with the current Y output word plus one (Y + 1 → µPC). Sequential microinstructions are thus executed . When the carry-in is low, the incrementer passes the Y output word unmodified so that mPC is reloaded with the same Y word on the next clock cycle (Y → µPC). The same microinstruction is thus executed any number of times.

Stack

This 9-word by 12-bit stack is used to provide return address linkage when executing microsubroutines or loops. The stack contains a built-in stack pointer which always points to the last word written. This allows stack reference operations (looping) to be performed without a pop.

Instruction Decoder

This block decodes the incoming instruction and generates the appropriates control signals for all the other blocks. The instruction decoder block also generates the outputs PLN, MAPN, and VECTN.

Core Modifications

The C2910A core can easily be customized to include:

- Larger data width
- Different stack depth

Please contact CAST directly for any required modifications.

Pinout

The pinout of the C2910A core has not been fixed to specific FPGA I/O, allowing flexibility with a users application. Signal names are shown in the block diagram in Figure 1, and in Table 1.

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
CP	Input	Clock
IR (3:0)	Input	Instruction
DATA (11:0)	Input	Direct Data
CCN	Input	Condition Code
CCENN	Input	Condition Code Enable
RLDN	Input	Register Load Enable
CI	Input	Carry-In
OEN	Input	Output Enable
Y (11:0)	Output	Microprogram Address
FULLN	Output	Full Flag
PLN	Output	Pipeline Address Enable
MAPN	Output	Map Address Enable
VECTN	Output	Vector Address Enable

Core Assumptions

Stack PUSH

After a depth of 9 is reached, the stack is full and the FULLN output goes LOW. If further PUSHes are attempted when the stack is full, the stack information at the top of the stack (9) will be over-written.

It has been observed that the AM2910A device inconsistently destroys the top 2 locations of the stack (8 and 9). This functionality is apparently not documented, and should not be relied upon.

Stack POP

Further POPs from an empty stack will place the bottom data on the Y-Bus (no changes). Is has been observed that the AM2910A device will place random data in the Y-Bus during POPs from an empty stack.

To achieve proper result, do not exercise the stack beyond its range (i.e. no PUSHes while the stack is full and no POPs while stack is empty).

Verification Methods

The C2910A Microprogram Controller core's functionality was verified by means of a proprietary hardware modeler. The same stimulus was applied to a hardware model which contained the original AM2910A chip, and the results compared with the core's simulation outputs.The C2910A core has also been successfully implemented into silicon.

Recommended Design Experience

The user must be familiar with HDL design methodology as well as instantiation of Xilinx netlists in a hierarchical design environment.

Ordering Information

This product is available from CAST, Inc. Please contact CAST for pricing and more information.

Related Information

Bipolar Microprocessor Logic and Interface Data Book

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