M8254 Programmable Timer

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Virtual IP Group, Inc.

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Features

- Multiple, programmable, multi-mode timers
- Real-time clock
- Event counter
- Digital one-shot
- Programmable rate generator
- Square wave generator

Applications

- Binary rate multiplier
- Complex waveform generator
- Complex motor controller
- Baud rate generator

General Description

The M8254 is a programmable interval timer/counter core designed for use with standard micro-processor systems. It has three 16 bit counters, each of which is programmable to generate an interrupt at the end of a user-defined interval.

AllianceCORE™ Facts

Core Specifics		
Device Family	Spartan	XC4000E
CLBs Used	260	260
IOBs Used	22[1]	22[1]
System Clock f_{max}	12.4 MHz	12.4 MHz
Device Features Used	Global Buffers	
Supported Devices/Resources Remaining		
	I/O	**CLBs**
XCS40PQ240-3	171[1]	524
XC4020EHQ240-2	171[1]	524
Provided with Core		
Documentation	Core Design Document Designer's Application Note	
Design File Formats	.ngd, XNF netlist Verilog Source RTL available extra	
Constraint Files	.cst file, xactinit.dat	
Verification Tool	Test Vectors	
Schematic Symbols	None	
Evaluation Model	None	
Reference designs & application notes	FPGA Design Document included	
Additional Items	None	
Design Tool Requirements		
Xilinx Core Tools	Alliance 1.3	
Entry/Verification Tool	Verilog RTL/Verilog XL simulator	
Support		
Support provided by Virtual IP Group Inc.		

Notes:
1. Assuming all core signals are routed off-chip.

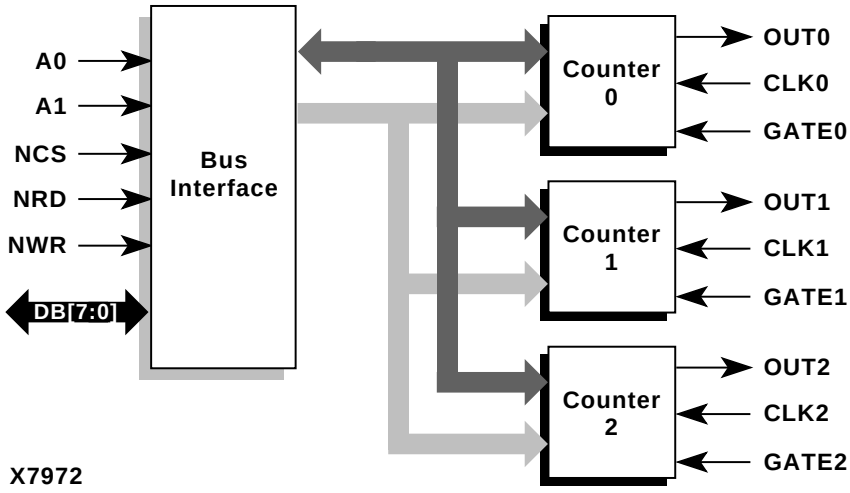

Figure 1: M8254 Block Diagram

Functional Description

The M8254 Core is partitioned into modules as shown in Figure1 and described below.

Bus Interface Block

This block contains decoders to generate counter select and the counter control select signals.

Counter 0-2 Blocks

These independently programmable counter blocks generate output based on the mode selected.

Core Modifications

Virtual IP Group, Inc. can modify this core to vary the number of timers.

Pinout

The pinout has not been fixed to specific FPGA I/O allowing flexibility with the user application. A pinout is suggested for use with a user-constructible evaluation board. Information for this is in the FPGA Design Document included with the core. Signal names are provided in the block diagram shown in Figure 1 and described in Table 1.

Verification Methods

The core has been tested with in-house developed test vectors that are provided with the core.

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
Bus Interface Signals		
A0, A1	Input	Address Signals
NCS	Input	Chip select, active low
NRD	Input	Read signal, active low
NWR	Input	Write signal, active low
DB[7:0]	Output	8-bit bidirectional CPU data bus
Counter Signals		
OUT0	Output	Output of counter 0
CLK0	Input	Clock input for counter 0
GATE0	Input	Gate input for counter 0
OUT1	Output	Output of counter 1
CLK1	Input	Clock input for counter 1
GATE1	Input	Gate input for counter 1
OUT2	Output	Output of counter 2
CLK2	Input	Clock input for counter 2
GATE2	Input	Gate input for counter 2

Recommended Design Experience

Knowledge of microprocessor based systems is required. The user must be familiar with HDL design methodology, instantiation of Xilinx netlists in a hierarchical design environment and usage of Xilinx Alliance or Foundation development tools.

Available Support Products

FPGA Evaluation Board

The FPGA Design Document included with the core gives directions for constructing a general purpose FPGA evaluation daughter board that can be plugged into a standard part socket on the target system through a flat cable.

Ordering Information

This product is available from Virtual IP Group, Inc. Please contact them for pricing and additional information.

Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
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For general Xilinx literature, contact:

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