M8255 Programmable Peripheral Interface

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Features

- Multi-mode programmable parallel I/O port peripheral interface
- 24 programmable general purpose I/O signals
- Functionally compatible with Intel 8255A
- Control word read-back facility
- Direct bit set/reset capability
- I/O data transfer with handshaking

Applications

- General purpose I/O ports used to control external peripherals

General Description

The M8255 Programmable Peripheral Interface (PPI) core is a general purpose I/O component to interface peripheral equipment to a microcomputer system bus. The functional configuration of the M8255 is programmable. This core is functionally compatible with the INTEL 8255.

AllianceCORE™ Facts

Core Specifics		
Device Family	Spartan	XC4000E
CLBs Used	111	111
IOBs Used	38[1]	38[1]
System Clock f_{max}	15.2 MHz	15.2 MHz
Device Features Used	Global Buffers	
Supported Devices/Resources Remaining		
	I/O	**CLBs**
XCS40PQ240-3	155[1]	673
XC4020EHQ240-2	155[1]	673
Provided with Core		
Documentation	Core Design Document Designer's Application Note	
Design File Formats	.ngd, XNF netlist Verilog Source RTL available extra	
Constraint Files	.cst file, xactinit.dat	
Verification Tool	Test Vectors	
Schematic Symbols	None	
Evaluation Model	None	
Reference designs & application notes	FPGA Design Document included	
Additional Items	None	
Design Tool Requirements		
Xilinx Core Tools	Alliance 1.3	
Entry/Verification Tool	Verilog RTL/Verilog XL simulator	
Support		
Support provided by Virtual IP Group, Inc.		

Notes:
1. Assuming all core signals are routed off-chip.

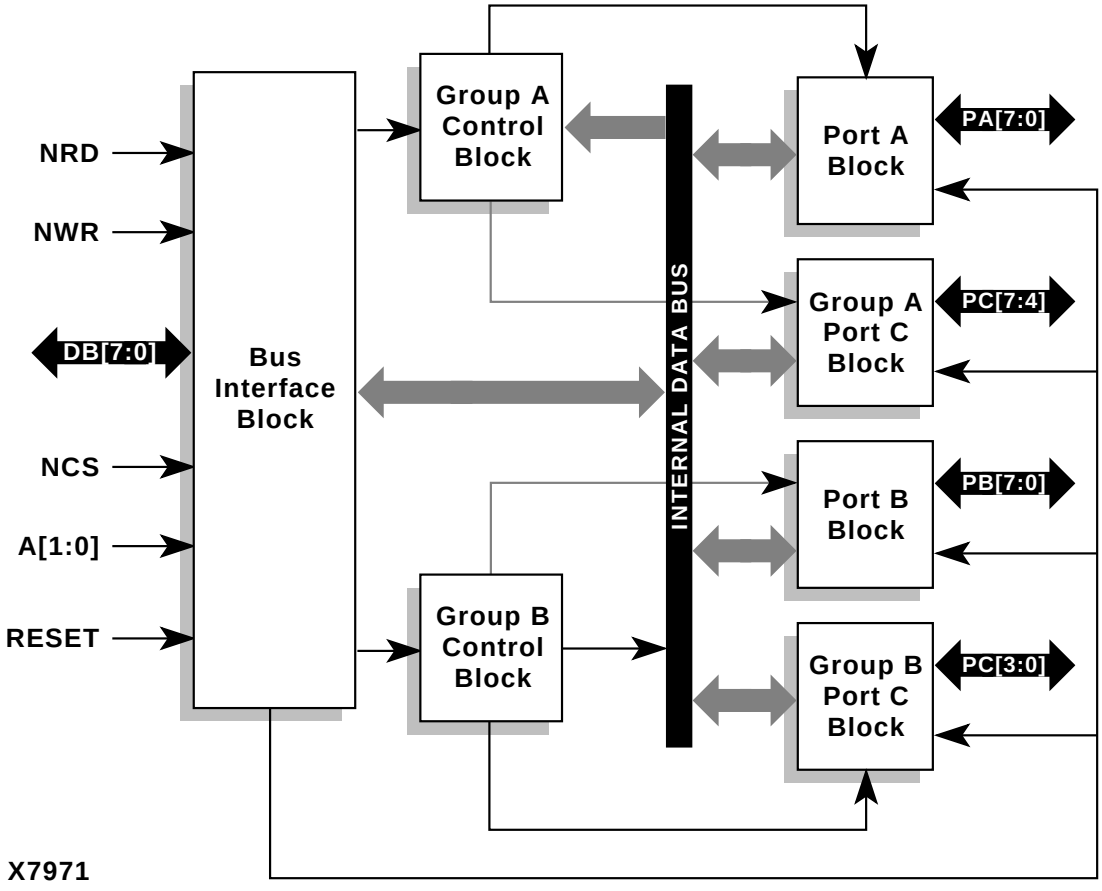

Figure 1: M8255 Functional Block Diagram

Functional Description

The M8255 core is partitioned into modules as shown in Figure 1 and described below.

Bus Interface Block

This block handles CPU Interface, and generates necessary control signals to pass CPU data to control and port blocks.

Group A Control Block

This block handles mode selection and control functions of Port A and Port C blocks for PC[7:4].

Group B Control Block

This block handles mode selection and control functions of Port B and Port C blocks for PC[3:0].

Port A Block

This block provides input and output latches to interface PA[7:0] data to external peripherals.

Port B Block

This block provides input and output latches to interface PB[7:0] data to external peripherals.

Group A Port C Block

This block provides the input and output latches to interface PC[7:4] data to external peripherals. This block also provides the interface to handshake signals in modes 1 and 2.

Group B Port C Block

This block provides the input and output latches to interface PC[3:0] data to external peripherals. This block also provides the interface to handshake signals in modes 1 and 2.

Core Modifications

Virtual IP Group, Inc. can integrate multiple M8255s to increase I/O capacity upon request.

Pinout

The pinout has not been fixed to specific FPGA I/O allowing flexibility with the user application. A pinout is suggested for use with a user-constructible evaluation board. Information for this is in the FPGA Design Document included with the core. Signal names are provided in the block diagram shown in Figure 1 and described in Table 1.

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
Bus Interface Signals		
NRD	Input	Read Enable used by host processor to read a byte from selected data port register; active low.
NWR	Input	Write Enable used by host processor to write a byte to data port or control register; active low.
DB[7:0]	In/Out	8 bit bi-directional CPU data bus.
NCS	Input	Chip Enable for accessing internal registers including Port registers for reads or writes; active low.
A[1:0]	Input	2 bit address from CPU to determine In/Out port accessed during Read or Write cycles.
RESET	Input	Reset, active high.
Port Signals		
PA[7:0]	In/Out	8 bit bi-directional Port A data bus.
PB[7:0]	In/Out	8 bit bi-directional Port B data bus.
PC[7:0]	In/Out	8 bit bi-directional Port C data bus.

Verification Methods

The core has been tested with in-house developed test vectors that are provided with the core.

Recommended Design Experience

Knowledge of DMA interfaces in a microprocessor based systems is required. The user must be familiar with HDL design methodology, instantiation of Xilinx netlists in a hierarchical design environment and usage of Xilinx Foundation or Alliance development tools.

Available Support Products

FPGA Evaluation Board

The FPGA Design Document included with the core gives directions for constructing a general purpose FPGA evaluation daughter board that can be plugged into a standard part socket on the target system through a flat cable.

Ordering Information

This product is available from Virtual IP Group, Inc. Please contact them for pricing and additional information.

Related Information

Refer to Specification Document for programming of this core for a typical system application. The user should refer to the Desginer's Application Note for integrating this with other cores. Both documents are included with the core.

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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