# XF8255 Programmable Peripheral Interface

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Product Specification

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## Features

- Software and function compatible with Industry Standard 8255
- MCS-85 compatible
- 24 programmable I/O pins
- Fully compatible with most microprocessor families
- Direct bit set/reset capability easing control application interface

## Applications

- Embedded Microprocessor Control

## General Description

The XF8255 Programmable Peripheral Interface Core is a general purpose programmable I/O device designed for use with most microprocessors. It has 24 I/O pins which may be individually programmed in two groups of 12 and used in three major modes of operation.

The first mode, MODE 0, is basic input/output operation where ports A and B are 8 bits wide and Port C is split into upper and lower halves of 4 bits each. Port A, Port B, Port C upper, and Port C lower can each be independently configured as input or output. This gives a total of 16 direction combinations.In MODE 1 each group may be programmed to have eight lines of input or output. Of the remaining four pins, three are used for handshaking and interrupt control signals.

The third mode of operation, MODE 2, is only available on the Group A ports (Port A and Port C upper). It is a bi-directional bus mode that uses eight lines for a bi-directional bus, and five lines, borrowing one from the other group, for handshaking and interrupt control signals.

## AllianceCORE™ Facts

| Core Specifics | | |
|---|---|---|
| Device Family | XC5200 | |
| CLBs Used | 57 | |
| IOBs Used | 38[1] | |
| System Clock $f_{max}$ | No External Clock[2] | |
| Device Features Used | Tbufs, global clock buffers | |
| **Supported Devices/Resources Remaining** | | |
| | **I/O** | **CLBs** |
| XC5202-5[3] PC84 | 27[1] | 7 |
| **Provided with Core** | | |
| Documentation | Core schematics<br>Implementation instructions | |
| Design File Formats | ViewLogic schematic files<br>Live hierarchical tree<br>LCA Files | |
| Verification Tool | Machine-readable simulation vectors for ViewLogic ViewSim | |
| Schematic Symbols | ViewLogic | |
| Constraint Files | TimeSpecs | |
| Evaluation Model | None | |
| Reference designs & application notes | None | |
| Additional Items | Warranty by MDS | |
| **Design Tool Requirements** | | |
| Xilinx Core Tools | XACTstep 6.0.0 | |
| Entry/Verification Tools | ViewLogic PROcapture 6.1<br>or Workview Office | |
| **Support** | | |
| Memec Design Services warrants that the design delivered by Memec Design Services will conform to the design specification. This warranty expires 3 months from the date of delivery of the design database. Contact Memec Design Services for the Design License Agreement with complete Terms and Conditions of Sale. | | |

Notes:

1. Assuming all core signals are routed off-chip.
2. Function does not have a clock, but will, at a minimum, perform no wait-state operation alongside an 8 MHz 80C86.
3. Specific devices are minimum size and speed recommended - the core will work in any larger or faster devices from the same families.

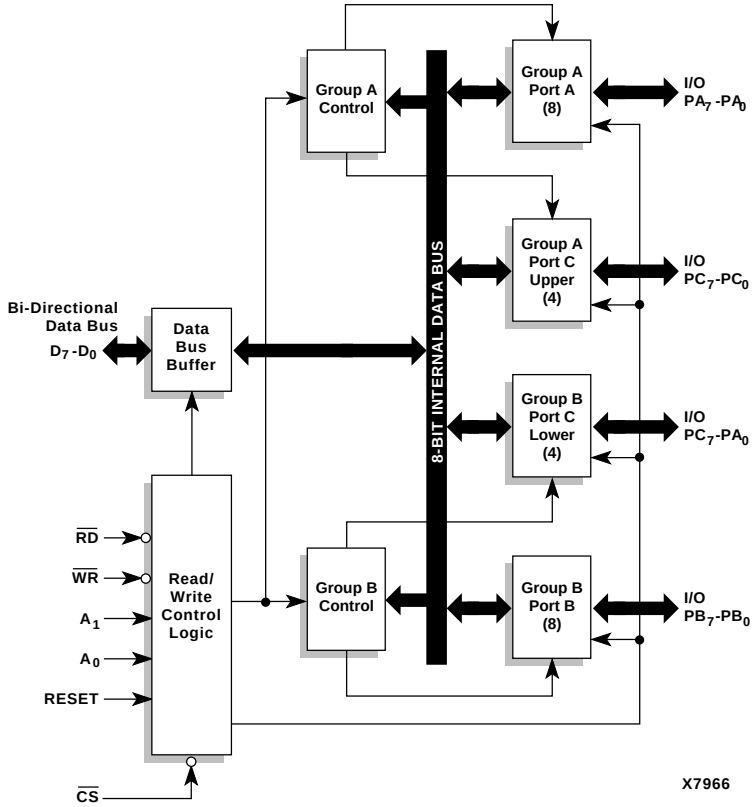


**Figure 1: XF8255 Block Diagram**

## Functional Description

The XF8255 is partitioned into modules as shown in Figure 1 and described below.

### Data Bus Buffer

This is a 3-state bi-directional 8-bit buffer used to interface the XF8255 to the system data bus.

### Read/Write Control Logic

This logic manages all of the internal and external transfers of both Data and Control or Status words.

### Group A and Group B Controls

The functional configuration of each port is programmed by the system software. Each of the Control blocks (Group A and Group B) accepts “commands” from the Read/Write Control Logic, receives “control words” from the internal data bus, and issues the proper commands to its associated ports.

### Port A:

One 8-bit data output latch/buffer and one 8-bit data input latch.

### Port B:

One 8-bit data input/output latch/buffer and one 8-bit data input buffer.

### Port C:

One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control.

Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.

# Pinout

The XF8255 may be implemented as stand-alone logic using the provided pinout or may be implemented internally with the users design. Both versions are included with the Core deliverables. Signal names are provided in the block diagram shown in Figure 1, and Table 1.

# Core Assumptions

Deviations from the Harris 82C55A functional specification are described below. Memec Design Services will perform any of the listed modifications upon request.

## IBF Flip-flops

The Input Buffer Full (IBF) flip-flops on ports A and B are not cleared when RESET is asserted. This is because the Xilinx architecture does not easily support D flip-flops with both asynchronous Set and asynchronous Reset.

Workaround: Perform a dummy read of ports A and B sometime after RESET is pulsed. This will clear the IBF flip-flops.

## Input Side Interrupt Request Flip-flops

The input side Interrupt Request (IN_INTR) flip-flops for Port A MODEs 1 and 2 and Port B MODE 1 are cleared asynchronously (level sensitive) when a read is performed on the port. The timing diagram (Figure 7) in the Harris 82C55A data sheet agrees with our implementation, however, the text in the data sheet says it is reset by the falling edge of RD.

**Workaround**: Since the Harris data sheet is inconsistent on this point and since our XF8255 still meets all the timing relationships indicated in Figure 7 of the Harris 82C55A data sheet, this change should be transparent to the user.

The input side Interrupt Request (IN_INTR) flip-flops for Port A MODEs 1 and 2 and Port B MODE 1, are set on the RISING EDGE of STBx_L when IBFx, INTEx, and Px_RD_L are high. The Harris data sheet indicates that this should be LEVEL sensitive. Since the Xilinx architecture does not easily support flip-flops with both asynchronous Set and Asynchronous Reset, we chose to use the rising edge of STBx_L to set the flip-flop.

**Workaround:** Since our XF8255 still meets all the timing relationships indicated in Figure 7 of the Harris 82C55A data sheet, this change should be transparent to the user.

## Output Side Interrupt Request Flip-flops

The output side Interrupt Request (OUT_INTR) flip-flops for Port A MODEs 1 and 2 and Port B MODE 1, are cleared asynchronously (level sensitive) when a write is performed on the port. The timing diagram (Figure 9) in the Harris 82C55A data sheet agrees with our implementation, however, the text in the data sheet says it is reset by the falling edge of WR.

**Table 1: Core Signal Pinout**

| Signal | Signal Direction | Description |
|---|---|---|
| **Control Signals** | | |
| RD- | Input | READ: used by the CPU to read status information or data via the data bus; active low |
| WR- | Input | WRITE: used by the CPU to load control words and data into the 82C55A; active low |
| A0-A1 | Input | ADDRESS: used in conjunction with RD- and WR- inputs to control selection of the control word register ports. A0 and A1 are normally connected to the least significant bits of address bus A0, A1 |
| RESET | Input | RESET: A high on this input clears the control register and all ports (A,B,C) are set to input mode with “bus hold” circuitry turned on |
| CS- | Input | CHIP SELECT: used to enable the 802C55A onto the data bus for CPU communications; active low |
| **Port and Data Bus Signals** | | |
| D0-D7 | In/Out | DATA BUS: bidirectional three-state pins connected to system data bus |
| PA0-PA7 | In/Out | PORT A: 8-bit input and output port. Both bus hold high and bus hold low circuitry are present on this port |
| PB0-PB7 | In/Out | PORT B: 8-bit input and output port. Bus hold high circuitry is present on this port |
| PC0-PC7 | In/Out | PORT C: 8-bit input and output port. Bus hold circuitry is present on this port |

**Workaround:** Since the Harris data sheet is inconsistent on this point and since our XF8255 still meets all the timing relationships indicated in Figure 9 of the Harris 82C55A data sheet, this change should be transparent to the user.

The output side Interrupt Request (OUT_INTR) flip-flops for Port A MODEs 1 and 2 and Port B MODE 1, are set on the RISING EDGE of ACKx_L when OBFx_L, INTEx, and Px_WR_L are high. The Harris data sheet indicates that this should be LEVEL sensitive. Since the Xilinx architecture does not easily support flip-flops with both asynchronous Set and asynchronous Reset, we chose to use the rising edge of ACKx_L to set the flip-flop.

**Workaround:** Since our XF8255 still meets all the timing relationships indicated in Figure 9 of the Harris 82C55A data sheet, this change should be transparent to the user.

### Bus-Hold Capability

Ports A, B, and C do not have Bus-Hold capability. This would require two OBUFTs per port pin. Since Xilinx devices only have one OBUFT per pin, it would take two Xilinx pins connected together externally for each port pin.

Workaround: Most applications don't require Bus-Hold capability, but for those that do, a customized version of the XF8255 macro can be developed.

## Core Modifications

The XF8255 is designed to meet or exceed the AC Specifications of the Harris 82C55A. However, in most cases the Timespecs can be tightened significantly. In all cases, a post-route timing analysis should be performed to verify performance. Implementation and other customizing is available through Memec Design Services.

## Verification Methods

Complete functional and timing simulation has been performed on the XF8255 using Viewsim. (Simulation vectors used for verification are provided with the core.) The README.TXT file has a short description of four top level CMD files used to simulate the design. These CMD files call other CMD files and all the CMD files have descriptions and comments as to their purpose.

### Recommended Design Experience

Users should be familiar with ViewLogic PROcapture or Office schematic entry and Xilinx design flows. Users should also have experience with microprocessor systems.

### Ordering Information

The XF8255 Programmable Peripheral Interface Core is provided under license from Memec Design Services for use in Xilinx programmable logic devices and Xilinx HardWire™ gate arrays. Please contact the partner for pricing and more information.



## Related Information

Harris Semiconductors 82C55A CMOS Programmable Peripheral Interface data sheet at: www.harris.com.

### Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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