XF8256 Multifunction Microprocessor Support Controller

October 20, 1997

Product Specification

Maria Aguilar, Project Coordinator
Memec Design Services
1819 S. Dobson Rd., Suite 203
Mesa, AZ 85202
Phone: +1 888-360-9044 (USA)
+1 602-491-4311 (international)
Fax: +1 602-491-4907
E-mail: info@memecdesign.com
URL: www.memecdesign.com

Features

- Programmable serial asynchronous communications interface for 5-, 6-, 7-, or 8-bit characters, 0.75, 1, 1.5, or 2 stop bits, and parity generation
- On-board baud rate generator programmable for 13 common baud rates up to 19.2 K bits/second, or an external baud clock maximum of 1M bit/second
- Five 8-bit programmable timer/counters; four can be cascaded to two 16-bit timer/counters
- Two 8-bit programmable parallel I/O ports; port 1 can be programmed for port 2 handshake controls and event counter input
- Eight-level priority interrupt controller programmable for 8085, 8086/88, 80186/188 systems and for fully nested interrupt capability
- Programmable system clock to 1x, 2x, 3x, or 5x 1.024 MHz

Applications

- Serial communications
- Process control
- Embedded systems

AllianceCORE™ Facts

Core Specifics		
Device Family	XC4000E	XC5200
CLBs Used	137	64
IOBs Used	38[1]	38[1]
System Clock f_{max}	10+ MHz[2]	
Device Features Used	Tbufs, global clock buffers	

Supported Devices/Resources Remaining		
	I/O	**CLBs**
XC4005E-4[3] PC84C	29[1]	59
XC5202PC84-5[3]	33[1]	0

Provided with Core	
Documentation	Core schematics Implementation instructions
Design File Formats	ViewLogic schematic files Live hierarchical tree LCA Files
Constraint Files	None
Schematic Symbols	ViewLogic
Verification Tool	Machine-readable simulation vectors for ViewLogic ViewSim
Evaluation Model	None
Reference designs & application notes	None
Additional Items	Warranty by MDS

Design Tool Requirements	
Xilinx Core Tools	XACTstep 6.0.0
Entry/Verification Tools	ViewLogic PROcapture 6.1 or Workview Office

Support

Memec Design Services warrants that the design delivered by Memec Design Services will conform to the design specification. This warranty expires 3 months from the date of delivery of the design database. Contact Memec Design Services for the Design License Agreement with complete Terms and Conditions of Sale.

Notes:
1. Assuming all core signals are routed off-chip.
2. Minimum guaranteed speed.
3. Specific devices are minimum size and speed recommended - the core will work in any larger or faster devices from the same families.

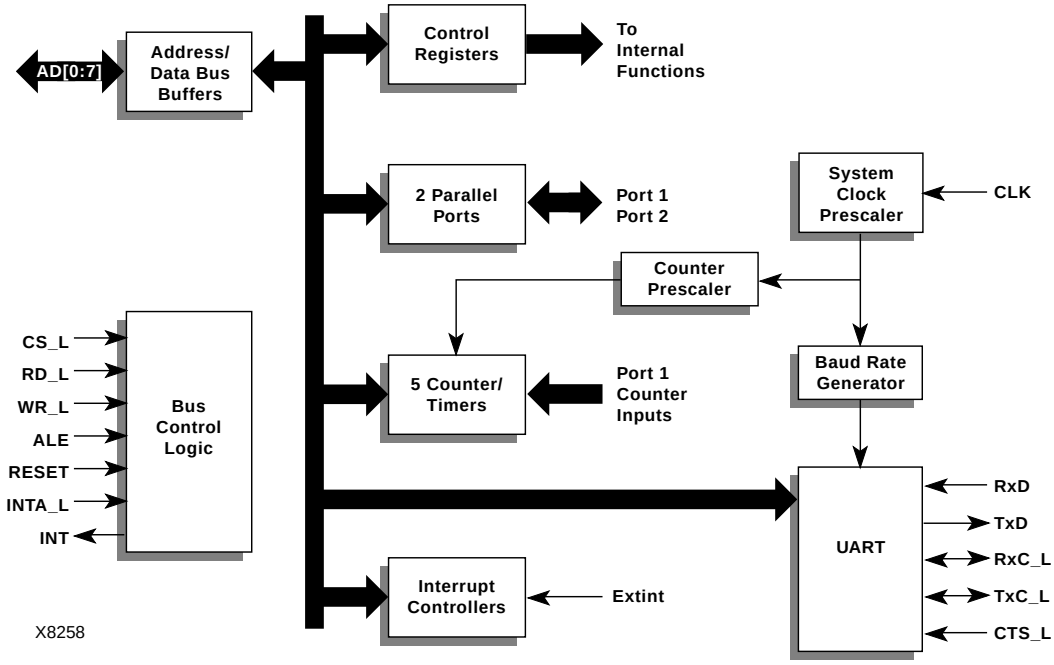

Figure 1: XF8256 Block Diagram

General Description

The XF8256 multifunction universal asynchronous receiver -transmitter combines five commonly used functions into a single device: serial communications, parallel I/O, timing, event counting, and priority interrupt functions.

It is designed to interface to the 8085, 8086/88, 80186/188, and 8051. All of these functions are fully programmable through internal registers. In addition, the five timer/ counters and two parallel I/O ports can be accessed directly by the microprocessor.

Functional Description

The block diagram with internal structure is shown in Figure 1, and described below.

Control Registers

These store commands and input and output data.

Parallel Ports

This block provides two 8-bit general purpose parallel ports. Port 2 has handshake capability and the eight bits of port 1 can be individually defined as input or output.

Counter/Timers

This block provides five 8-bit counter/timers with either 1 kHz or 16 kHz clocks. Four of them can be cascaded to form two 16-bit counter/timers.

Interrupt Controller

This block functions as an eight-level priority interrupt controller with fully nested or normal interrupt priority modes.

System Clock Prescaler

This provides division ratios of 5, 3, 2, and 1 to generate the internal clock operating frequency of 1.024 MHz.

Baud Rate Generator

This block is a programmable baud rate generator with selectable internal or external clock inputs.

UART

This block is a full-duplex serial asynchronous receiver-transmitter with 32x or 64x sampling rate.

Core Modifications

With little effort, the XF8256 can be broken into sub-functions that can be used as needed. Multiple XF8256s can be instantiated into one device to perform functions in parallel. Timing specifications are not critical and can be tightened significantly.

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
Bus Control Signals		
CS_L	Input	**Chip select:** Low input enables interface functions to send or receive, latched with address on falling edge of ALE. RD_L and WR_L have no effect unless CS_L was latched low during ALE cycle.
RD_L, WR_L	Input	**Read and write control:** Enables data buffers to send or receive, data external.
ALE	Input	**Address latch enable:** Latches address on AD[0:4] and CS_L on falling edge.
RESET	Input	**Reset:** Active high input forces core into initial state until control information is written.
INTA_L	Input	**Interrupt acknowledge:** If core enabled for interrupts, INTA_L indicates interrupt request is being acknowledged by microprocessor. During acknowledgment, the core puts an RSTn instruction (8-bit mode) or a vector (16-bit mode) on data bus.
INT	Output	**Interrupt request:** A high signals processor for interrupt service.
UART Signals		
RxD	Input	**Receive data:** Serial data input.
TxD	Output	**Transmit data:** Serial data output.
RxC_L	In/Out	**Receive clock:** In/Out programmable. As input, it clocks serial data into RxD pin on rising edge of RxC_L. As output, rising edge indicates data on RxD is being sampled. Output remains high during start, stop, and parity bits.
TxC_L	In/Out	**Transmit clock:** In/Out program. As input, it clocks data out of transmitter on falling edge or it can permit use of 32x or 64x clock for receiver and transmitter. As output, it presents internal transmitter clock.
CTS_L	Input	**Clear to send:** Enables serial transmitter; as level sensitive, with CTS_L low, characters loaded into transmit buffer register are transmitted serially; a negative pulse transmits previous character. For edge sensitive, a negative edge on CTS_L transmits next character.
I/O and Clock Signals		
AD[0:7]	In/Out	**Address/data:** Three-state interface to lower 8-bits of processor's multiplexed address/data bus. 5-bit address latched on falling edge of ALE. In 8-bit mode, AD[0:3] selects proper register and AD [1:4]is ignored. In 16-bit mode AD[1:4] selects register and AD0 acts as second chip select, active low.
P1[0:7]	In/Out	**Parallel I/O port 1:** Pin-programmable as general purpose input or output. All outputs latched, inputs are not. Can also serve as functional control pins.
P2[0:7]	In/Out	**Parallel I/O port 2:** 8-bit general-purpose I/O port. Each nibble can input or output. Outputs are latched, inputs are not. Can also be used as 8-bit input or output port when using two-wire handshake mode where both inputs and outputs are latched.
CLK	Input	**System clock:** Used to generate internal timing.

Table 1: Core Signal Pinout (cont.)

Signal	Signal Direction	Description
EXTINT	Input	**External interrupt request:** Input is level-high sensitive; must be held high until an interrupt acknowledge occurs.

In all cases, a functional and post-route timing analysis should be performed to verify performance. Implementation and customizing is available through Memec Design Services.

Pinout

The XF8256 may be implemented internally with the user's design or as stand-alone logic with the pinout that is provided with the Core. For a fast replacement of the industry standard 8256, MDS offers a 40-pin device carrier that is pin-compatible. Signal names are provided in the block diagram shown in Figure 1 and described in Table 1.

Verification Methods

Basic functional simulation has been performed on the XF8256 using ViewSim. Simulation vectors used for verification are provided with the core. This FPGA design was also physically tested and compared with the industry standard 8256 for verification purposes.

Additional Support Products

Memec Design Services supplies a Xilinx-based FPGA Development Module that can be used to hardware test this and other MDS cores. To purchase this, or obtain more information, contact MDS directly.

Recommended Design Experience

Users should be familiar with ViewLogic PRO series or Workview Office schematic entry and Xilinx design flows. Users should also have experience with microprocessor systems.

Ordering Information

The XF8256 Multifunction Microprocessor Support Controller is provided under license from Memec Design Services for use in Xilinx programmable logic devices and Xilinx HardWire™ gate arrays. To purchase or make further inquiries about this or other Memec Design Services products, contact MDS directly at the location listed on the front page.

Related Documentation and Information

Intel 8256AH Multifunction Microprocessor Support Controller, data sheet, 1994, order number 230759-002.

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
URL: www.xilinx.com

For general Xilinx literature, contact:

Phone: +1 800-231-3386 (inside the US)
+1 408-879-5017 (outside the US)
E-mail: literature@xilinx.com

For AllianceCORE™ specific information, contact:

Phone: +1 408-879-5381
E-mail: alliancecore@xilinx.com
URL: www.xilinx.com/products
/logicore/alliance/tblpart.htm