XF8279 Programmable Keyboard Display Interface

October 20, 1997 | Product Specification

Maria Aguilar, Project Coordinator
Memec Design Services
1819 S. Dobson Rd., Suite 203
Mesa, AZ 85202
Phone: +1 888-360-9044 (in the USA)
+1 602-491-4311 (international)
Fax: +1 602-491-4907
E-mail: info@memecdesign.com
URL: www.memecdesign.com

Features

- Simultaneous keyboard display operations
- Scanned keyboard mode
- Scanned sensor mode
- Strobed input entry mode
- 8-character keyboard FIFO
- 2-key lockout or N-Key rollover with contact debounce
- Dual 4, 8, or 16 numerical display
- Single 8 or 16 character display
- Mode programmable from CPU
- Right or left entry 16-Byte display RAM
- Programmable scan timing
- Interrupt output on key entry

Applications

- User interface for embedded systems

General Description

The XF8279 is a general purpose programmable keyboard and display I/O interface device designed for use with 8-bit microprocessors. This core is functionally compatible with the industry standard 8279 and relieves the CPU from scanning the keyboard or refreshing the display.

The keyboard portion can provide a scanned interface to a 64-contact key matrix such as typewriter style keyboards or thumb switches. The keyboard portion will also interface to an array of sensors or a strobed interface keyboard, such as the Hall effect and ferrite variety. Keyboard entries are debounced and strobed into an 8-character FIFO. Key entries set the interrupt output line to the CPU.

AllianceCORE™ Facts

Core Specifics	
Device Family	XC4000E
CLBs Used	171
IOBs Used	38[1]
System Clock f_{max}	8 MHz[2]
Device Features Used	RAM, OSC4, 3BUFGs

Supported Devices/Resources Remaining		
	I/O	CLBs
XC4005EPQ100-4	39[1]	25

Provided with Core	
Documentation	Core schematics Implementation instructions
Design File Formats	ViewLogic schematic files Live hierarchical tree LCA Files
Constraint Files	None
Schematic Symbols	ViewLogic
Verification Tool	Machine-readable simulation vectors for ViewLogic ViewSim
Evaluation Model	None
Reference designs & application notes	None
Additional Items	Warranty by MDS

Design Tool Requirements	
Xilinx Core Tools	XACTstep 6.0.0/XACT M1.2
Entry/Verification Tools	ViewLogic PRO series or Workview Office

Support

Memec Design Services warrants that the design delivered by Memec Design Services will conform to the design specification. This warranty expires 3 months from the date of delivery of the design database. Contact Memec Design Services for the Design License Agreement with complete Terms and Conditions of Sale.

Notes:
1. Assuming all core signals are routed off-chip.
2. Minimum guaranteed speed.
3. Specific devices are minimum size and speed recommended - the core will work in any larger or faster devices from the same families.

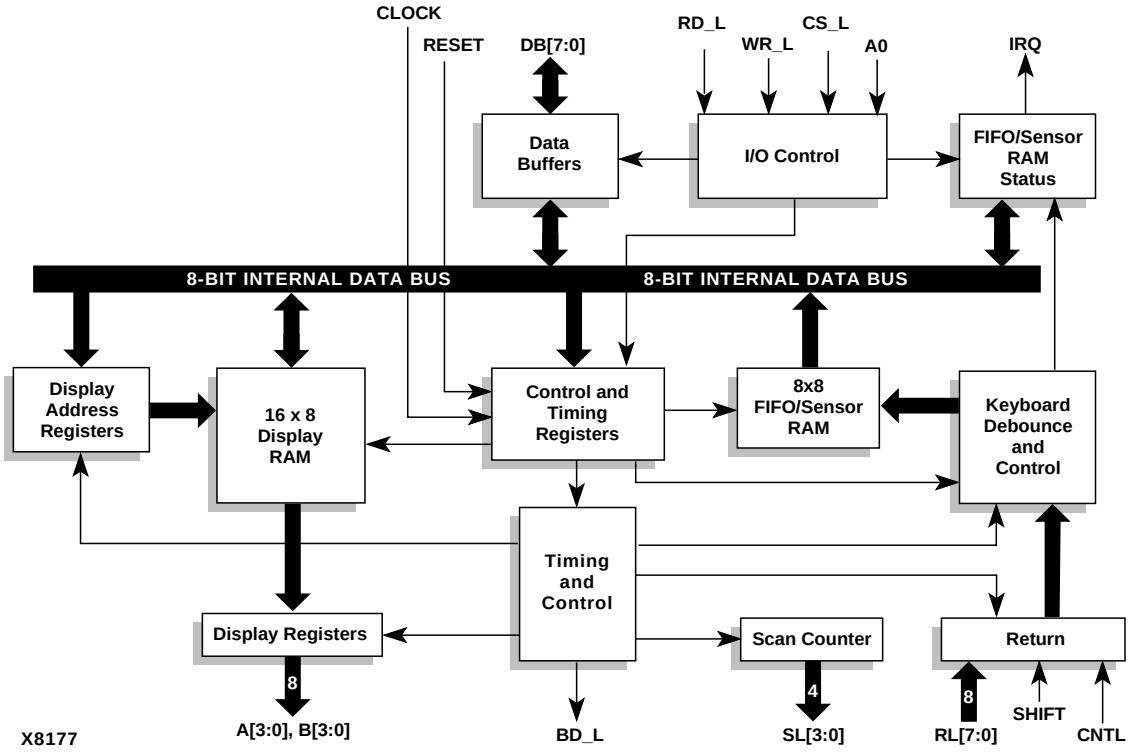

Figure 1: XF8279 Block Diagram

The display portion provides a scanned display interface for LED, incandescent, and other popular display technologies. Both numeric and alphanumeric segment displays may be used as well as simple indicators. The XF8279 has a 16 x 8 display RAM that can be organized into dual 16 x 4 RAMs. The RAM can be loaded or interrogated by the CPU. Both right entry calculator and left entry typewriter display formats are possible. Both read and write of the display RAM can be done with auto increment of the display RAM address.

Functional Description

The XF8279 is partitioned into modules as shown in Figure 1 and described below.

Display Address Registers

These registers hold the write or read display RAM address. They also perform the auto increment function.

Display RAM

This stores the data being displayed.

Display Registers

These registers hold display data during digit switching.

Data Buffers

This block provides direct data output and interface to external bus.

I/O Control

This block controls data flow between internal registers and external bus.

Control and Timing Registers

CPU commands are stored in these registers.

Timing and Control

Reset operations and command functions are accomplished in this block.

FIFO/Sensor RAM

This block provides FIFO or 8x8 RAM for sensor mode.

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
CLOCK	Input	**Clock:** Clock from system used to set scan frequency.
RESET	Input	**Reset:** A high input resets the XF8279.
DB[7:0]	In/Out	**Bi-directional data bus:** Three-state data and command bus between CPU and XF8279.
RD_L, WR_L	Input	**I/O Read and Write:** Enables data buffers to send or receive data from external bus.
CS-L	Input	**Chip Select:** A low input enables interface functions to read or write.
A_0	Input	**Buffer Address:** A high input indicates signals are interpreted as a command or status; a low indicates they are data.
IRQ	Output	**Interrupt Request:** In keyboard mode, IRQ is high when data is in FIFO/Sensor RAM. In sensor mode, interrupt line goes high whenever a sensor change is detected.
A[3:0] B[3:0]	Output	**Outputs:** Two data outputs for 16X4 display; ports may be blanked independently.
BD-L	Output	**Blank Display:** Output blanks display during digit switching or can be set by a display blanking command.
SL[3:0]	Output	**Scan Lines:** Used to scan key switch or sensor matrix and display digits; can be either encoded (1 of 16) or decoded (1 of 4).
RL[7:0]	Input	**Return Line:** Inputs connected to scan lines through keys or sensor switches; internal pull-up resistors keep them high until a switch closure pulls one low.
Shift	Input	**Shift:** Shift-input status is stored along with key position on key closure in keyboard modes; it has an internal pull-up resistor.
CNTL	Input	**Control/Strobed Input Mode:** Status is stored on rising-edge; data into FIFO. It has an internal pull-up resistor.

Scan Counter

This counter has two modes. In encoded mode, the scan counter needs an external decoder to provide the scan lines for the keyboard and display. In decoded mode, the scan counter provides a decoded output, however, the keyboard matrix is reduced to 4x8 and only 4 characters can be displayed.

FIFO/Sensor RAM Status

This block keeps track of how many characters are in the FIFO and provides flags for different functional conditions.

Keyboard Debounce and Control

In keyboard mode, this block debounces the return lines. In sensor and strobed modes, data is directed and transferred directly to the FIFO/Sensor RAM.

Return

This block buffers and registers data from the Return, Control, and Shift input lines.

Core Modifications

The XF8279 is designed to meet or exceed the AC Specifications of the Intel 8279. However, in most cases the Timespecs can be tightened significantly. In all cases, a post route timing analysis should be performed to verify performance. Implementation and customizing are available through Memec Design Services.

Pinout

The XF8279 may be implemented internally with the user's design or as stand alone logic with the pinout that is provided with the Core. For a fast replacement of the industry standard 8279 we provide a 40-pin device carrier which is pin compatible. Signal names are provided in the block diagram shown in Figure 1 and in Table 1.

Core Assumptions

There is an important deviation in the design implementation. The internal timing is fixed to 8 MHz (using OSC4) and only the scan frequency is controlled by the external clock. The scan frequency is then synchronized with the internal clock. The reason for this is to meet and exceed the read and write cycle time. However, to our best understanding and practical experience, there are no deviations from the

Intel 8279 functional specifications. Memec Design Services will perform any modification if a deviation is found.

Verification Methods

Basic functional simulation has been performed on the XF8279 using ViewSim. (Simulation vectors used for verification are provided with the core). The design was also physically tested in three different environments and two different Xilinx FPGA devices without any problem.

Recommended Design Experience

Users should be familiar with ViewLogic PRO series or Workview Office schematic entry and Xilinx design flows. Users should also have experience with microprocessor systems.

Available Support Products

Memec Design Services supplies a Xilinx-based FPGA Development Module that can be used to hardware test this and other MDS cores. To purchase this, or obtain more information, contact MDS directly.

Ordering Information

The XF8259 Programmable Keyboard Display Interface is provided under license from Memec Design Services for use in Xilinx programmable logic devices and Xilinx HardWire™ gate arrays. To purchase or make further inquiries about this or other Memec Design Services products, contact MDS directly at the location listed on the front page.

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Related Documentation and Information

Intel 8279/8279-5 Programmable Keyboard/Display Interface, data sheet, 1993, order number 290123-002.

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
URL: www.xilinx.com

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E-mail: literature@xilinx.com

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