XF8250 Asynchronous Communications Core

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Features

- Software and function compatible with Industry Standard 8250
- Single macro UART and Baud Rate Generator
- DC to 625K baud (DC to 10 MHz Clock)
- External clock input In-macro Baud Rate Generator
- 1 to 65535 divisor generates 16X clock
- Prioritized interrupt mode
- Microprocessor bus oriented interface
- 80C86/80C88 compatible
- Modem interface Line break generation and detection
- Loopback and Echo modes

Applications

- Serial data communications applications
- Logic consolidation

General Description

The XF8250 Asynchronous Communications Core is a high-performance programmable Universal Asynchronous Receiver/Transmitter (UART) and Baud Rate Generator (BRG).

The Harris 82C50A datasheet, dated January 1992, is the target functional specification for the XF8250. The AC Specifications, both Timing Requirements and Timing, are met or exceeded in every case. A post-route timing analysis should be used to verify performance. Memec Design Services (MDS) can assist with this.

AllianceCORE™ Facts

Core Specifics			
Device Family	Spartan	XC4000E	XC5200
CLBs Used	97	97	64
IOBs Used	35[1]		
Systems Clock f_{max}	10+ MHz[2]		
Device Features Used	Tbufs, global clock buffers		

Supported Devices/Resources Remaining		
	I/O[1]	CLBs
XC4005E-6[3]	26	99
XC5202-6[3]	30	0
XCS05-3 PC84[3]	26	99

Provided with Core	
Documentation	Core schematics Implementation instructions
Design File Formats	ViewLogic Schematic files Live hierarchical tree LCA Files
Constraint Files	TimeSpecs
Verification Tool	Machine-readable simulation vectors for ViewLogic ViewSim
Schematic Symbols	ViewLogic
Evaluation Method	None
Reference designs & application notes	None
Additional Items	Warranty by MDS

Design Tool Requirements	
Xilinx Core Tools	Alliance/Foundation 1.3

Memec Design Services warrants that the design delivered by Memec Design Services will conform to the design specification. This warranty expires 3 months from the date of delivery of the design database. Contact Memec Design Services for the Design License Agreement with complete “Terms and Conditions of Sale.”

Notes:
1. Assuming all core signals are routed off-chip.
2. Minimum guaranteed speed to meet Harris specification.
3. Specific devices are minimum size and speed recommended - the core will work in larger or faster devices from the same families.

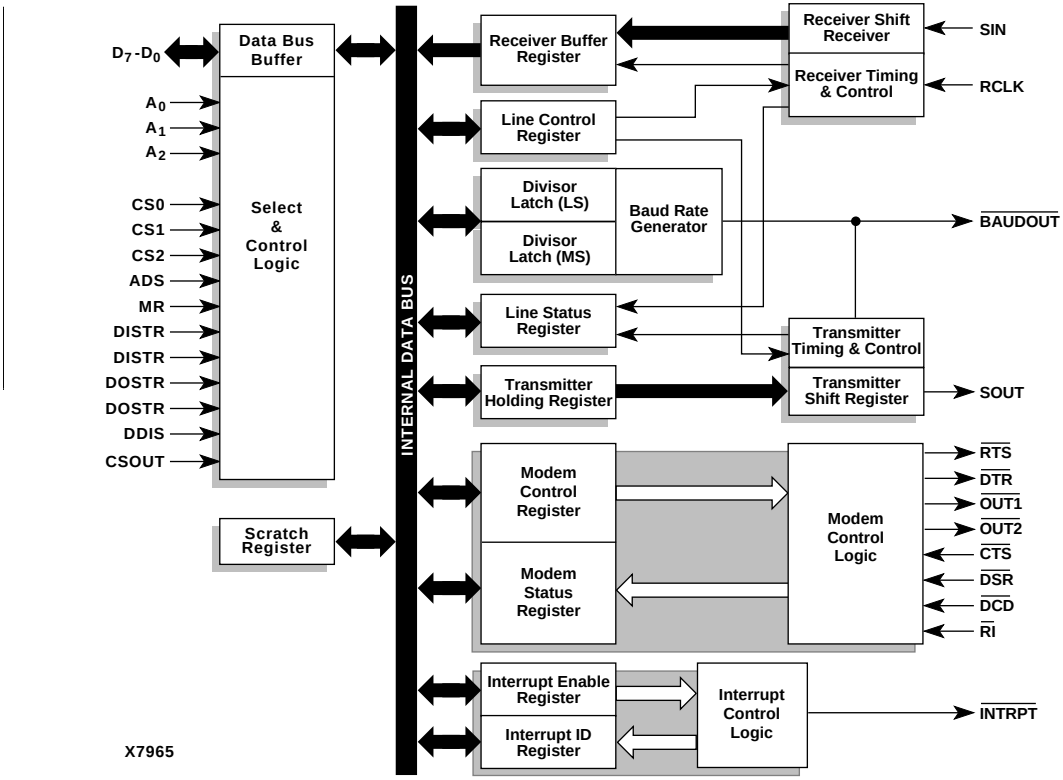

Figure 1: XF8250 Block Diagram

The Absolute Maximum Ratings, Operating Conditions, DC Electrical Specifications, and Capacitance are device dependent and can be found in the Xilinx datasheet for the target device.

Functional Description

The XF8250 is partitioned into modules as shown in Figure 1 and described below.

Select and Control Logic

This controls decodes for the core and the direction of the data bus buffer.

Receiver Timing & Control

This block detects the start-bit, controls the sampling of the asynchronous receive data (SIN), and determines when a complete word has been shifted into the receiver shift register.

Line Control Register (LCR)

This register controls the format of the data character. The contents of the LCR may be read, eliminating the need for separate storage of the line characteristics in system memory.

Line Status Register (LSR)

A single register that provides status indications. The LSR is usually the first register read by the CPU to determine the cause of an interrupt or to poll the status of the XF8250.

Modem Control Register

This controls the interface to the modem or data set. The MCR can be written to and read from.

Modem Status Register

This provides the CPU with the status of the modem input lines from the external device. The MSR allows the CPU to read the modem signal inputs by accessing the data bus interface of the XF8250.

Baud Rate Generator

This divides the clock by a 16-bit divisor to generate the 16x baud rate clock (BAUDOUT).

Receiver Shift Register

This register is programmable for 5, 6, 7, or 8 data-bits per character.

Transmitter Holding Register

This register holds parallel data from the data bus (D0-D7) until the Transmitter Shift Register is empty and ready to accept a new character for transmission.

Scratch Register

This register is an 8-bit Read/Write register which has no effect on the XF8250. It is intended as a scratch pad register to be used by the programmer to hold temporary data.

Interrupt ID Register

This register provides the XF8250 with interrupt capability for interfacing to microprocessors. In order to minimize software overhead during data character transfers, the XF8250 four levels of interrupt priorities:

- Priority 1 - Receiver Line Status
- Priority 2 - Received Data Ready
- Priority 3 - Transmitter Holding Register Empty
- Priority 4 - Modem Status

Interrupt Enable Register

This is a Write register used to independently enable the four XF8250 interrupts which activate the interrupt (INTRPT) output.

Core Modifications

The XF8250 meets or exceeds the AC Specifications of the Harris 82C50A-5. However, in most cases the TimeSpecs can be tightened significantly. Successful operation with 120 ns bus cycles has been achieved. In all cases, a post-route timing analysis should be performed to verify performance. Implementation beyond 10 MHz and other customizing is available through Memec Design Services.

Pinout

The XF8250 may be implemented as stand-alone logic using the provided pinout or may be implemented internally with the user's design. Both versions are included with the Core deliverables. Signal names are provided in the block diagram shown in Figure 1, and Table 1.

Core Assumptions

Deviations from the Harris 82C50 functional specification are described below. Memec Design Services will perform any of the listed modifications upon request.

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
D7-D0	In/Out	Data bits 7-0
A0	Input	Register Reset 0
A1	Input	Register Reset 1
A2	Input	Register Reset 2
CS0	Input	Chip Select 0
CS1	Input	Chip Select 1
/CS2	Input	Chip Select 2
/ADS	Input	Address Strobe
MR	Input	Master Reset
DISTR	Input	Data In Strobe
/DISTR	Input	Data In Strobe
DOSTR	Input	Data Out Strobe
/DOSTR	Input	Data Out Strobe
DDIS	Output	Driver Disable
CSOUT	Output	Chip Select Out
SIN	Input	Serial Data Input
RCLK	Input	16x Baud for Receiver
/BAUDOUT	Output	BAUDOUT
SOUT	Output	Serial Data Output
/RTS	Output	Request to Send
/DTR	Output	Data Terminal Ready
/OUT1	Output	Output 1
/OUT2	Output	Output 2
/CTS	Input	Clear To Send
/DSR	Input	Data Set Ready
/DCD	Input	Data Carrier Detect
/RI	Input	Ring Indicator
INTRPT	Output	Interrupt Requests

Stop-Bit Programming

When the UART is programmed for two stop-bits (1.5 in 5-bit mode), the receiver does not check for the second stop-bit. If the first stop-bit is high and the second stop-bit is either high or low, the receiver moves the shift register contents into the

Receiver Buffer Register without posting a framing error. In the majority of applications, this will not cause a problem. However, in cases where a corrupted second stop-bit must be reported as a framing error, the receiver will need modification.

External Crystal Support

This core does not support connection of a crystal directly to the device. The XC4000 and XC5200 families will require a clock input.

Internal Loopback

The internal loopback function (enabled by setting MCR(4)) loops the four lower bits of the Modem Control Register (MCR) to the four upper bits of the Modem Status Register (MSR), however, the Harris 82C50A data sheet is ambiguous as to which MCR bit loops to which MSR bit. The XF8250 Core loops these bits as follows:

MCR(0) (DTR) ----> MSR(5) (DSR)

MCR(1) (RTS) ----> MSR(4) (CTS)

MCR(2) (OUT1) ----> MSR(6) (RI)

MCR(3) (OUT2) ----> MSR(7) (DCD)

If it is discovered that this is incorrect, the design will need modification.

Baud Rate Generator

The Baud Rate Generator differs from the Harris datasheet in the following ways.

Divide by Zero - A divisor value of 0x0000 acts like divide by 65536, where “BAUDOUT” is high for one “XINCLK” period and low for 65535 “XINCLK” periods. The Harris datasheet does not specify what results from a divisor of zero.

Divide by One - A divisor of one is not supported. The “BAUDOUT” signal is always high when a divisor of 0x0001 is used. If only a divisor of one is required, “XINCLK” can be connected directly to “RCLK” and “TXCLK” and the Baud Rate Generator can be removed entirely. If various divisors are required including divide by one, then the Baud Rate Generator will have to be modified.

Other Division - For all divisor values between 0x0002 and 0xffff, the “BAUDOUT” signal is high for one “XINCLK” period and low for N-1 “XINCLK” periods, where N is the divisor value. For divisors of 0x0002 and 0x0003, the “BAUDOUT” signal is identical to the Harris datasheet.

For divisors greater than 0x0003, the Harris BAUDOUT signal is high for two XTAL1 clock periods and low for N-2 XTAL1 clock periods. The duty cycle is not an issue within the XF8250 macro, but external devices that use “BAUDOUT” must consider this.

Verification Methods

Complete functional and timing simulation has been performed on the XF8250 using ViewSim. (Simulation vectors used for verification are provided with the core.) This core has also been used successfully in customer designs. The README.TXT file has a short description of three top level CMD files used to simulate the design. These CMD files call other CMD files (19 in all) and all the CMD files have descriptions and comments as to their purpose.

Recommended Design Experience

Users should be familiar with ViewLogic PROcapture or Office schematic entry and Xilinx design flows. Users should also have experience with microprocessor systems and asynchronous communication controllers.

Ordering Information

The XF8250 Asynchronous Communications Core is provided under license from Memec Design Services for use in Xilinx programmable logic devices and Xilinx HardWire gate arrays. Please contact Memec for pricing and more information.

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Related Information

Harris Semiconductor’s *Microprocessor Products for Commercial and Military Digital Applications*, 1992.

Xilinx Programmable Logic

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