M16450 Universal Asynchronous Receiver/Transmitter

January 12, 1998 | Product Specification

Virtual IP Group, Inc.

1094 E. Duane Ave., Suite 211
Sunnyvale, CA 94086 USA
Phone: +1 408-733-3344
Fax: +1 408-733-9922
E-mail: sales@virtualipgroup.com
URL: www.virtualipgroup.com

Features

- Functionally compatible to NS16450
- Complete asynchronous communication protocol including:
  - 5, 6, 7 or 8 bit data transmission
  - Even/odd or no parity bit generation and detection
  - Start and stop bit generation and detection
  - Line break detection and generation
  - Receiver overrun and framing errors detection
  - Communications rates of upto 56K baud
- Internal programmable baud rate generator
- Buffered transmit and receive registers
- Exception handling using interrupt/polled modes
- Internal diagnostic capabilities with loopback
- Modem handshake capability using CTS, RTS, DSR, DTR, RI and DCD signals
- Complete status reporting capabilities
- Line break generation and detection

Applications

- Serial Communication Port
- Modem Interface port

AllianceCORE™ Facts

Core Specifics		
Device Family	Spartan	XC4000E
CLBs Used	188	188
IOBs Used	34[1]	34[1]
CLKIOBs Used	4	4
System Clock fmax	18.4 MHz	18.4 MHz
Device Features Used	Global Buffers	
Supported Devices/Resources Remaining		
	I/O	**CLBs**
XCS40PQ240-3	155[1]	596
XC4020EHQ240-2	155[1]	596
Provided with Core		
Documentation	Core Design Document Designers application note	
Design File Formats	.ngd, XNF netlist Verilog Source RTL available extra	
Constraint Files	.cst file, xactinit.dat.	
Verification Tool	Test Vectors	
Schematic Symbols	None	
Evaluation Model	None	
Reference designs & application notes	FPGA Design Document	
Additional Items	Evaluation board available extra	
Design Tool Requirements		
Xilinx Core Tools	Alliance 1.3	
Entry/Verification Tool	Verilog RTL/Verilog XL simulator	
Support		
Support provided by Virtual IP Group, Inc.		

Note:
1. Assuming all core signals are routed off chip.

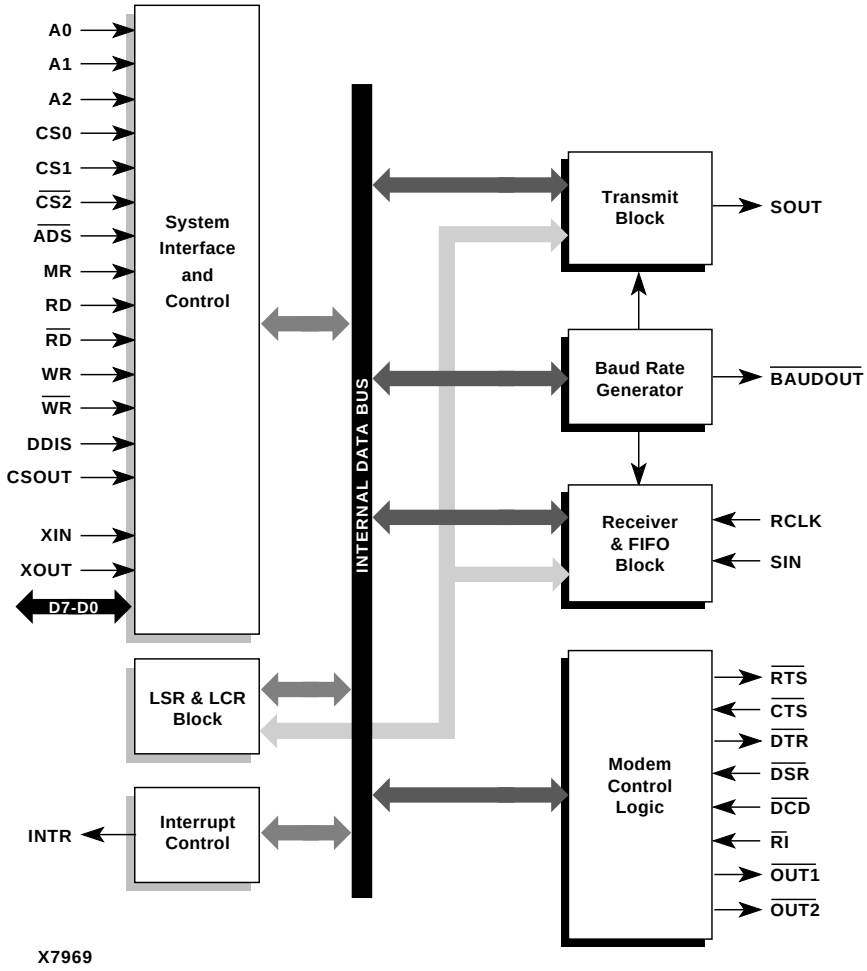

Figure 1: M16450 Block Diagram

General Description

M16C450 interfaces with a microcontroller or microprocessor on one side and serial communications equipment on the other. It provides full modem control through input and output signals for easy handshaking with modems during communication. Internal registers provide full programmability of serial asynchronous communication parameters. This core is functionally compatible to the National Semiconductor NS16450.

Functional Description

The functional Block Diagram is shown in Figure 1. The internal modules are explained below.

System Interface and Control Block

This block supports the Processor interface and generates the internal system level signals for proper functioning.

LSR and LCR Block

This block holds the Line Status and Line Control Registers. These two registers control communication for the core.

Interrupt Control Block

This block handles all interrupt capabilities for the core.

Table 1: Core Signal Pinout

Signal	Signal Direction	Description
System Interface Signals		
A0, A1, A2	Input	Address signals to select an internal register for read/ write operations.
CS0-2	Input	Chip Select. CS0 and CS1 are active high, CS2 is active low.
ADS	Input	Address Strobe. Chip Select and address signals are latched internally on rising edge of $\overline{ADS}$. Pulled low if unused.
MR	Input	Master Reset, active high.
RD	Input	Read Control, active high. Pulled low if unused.
$\overline{RD}$	Input	Read Control, active low. Pulled high if unused.
WR	Input	Write Control, active high. Pulled low if unused.
$\overline{WR}$	Input	Write Control, active low. Pulled high if unused.
DDIS	Output	**D**river **DIS**able signal, driven low, when core outputs data. Used to control data flow direction in transceiver or, tristate buffers enable control.
CSOUT	Output	Indicates read/write selection of UART. Active high and remains high when UART is selected through chip select inputs.
XIN	Input	Master clock input.
XOUT	Input	Master clock output, inverted from XIN.
D7 - D0	In/Out	Bidirectional databus carries data to be written to internal registers; also reports status of registers during read cycle.
Modem Interface Signals		
$\overline{RTS}$	Output	Active low **R**EQUEST **T**O **S**END indicates UART is ready to exchange data. System controls this pin bit in modem control register.
$\overline{CTS}$	Input	Active low **C**LEAR **T**O **S**END indicates modem is ready to exchange data. Present state monitored by reading MSR.
$\overline{DTR}$	Output	Active low **D**ATA **T**ERMINAL **R**EADY tells modem that UART is ready to establish communication link. System controls this pin through bit in MSR.r.
$\overline{DSR}$	Input	Active low **D**ATA **S**ET **R**EADY indicates modem is ready to handshake with core. Present state monitored by reading MSR.
$\overline{DCD}$	Input	Active low **D**ATA **C**ARRIER **D**ETECT indicates modem has detected carrier on communications line. Present state monitored by reading MSR.
$\overline{RI}$	Input	Active low **R**ING **I**NDICATOR indicates modem has detected ring signal. Present state monitored by reading MSR.
OUT1-2	Output	General purpose outputs. System controls these pins by through bit in MSR.
Transmit/Receive Signals		
SOUT	Output	Serial data output from transmitter block.
RCLK	Input	Input receive clock, should be 16 times communications baud rate.
SIN	Input	Serial data input for receiver block.
Other Signals		
INTR	Output	Active high interrupt signal.
BAUDOUT	Output	Baud rate generator output clock. 16 times programmed communication baud rate.

Transmit Block

This block controls serial data transmission as per programmed parameters.

Baud Rate Generator Block

This block generates the Baud Rate Clock for the transmitter section of the core. This clock can also be used by the receiver block connecting $\overline{\text{BAUDOUT}}$ to RCLK.

Receiver Block

This block handles reception for the core. The clock for this block is provided by RCLK. This clock should be 16 times the baud rate.

Modem Control Logic Block

This block handles modem handshaking for the core. These signals can be used for communication or as general purpose signals. The modem control register resides in this block, providing internal diagnostic capability.

Core Modifications

Modifications can be done to remove the internal baud rate generator, or to strip off either transmitter or receiver. These modifications can be performed by Virtual IP Group, Inc. for additional cost.

Pinout

The pinout has not been fixed to a specific FPGA/IO allowing flexibility with the user application. A pinout is suggested for use with a user-constructible evaluation board. Information for this is in the FPGA Design Document included with the core. Signal names are provided in the block diagram shown in Figure 1 and Table 1.

Verification Methods

The core has been tested with in-house developed simulation test vectors that are provided with the core. Assembly level 80x86 programs were used to test the functionality of the FPGA using a hardware evaluation board.

Recommended Design Experience

Knowledge of interface with Microprocessor based systems is required. The user must be familiar with HDL design methodology as well as instantiation of Xilinx netlists in a hierarchical design environment. Usage of Alliance or Foundation tools is required.

Available Support Products

The FPGA Design Document included with the core gives directions of constructing a general purpose FPGA evaluation daughter board that can be plugged in to a standard port socket on the target system through a flat cable.

Ordering Information

This product is available from Virtual IP Group, Inc. Please contact them for pricing and additional information.

Related Information

Refer to Specification Document for programming of this core for a typical application in a system. The user is required to refer to Designer's application note for integrating this core with other cores.

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
Phone: +1 408-559-7778
Fax: +1 408-559-7114
URL: www.xilinx.com

For general Xilinx literature, contact:

Phone: +1 800-231-3386 (inside the US)
+1 408-879-5017 (outside the US)
E-mail: literature@xilinx.com

For AllianceCORE™ specific information, contact:

Phone: +1 408-879-5381
E-mail: alliancecore@xilinx.com
URL: www.xilinx.com/products/logicore/alliance/tblpart.htm