XILINX PROGRAMMER QUALIFICATION SPECIFICATION

XC9500 FAMILY

Introduction

The device programming and verification procedures are similar to those used with standard FLASH EPROM memories. Initially, and after each erasure, all cells in the device are in the logical “1” (FFH) state.

The Xilinx XEPLD software generates device programming files in JEDEC format. The JEDEC file also contains information specific to each device which will be compared to the device being programmed. Each product contains a ROM with a manufacturer’s code to identify Xilinx as the manufacturer.

Features

Erase

The device is electrically erasable. The algorithm has to perform a blank check on the device to ensure all bits are erased before allowing programming.

Addressing

The device is addressed as a byte-wide memory with several significant exceptions. There are several illegal addresses and some bytes in which not all bits can be programmed. The legal device addresses are contained on the included Add.dat floppy disk.

Signature String

The programmer or host computer must support a mode for reading and displaying the four signature string bytes of alphanumeric characters. Programming of these bytes is automatic because the Xilinx software inserts this string into the design file.

Note: In order to correctly interpret the Signature String the “Logical Complement” must be applied for display purposes.

Device Security

The device supports two types of security; one to protect the design from being copied (read secure), and one to protect the device from being erased and/or reprogrammed (write secure).

Special Instructions

Device/ File Checksum Calculation

Contained in each JEDEC file is a fuse checksum (C-Field), which should be used to represent the file checksum. This checksum is the 16-bit sum (i.e. modulo 65,535) of the 8-bit word containing the fuse states of the entire device. Unused bits in the final 8-bit word must be set to zero. The same method must be used to calculate the device checksum and the two should match.

Programming Sequence

The device programming sequence, illustrated in Figure 1, begins by verifying that the device design file and programming algorithm match the installed programmer adapter. This check is accomplished by comparing the programmer adapter ID, first to all acceptable adapter IDs in the programmer algorithm and next to the fuse count and pin count contained in the JEDEC file. If a mismatch occurs, display message **A: "Incompatible Adapter Or File" For Current Algorithm"** and terminate the programming sequence.

Read Manufacturer's Code ID

Verify that the manufacturer's code in the device matches the value listed in the Add.dat file contained on the supplied disk. If the manufacturer's code ID does not match, display the message **B:** "**Manufacturer's Code Error"** and terminate the programming sequence.

Read Product Code ID

Verify that the product code in the device matches the value listed in the Add.dat file contained on the supplied disk. If the product code ID does not match, display the message **C: "Product Code Error"** and terminate the programming sequence.

Device Security Tests

Verify that the device is not secured (see security on page 8. If secured, display the message **D: "Device Secured"** and terminate the programming sequence.

Device Blank Check

Verify that all EPROM cells are in the unprogrammed state. If any one of the EPROM cells is programmed, display the message **E: "Device Not Blank"** and allow the option to erase the device. The device has to be blank prior to programming. If the device fails, display message **F: "Device Failed To Erase"** and terminate the programming sequence.

Device Programming/Verification

At this point the actual programming cycle begins. To minimize the duration of the programming cycle, all EPROM cells are programmed with a short pulse. After programming the full address array, power down the device and perform a margin verify, as illustrated in Figure 5. The programming/margin verify cycle is repeated until all EPROM cells pass. If any one of the cells fails margin testing, a number of retries is permitted. Each time, the full address array is reprogrammed. The number of retries ($N_{MAX)}$ can be calculated using the following equation:

$$N_{MAX} = \frac{2.5\ ms}{t_{PWPGM}}$$

Where t_{PWPGM} is the actual, measured value of the programming pulse width used. If after N_{MAX} attempts, any cell still fails to pass margin test, display the message **G: "Device Failed To Program"** and terminate the programming sequence.

Stand Alone Verify

Once programmed successfully, power the device down then perform a stand alone verify (See figure 6). If the device fails, display message **I: "Device Failed To Verify"** and terminate the programming sequence.

Secure Device

Following the programming sequence, the algorithm should prompt the operator to secure the device, as illustrated in Figure 1. If the user elects not to secure the device, display the message **H: "Device Not Secured"** and terminate the programming sequence. If the user chooses to secure the device, program the security bits (see Figure 4) and display the message **D: "Device Secured"** and terminate the programming sequence. If the device fails to secure, a number of retries is permitted. The number of retries (N_{MAX}) can be calculated using the following equation:

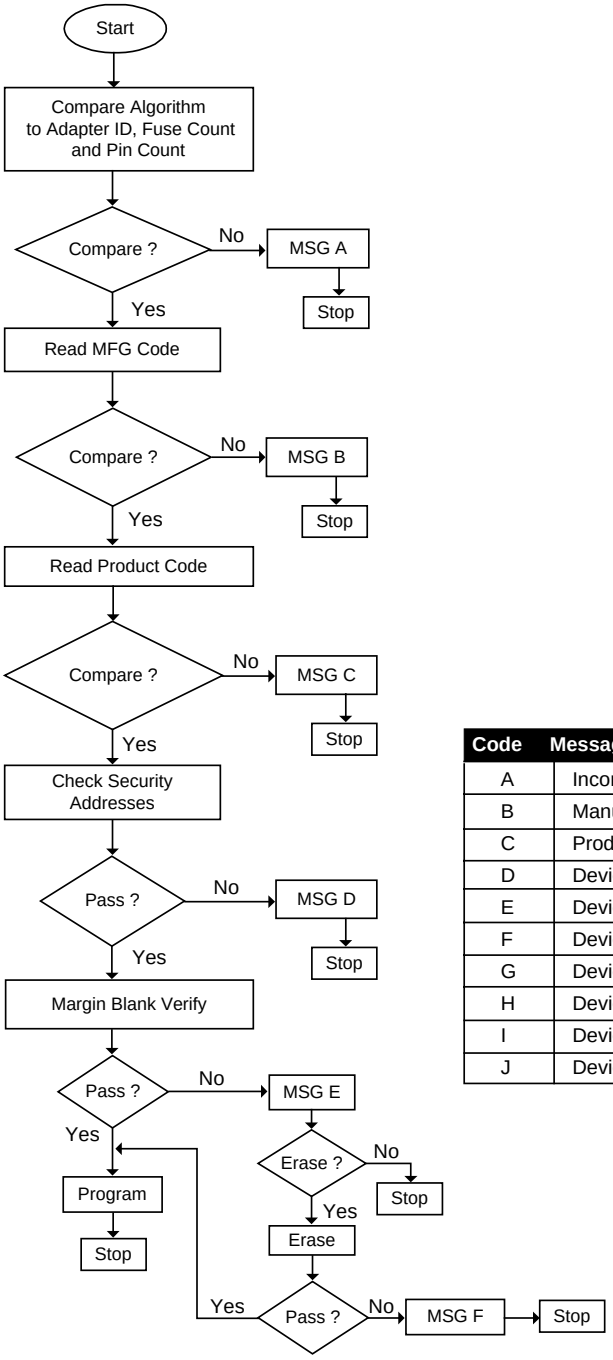
$$N_{MAX} = \frac{2.5\ ms}{t_{PWPGM}}$$

Where t_{PWPGM} is the actual, measured value of the programming pulse width used. If after N_{MAX} attempts, the first address still fails to pass margin test, display the message **J: Device Failed To Secure"** and terminate the programming sequence.

If the user elects to use both Read and Write Secure, the Read Security addresses must be programmed first, followed by the Write Security addresses. Do not power down between programming of the Read and Write Secure addresses or between Program and Verify operations.

Both Program and Verify are performed in the same mode. To Verify without powering down after programming the Security addresses, simply lower V_{PP} from V_{PPPROG} to V_{PPVF1} and wait a minimum of 200µs before reading the first Read and Write Security addresses.

Note: When either Read or Write securing the device, the above methodologies still apply.



Code	Messages
A	Incompatible Adapter or File for Current Algorithm
B	Manufacturer's Code Error
C	Product Code Error
D	Device Secured
E	Device Not Blank
F	Device Failed To Erase
G	Device Failed To Program
H	Device Not Secured
I	Device Failed To Verify
J	Device Failed To Secure

Figure 1. Overall Programming Sequence

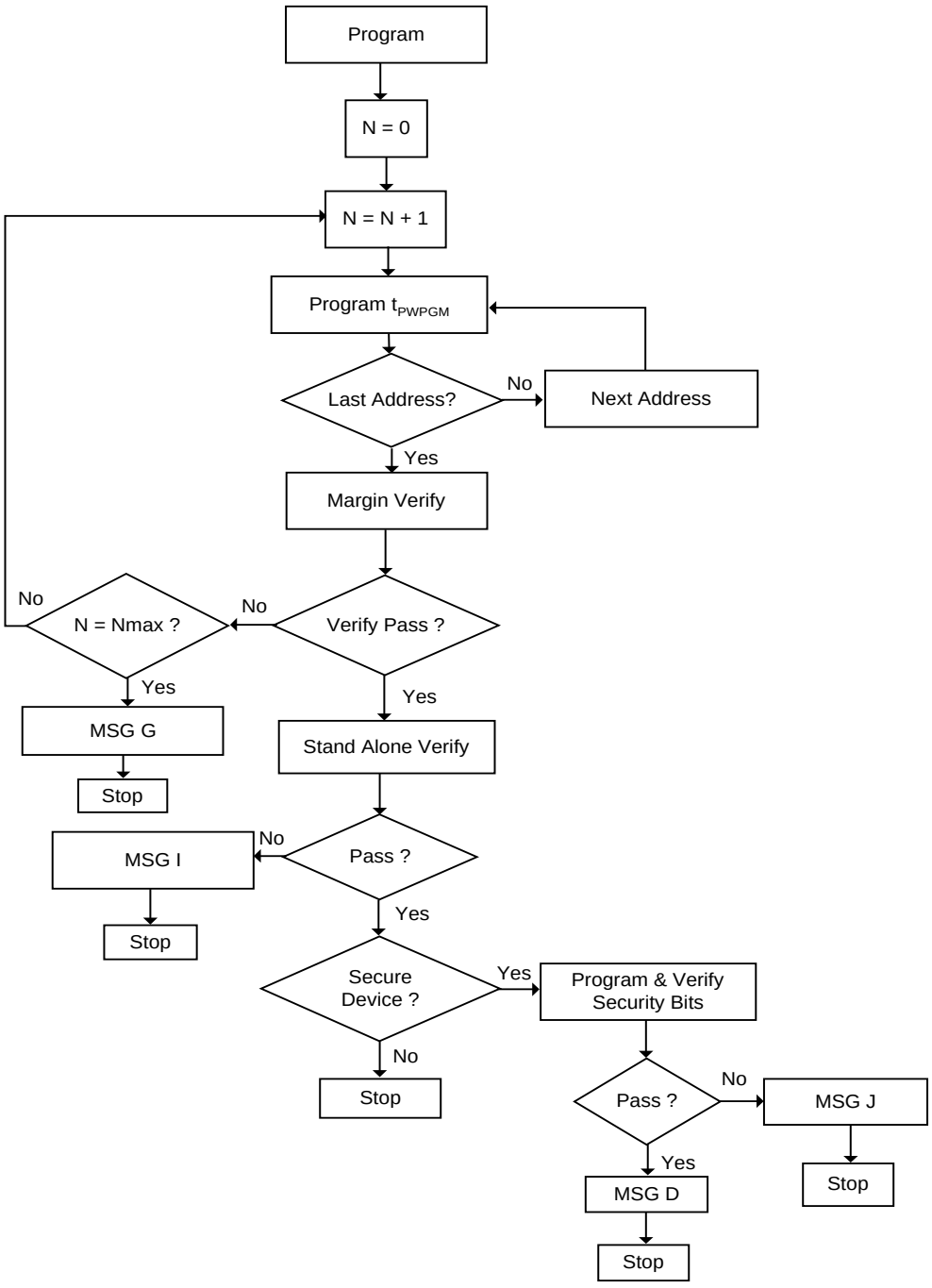


Figure 2. Programming Flow

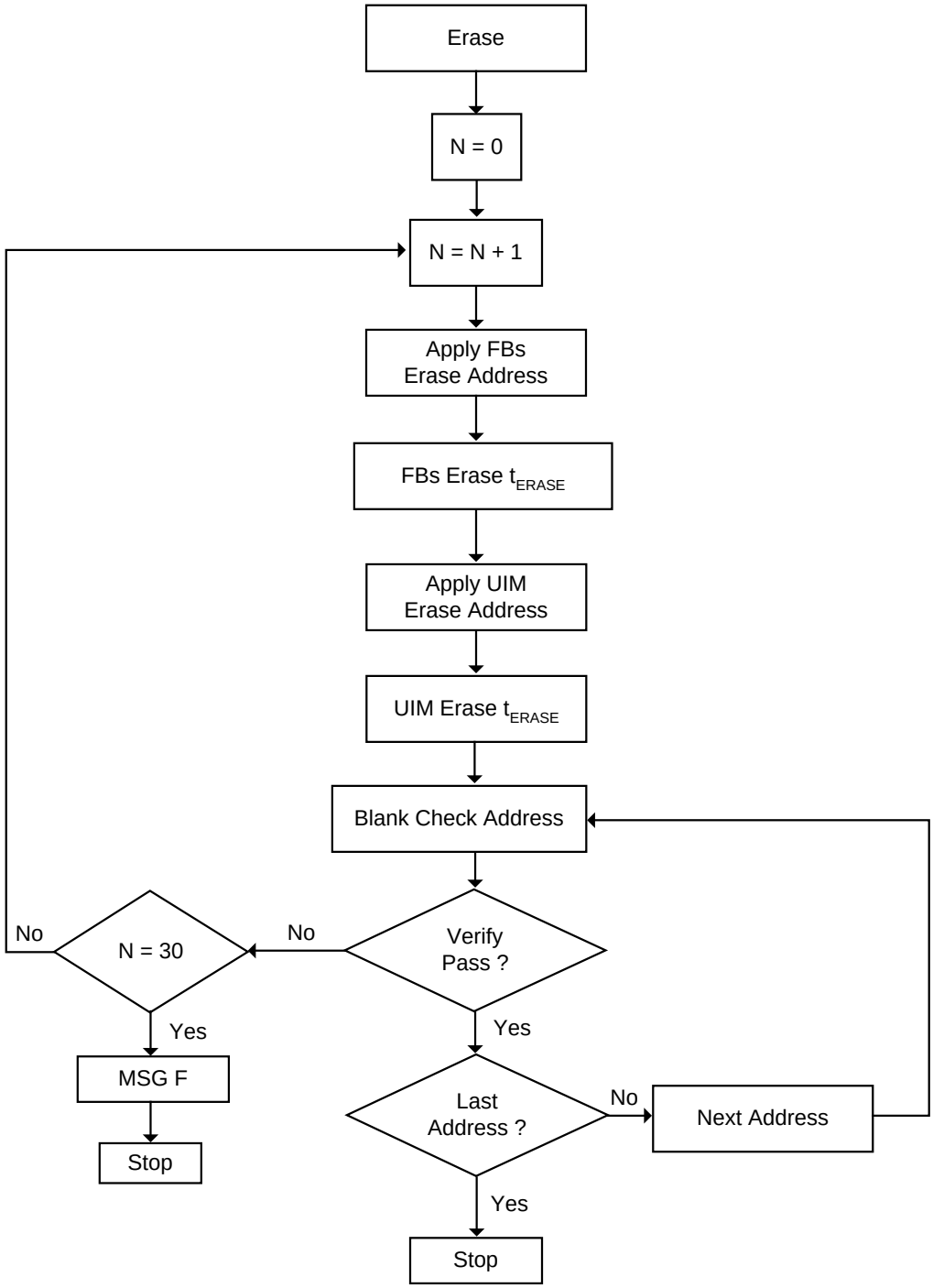


Figure 3. Erase Flow

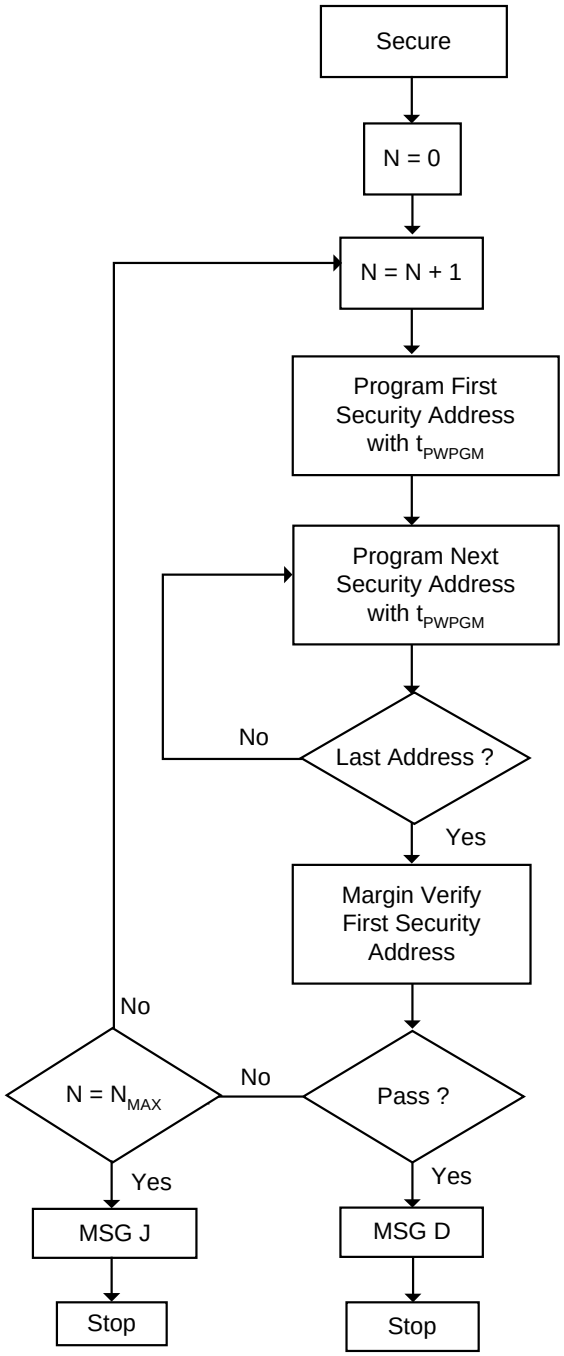


Figure 4. Read/Write Secure Flow

Compatibility Checks

Adapter Type

The adapter should contain an electronically readable code for identification. The programming algorithm must check the adapter ID for compatibility with the target device. The JEDEC design file also contains information specific to the device pin count and fuse size, both of which must be compared to the adapter in use. The pin count, fuse size, and packages for each device are listed in the Add.dat file, supplied on the floppy disk.

Manufacturer's Code/Product Code

Each Xilinx CPLD product contains a readable manufacturer's code which identifies Xilinx as the manufacturer and a product code which identifies the product. The programming algorithm must confirm that both of these codes match the target device. The device address location and data for each of the XC9500 devices is contained in the Add.dat files supplied on floppy disks.

Operating Modes

The device has two operating modes: Program and Erase. Program is used for selectively changing FLASH EPROM cells within the device. Erase is the procedure used to erase the device. All other operations make use of the programming mode. This includes Stand Alone Verify, Blank Check, Load, and reading of the Signature String, Manufacturer's and Product Codes.

Erase

To erase the device, follow the flow in Figure 3 and the timing according to Figure 9. See the Add.dat file for the Function Block (FB) and Universal Interconnect Matrix (UIM) erase addresses. If the device does not erase on the first attempt, a maximum of 30 retries is permitted.

Security

Two security features are available on the device. The algorithm has to offer both as options to the user when programming a device. Two types of security addresses are listed in the Add.dat file.The algorithm also has to check the security addresses before any operation is performed, to assure that only valid operations are performed. (see Tables 1 & 2). Read all the security addresses and if any one bit of any address is programmed, consider the device secured. If both security features are enabled only the signature string, manufacturer's code and product code can be read and no other operations should be permitted.

When securing a device, first program all security addresses for the type of security required, then margin verify only the first security address. If this address fails to verify, reprogram all the security addresses until the first address passes. The amount of retries permitted before failing the device is defined on page 3.

Table 1

Read Secure*

Operation	Valid
Program	No
Erase	Yes
Verify	No
Load	No
Blank Check	No
Signature String	Yes
Mfg/Product Code	Yes

* See Add.dat file for addresses.

Table 2

Write Secure*

Operation	Valid
Program	No
Erase	No
Verify	Yes
Load	Yes
Blank Check	Yes
Signature String	Yes
Mfg/Product Code	Yes

- See Add.dat file for addresses.

Common DC Programming and Erase Characteristics T_A = 25°C ± 5°C

Symbol	Description	Limits		
		Min	Max	Units
I_{IL}	Input Leakage		10	µA
I_{CC}	V_{CC} Supply Current		400	MA
I_{PP}	V_{PP} Supply Current		200	MA
V_{IL}	Low-Level Input Voltage	0	0.8	V
V_{IH}	High-Level Input Voltage	2.0	V_{cc}+0.3	V
V_{OL}	Low-Level Output Voltage		0.5	V
V_{OH}	High-Level Output Voltage	2.4		V
V_{PPTST}	V_{PP} During Test Mode Entry	11.0	11.6	V
V_{PPTST} – 95144	V_{PP} for XC95144, Product Code 25	10.4	10.6	V
V_{CCBNK}	V_{CC} During Blank Verify	4.6	4.8	V
V_{PPNOM}	Nominal V_{PP}	5.15	5.35	V
V_{PPVF1}	Margin Verify	6.9	7.1	V
V_{PPBNK}	V_{PP} During Blank Verify	2.9	3.1	V
V_{PPVF2}	Stand Alone Verify, Secure Verify, Load	6.5	6.7	V

Note: Although min and max limits are given, Xilinx recommends that the mean be used whenever possible.

Specific DC Programming and Erase Characteristics T_A = 25°C ± 5°C

Symbol	Description	Product	Product Code	Limits		
				Min	Max	Units
V_{CCNOM}	Nominal V_{CC}	XC9536	22	5.15	5.35	V
		XC9572	23	5.15	5.35	V
		XC95108	20	5.15	5.35	V
		XC95108	27	5.15	5.35	V
		XC95144	25	5.15	5.35	V
		XC95216	21	4.90	5.10	V
		XC95216	28	5.15	5.35	V
		XC95288	24	5.15	5.35	V
V_{PPERS}	V_{PP} Erase	XC9536	22	12.1	12.4	V
		XC9572	23	12.1	12.4	V
		XC95108	20	12.1	12.4	V
		XC95108	27	11.15	11.35	V
		XC95144	25	10.20	10.40	V
		XC95216	21	10.8	11.2	V
		XC95216	28	11.15	11.35	V
		XC95288	24	11.15	11.35	V
V_{PPPROG}	V_{PP} Program	XC9536	22	10.8	11.2	V
		XC9572	23	10.8	11.2	V
		XC95108	20	10.8	11.2	V
		XC95108	27	11.15	11.35	V
		XC95144	25	10.60	10.80	V
		XC95216	21	10.8	11.2	V
		XC95216	28	11.15	11.35	V
		XC95288	24	11.15	11.35	V

AC Programming Specifications

Symbol	Description	Limits		
		Min	Max	Units
T_{D1}	Delay from V_{CCNOM} to V_{PPNOM}	100		µs
T_{D2}	Delay from V_{CCNOM} to TSTEN	10		µs
T_{PWTST}	Test Mode Enable Pulse Width	200		µs
T_{S1}	V_{PP} Setup Time	100		µs
T_{S2}	VFYEN or PGMEN Setup Time	1		µs
T_{S3}	Test Pin Setup Time	1		µs
T_{S4}	AD_STB Setup Time	0.5		µs
T_{H2}	PGMEN or VFYEN Hold Time	0.5		µs
T_{H3}	Test Pin Hold Time	0.5		µs
T_{H4}	AD_STB Hold Time	0.5		µs
T_{PWSTB}	AD_STB Pulse Width	1		µs
T_{AS}	Address Setup Time	0.5		µs
T_{AH}	Address Hold Time	0.5		µs
T_{PWPGM}*	Program Pulse Width	20	200	µs
T_{VDV}	VFYEN to Data Valid	0.5		µs
T_{ERASE}	Erase Pulse Width	100		ms
T_{VOFF1}	V_{PP} Off Before All Signals	10		µs
T_{VOFF2}	All Signals Off Before V_{CC}	100		µs

*Recommended t_{PWPGM} is 100 µs

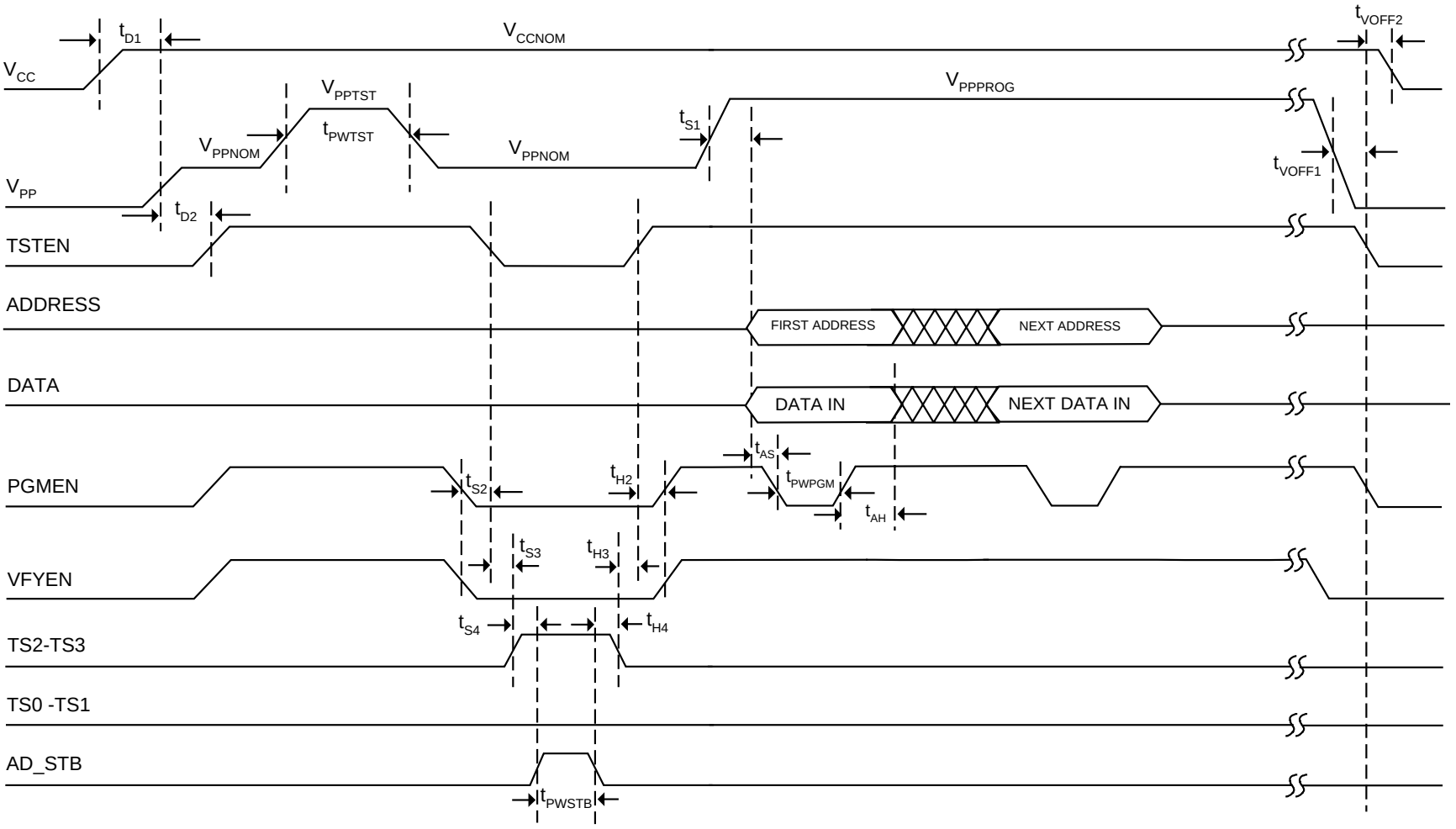
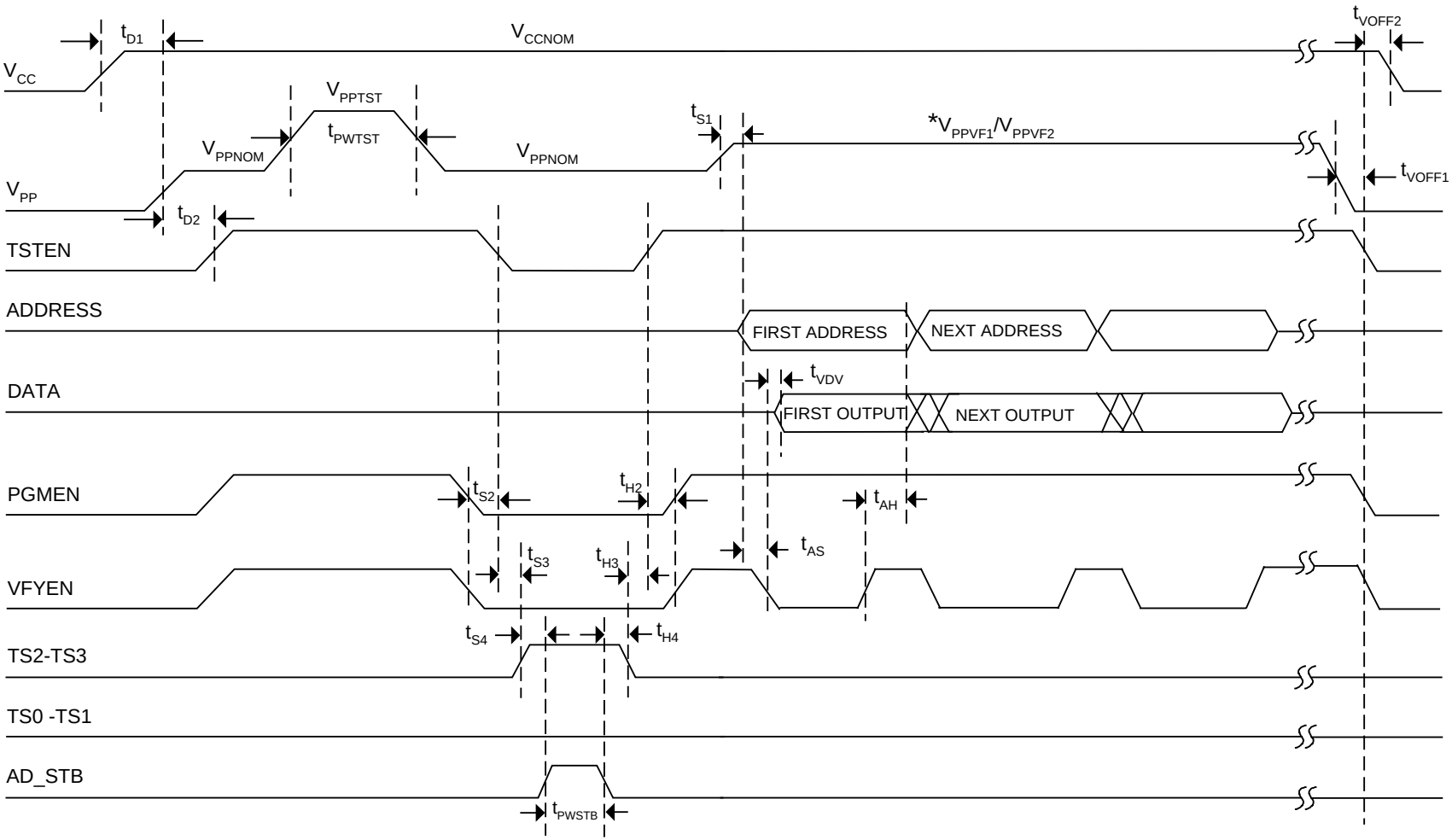


Figure 5. Program



*V_{PPVF1} only used for Margin Verify

Figure 6. Margin Verify, Stand Alone Verify, Secure Verify, and Load

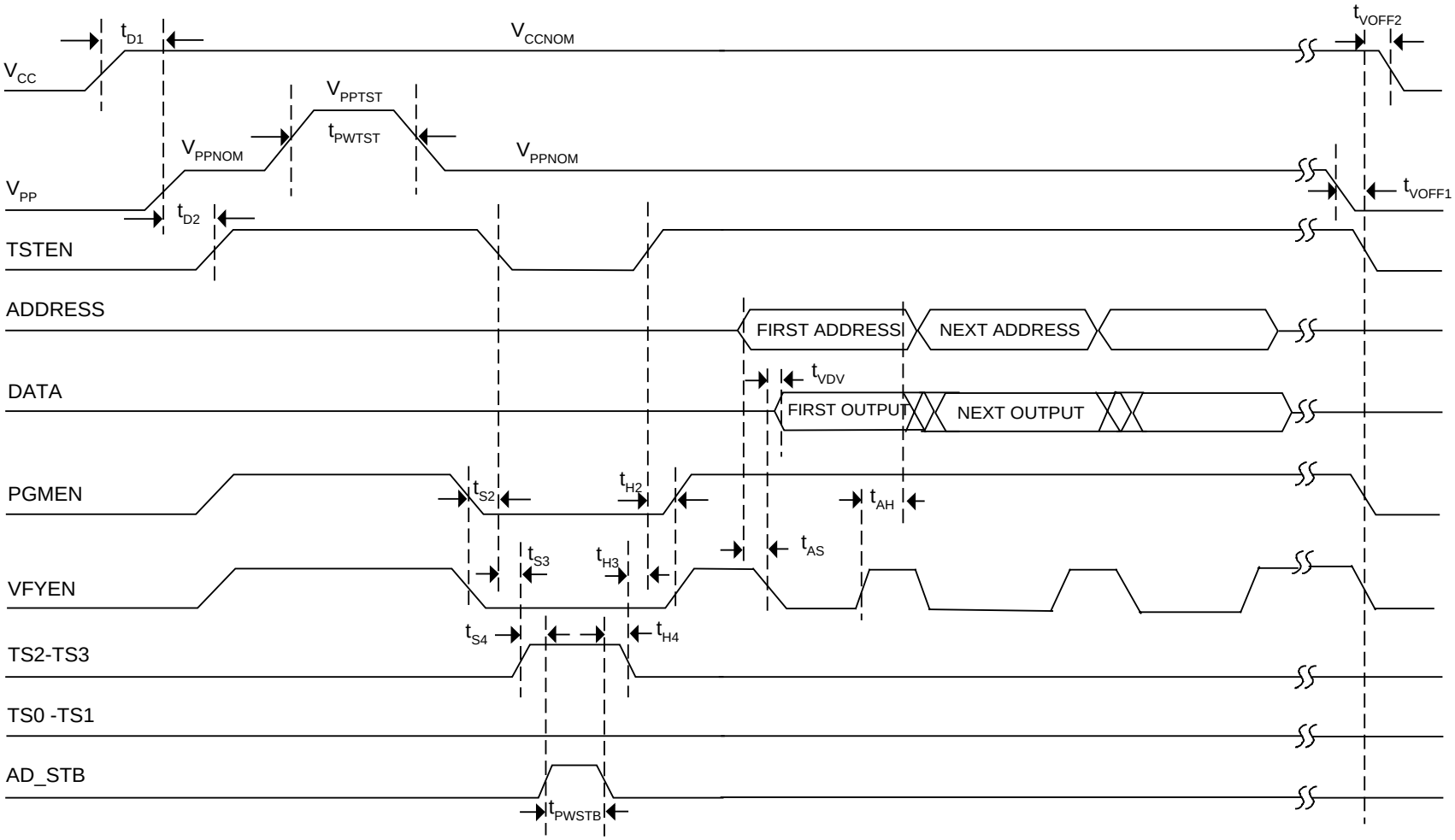


Figure 7. Manufacturer's Code, Product Code, and Signature String

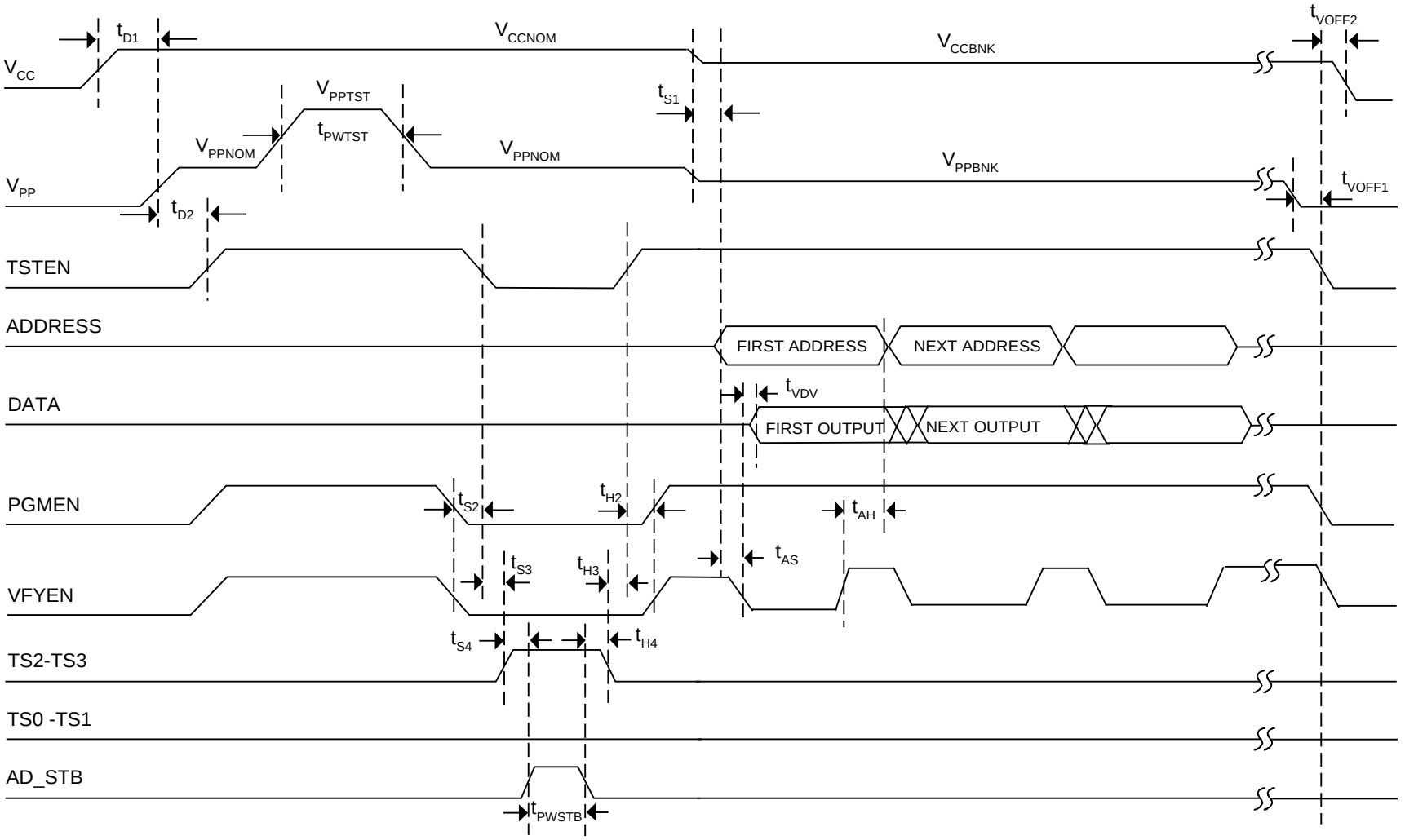


Figure 8. Blank Check

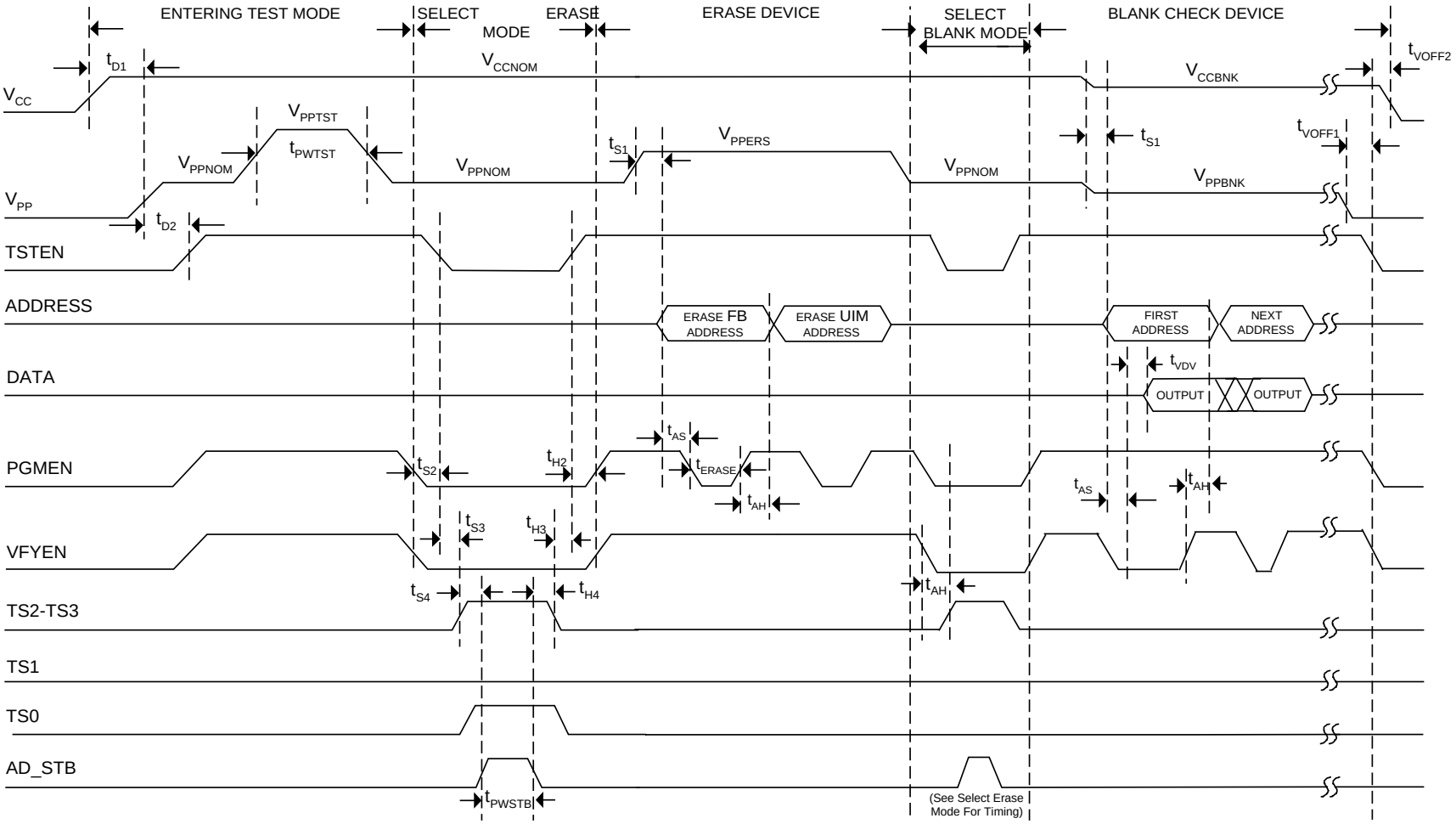


Figure 9. Erase

XC9536/9536F Programming Signal Definitions

Pin Type	44 LCC	44 VQFP
TSTEN	1	39
Ts2	2	40
Ts3	3	41
Ts0	4	42
*	5	43
*	6	44
Ts1	7	1
A8	8	2
A9	9	3
GND	10	4
A10	11	5
A11	12	6
A12	13	7
A13	14	8
D3	15	9
*	16	10
*	17	11
D0	18	12
D1	19	13
D2	20	14
Vcc	21	15
D4	22	16

Pin Type	44 LCC	44 VQFP
GND	23	17
D5	24	18
D6	25	19
D7	26	20
*	27	21
PGMEN	28	22
A0	29	23
A1	30	24
GND	31	25
Vcc	32	26
A2	33	27
A3	34	28
A4	35	29
A5	36	30
A6	37	31
A7	38	32
*	39	33
*	40	34
V_{PP}	41	35
VFYEN	42	36
*	43	37
AD_STB	44	38

NOTE: Pins marked with * must be connected to V_{CC} or GND.

XC9572/9572F Programming Signal Definitions

Pin Type	44 LCC	84 LCC	100 PQFP	100 TQFP
*	.	75	3	1
NC	.	.	4	2
*	.	76	5	3
*	40	77	6	4
V_{PP}	41	78	7	5
*	.	79	8	6
NC	.	.	9	7
A0	42	80	10	8
*	43	81	11	9
A1	44	82	12	10
*	.	83	13	11
*	.	84	14	12
TSTEN	1	1	15	13
*	.	2	16	14
PGMEN	3	3	17	15
A2	2	4	18	16
VFYEN	4	5	19	17
A3	7	6	20	18
NC	.	.	21	19
*	.	7	22	20
GND	.	8	23	21
*	5	9	24	22
*	6	10	25	23
NC	.	.	26	24
*	.	11	27	25
Vcc	.	.	28	26
*	.	12	29	27
A4	14	13	30	28
D0	8	14	31	29
D1	9	15	32	30
GND	10	16	33	31
D2	11	17	34	32
A5	15	18	35	33
NC	.	.	36	34
D3	12	19	37	35
A6	17	20	38	36
D4	13	21	39	37
Vcc	.	22	40	38
*	.	23	41	39

Pin Type	44 LCC	84 LCC	100 PQFP	100 TQFP
*	.	24	42	40
*	.	25	43	41
*	.	26	44	42
NC	.	.	45	43
GND	.	27	46	44
*	.	28	47	45
NC	.	.	48	46
*	16	29	49	47
*	.	30	50	48
A7	24	31	51	49
A8	25	32	52	50
Vcc	.	.	53	51
D5	18	33	54	52
*	.	34	55	53
*	.	35	56	54
D6	19	36	57	55
D7	20	37	58	56
Vcc	21	38	59	57
*	22	39	60	58
*	.	.	61	59
A9	26	40	62	60
A10	27	41	63	61
GND	23	42	64	62
A11	28	43	65	63
*	.	44	66	64
*	.	45	67	65
*	.	46	68	66
*	.	47	69	67
*	.	48	70	68
GND	.	49	71	69
*	.	50	72	70
*	.	51	73	71
*	.	52	74	72
NC	.	.	75	73
*	.	53	76	74
GND	.	.	77	75
*	.	54	78	76
*	.	55	79	77
*	.	56	80	78

Note: Pins marked with *must be connected to V_{CC} or GND
NC = No Connection
Pinout for the 44 pin package is not in numerical order

XC9572/9572F Programming Signal Definitions (Cont.)

Pin Type	44 LCC	84 LCC	100 PQFP	100 TQFP
*	.	.	81	79
NC	.	.	82	80
*	.	57	83	81
*	.	58	84	82
*	.	59	85	83
GND	31	60	86	84
*	.	61	87	85
*	.	62	88	86
*	.	63	89	87
Vcc	32	64	90	88
AD_STB	33	65	91	89
A12	29	66	92	90
A13	30	67	93	91
*	.	.	94	92
A14	34	68	95	93
TS0	35	69	96	94
TS1	36	70	97	95
TS2	37	71	98	96
TS3	38	72	99	97
Vcc	.	73	100	98
*	39	74	1	99
GND	.	.	2	100

Note: Pins marked with *must be connected to V_{CC} or GND
NC = No Connection
Pinout for the 44 pin package is not in numerical order

XC95108/95108F Programming Signal Definitions

Pin Type	84 LCC	100 PQFP	100 TQFP	160 PQFP	Pin Type	84 LCC	100 PQFP	100 TQFP	160 PQFP
V_{CC}	.	.	.	1	Vcc	.	28	26	41
*	75	3	1	2	*	12	29	27	42
NC	.	.	.	3	*	.	.	.	43
*	.	4	2	4	A8	13	30	28	44
NC	.	.	.	5	*	.	.	.	45
*	76	5	3	6	Vcc	.	.	.	46
NC	.	.	.	7	A9	14	31	29	47
*	77	6	4	8	NC	.	.	.	48
*	.	.	.	9	A10	15	32	30	49
V_{PP}	78	7	5	10	*	.	.	.	50
*	79	8	6	11	GND	16	33	31	51
*	.	9	7	12	*	.	.	.	52
VFYEN	80	10	8	13	NC	.	.	.	53
*	.	.	.	14	A11	17	34	32	54
GND	81	11	9	15	NC	.	.	.	55
*	.	.	.	16	A12	18	35	33	56
AD_STB	82	12	10	17	*	.	36	34	57
PGMEN	83	13	11	18	A13	19	37	35	58
*	84	14	12	19	A14	20	38	36	59
GND	.	.	.	20	A15	21	39	37	60
TSTEN	1	15	13	21	Vcc	22	40	38	61
*	2	16	14	22	*	23	41	39	62
TS0	3	17	15	23	*	24	42	40	63
TS1	4	18	16	24	*	25	43	41	64
*	.	.	.	25	NC	.	.	.	65
TS2	5	19	17	26	NC	.	.	.	66
*	.	.	.	27	NC	.	.	.	67
TS3	6	20	18	28	*	26	44	42	68
*	.	21	19	29	*	.	45	43	69
*	7	22	20	30	GND	27	46	44	70
GND	8	23	21	31	GND	28	47	45	71
NC				32	*	.	48	46	72
*	9	24	22	33	GND	29	49	47	73
*	.	.	.	34	*	.	.	.	74
*	10	25	23	35	GND	30	50	48	75
*	.	26	24	36	*	.	.	.	76
*	11	27	25	37	D0	31	51	49	77
NC	.	.	.	38	*	.	.	.	78
NC	.	.	.	39	D1	32	52	50	79
GND	.	.	.	40	GND	.	.	.	80

Note: Pins marked with *must be connected to V_{CC} or GND

NC = No Connection

XC95108/95108F Programming Signal Definitions (Cont.)

Pin Type	84 LCC	100 PQFP	100 TQFP	160 PQFP
Vcc	.	53	51	81
D2	33	54	52	82
NC	.	.	.	83
*	.	.	.	84
NC	.	.	.	85
*	34	55	53	86
*	.	.	.	87
*	35	56	54	88
*	.	.	.	89
D3	36	57	55	90
*	.	.	.	91
D4	37	58	56	92
NC	.	.	.	93
Vcc	38	59	57	94
D5	39	60	58	95
*	.	61	59	96
D6	40	62	60	97
D7	41	63	61	98
GND	.	.	.	99
GND	42	64	62	100
*	43	65	63	101
*	44	66	64	102
*	45	67	65	103
*	46	68	66	104
*	.	.	.	105
*	47	69	67	106
*	.	.	.	107
*	48	70	68	108
NC	.	.	.	109
GND	49	71	69	110
*	50	72	70	111
*	.	.	.	112
*	51	73	71	113
*	.	.	.	114
*	52	74	72	115
*	.	75	73	116
*	53	76	74	117
NC	.	.	.	118
NC	.	.	.	119
GND	.	77	75	120

Pin Type	84 LCC	100 PQFP	100 TQFP	160 PQFP
Vcc	.	.	.	121
*	54	78	76	122
*	.	.	.	123
*	55	79	77	124
NC				125
*	56	80	78	126
GND	.	.	.	127
*	.	.	.	128
*	.	81	79	129
NC	.	.	.	130
NC	.	.	.	131
NC	.	.	.	132
*	.	82	80	133
*	57	83	81	134
*	58	84	82	135
GND	59	85	83	136
GND	60	86	84	137
*	61	87	85	138
*	62	88	86	139
*	63	89	87	140
Vcc	64	90	88	141
A0	65	91	89	142
A1	66	92	90	143
A2	67	93	91	144
*	.	94	92	145
A3	68	95	93	146
*	.	.	.	147
A4	69	96	94	148
NC	.	.	.	149
NC	.	.	.	150
NC	.	.	.	151
A5	70	97	95	152
*	.	.	.	153
A6	71	98	96	154
*	.	.	.	155
A7	72	99	97	156
Vcc	73	100	98	157
*	.	.	.	158
*	74	1	99	159
GND	.	2	100	160

NOTE: Pins marked with * must be connected to V_{CC} or GND

NC = No Connection

XC95144 Programming Signal Definitions

Pin Type	160 PQFP	100 PQFP	100 TQFP
Vcc	1	.	.
*	2	3	1
*	3	.	.
*	4	4	2
*	5	.	.
*	6	5	3
*	7	.	.
*	8	6	4
*	9	.	.
Vpp	10	7	5
*	11	8	6
*	12	9	7
VFYEN	13	10	8
*	14	.	.
*	15	11	9
*	16	.	.
ADSTB	17	12	10
PGMEN	18	13	11
*	19	14	12
GND	20	.	.
TSTEN	21	15	13
*	22	16	14
TS0	23	17	15
TS1	24	18	16
*	25	.	.
TS2	26	19	17
*	27	.	.
TS3	28	20	18
*	29	21	19
*	30	22	20
GND	31	23	21
*	32	.	.
*	33	24	22
*	34	.	.
*	35	25	23
*	36	26	24
*	37	27	25
*	38	.	.
*	39	.	.
GND	40	.	.

Pin Type	160 PQFP	100 PQFP	100 TQFP
Vcc	41	28	26
*	42	29	27
*	43	.	.
A8	44	30	28
*	45	.	.
Vcc	46	.	.
A9	47	31	29
*	48	.	.
A10	49	32	30
*	50	.	.
GND	51	33	31
*	52	.	.
*	53	.	.
A11	54	34	32
*	55	.	.
A12	56	35	33
*	57	36	34
A13	58	37	35
A14	59	38	36
A15	60	39	37
Vcc	61	40	38
*	62	41	39
*	63	42	40
*	64	43	41
*	65	.	.
*	66	.	.
*	67	.	.
*	68	44	42
*	69	45	43
GND	70	46	44
TDI #	71	47	45
*	72	48	46
TMS #	73	49	47
*	74	.	.
TCK #	75	50	48
*	76	.	.
D0	77	51	49
*	78	.	.
D1	79	52	50
GND	80	.	.

NOTE: Pins marked with * must be connected to Vcc or GND.
Pins marked with # are JTAG pins and must be connected to Vcc or GND when not used.

XC95144 Programming Signal Definitions (continued)

Pin Type	160 PQFP	100 PQFP	100 TQFP
Vcc	81	53	51
D2	82	54	52
*	83	.	.
*	84	.	.
*	85	.	.
*	86	55	53
*	87	.	.
*	88	56	54
*	89	.	.
D3	90	57	55
*	91	.	.
D4	92	58	56
*	93	.	.
Vcc	94	59	57
D5	95	60	58
*	96	61	59
D6	97	62	60
D7	98	63	61
GND	99	.	.
GND	100	64	62
*	101	65	63
*	102	66	64
*	103	67	65
*	104	68	66
*	105	.	.
*	106	69	67
*	107	.	.
*	108	70	68
*	109	.	.
GND	110	71	69
*	111	72	70
*	112	.	.
*	113	73	71
*	114	.	.
*	115	74	72
*	116	75	73
*	117	76	74
*	118	.	.
*	119	.	.
GND	120	77	75

Pin Type	160 PQFP	100 PQFP	100 TQFP
Vcc	121	.	.
*	122	78	76
*	123	.	.
*	124	79	77
*	125	.	.
*	126	80	78
GND	127	.	.
*	128	.	.
*	129	81	79
*	130	.	.
*	131	.	.
*	132	.	.
*	133	82	80
*	134	83	81
*	135	84	82
TDO #	136	85	83
GND	137	86	84
*	138	87	85
*	139	88	86
*	140	89	87
Vcc	141	90	88
A0	142	91	89
A1	143	92	90
A2	144	93	91
*	145	94	92
A3	146	95	93
*	147	.	.
A4	148	96	94
*	149	.	.
*	150	.	.
*	151	.	.
A5	152	97	95
*	153	.	.
A6	154	98	96
*	155	.	.
A7	156	99	97
Vcc	157	100	98
*	158	.	.
*	159	1	99
GND	160	2	100

NOTE: Pins marked with * must be connected to Vcc or GND.
Pins marked with # are JTAG pins and must be connected to Vcc or GND when not used.

XC95216 Programming Signal Definitions

Pin Type	160 PQFP	208 HQPF	352 BGA
Vcc	1	1	P
GND	.	2	G
*	2	3	E23
*	3	4	C26
*	4	5	E24
*	5	6	F24
*	6	7	E25
*	7	8	G24
*	8	9	F26
*	9	10	H23
Vpp	10	11	H24
*	.	12	G26
GND	.	13	G
*	.	14	H25
*	11	15	K23
*	12	16	K24
VFYEN	13	17	J25
*	14	18	L24
*	15	19	K25
*	16	20	L26
ADSTB	17	21	M24
PGMEN	18	22	M25
*	19	23	M26
GND	20	24	G
TSTEN	21	25	N25
Vcc	.	26	P
GND	.	27	G
*	.	28	N26
*	.	29	P25
*	22	30	P23
TS0	23	31	P24
TS1	24	32	R26
*	25	33	R24
TS2	26	34	T26
*	27	35	T25
TS3	28	36	T23
*	29	37	V26
*	30	38	U24
*	.	39	U23
*	.	40	Y26

Pin Type	160 PQFP	208 HQPF	352 BGA
*	.	41	W25
GND	31	42	G
*	32	43	AA26
*	33	44	Y24
*	34	45	AB25
*	35	46	AA24
*	36	47	Y23
*	.	48	AC26
*	37	49	AA23
*	38	50	AB24
*	39	51	AD25
GND	40	52	G
Vcc	41	53	P
*	.	54	AE24
*	42	55	AD23
*	43	56	AF24
A8	44	57	AE23
*	45	58	AE22
Vcc	46	59	P
A9	47	60	AE21
*	48	61	AF21
*	.	62	AC19
A10	49	63	AD19
*	50	64	AE20
Vcc	.	65	P
GND	.	66	G
*	.	67	AD18
GND	51	68	G
GND	.	69	G
*	52	70	AF18
*	53	71	AE17
A11	54	72	AE16
*	55	73	AF16
A12	56	74	AE14
*	57	75	AF14
A13	58	76	AE13
A14	59	77	AC13
A15	60	78	AD13
Vcc	61	79	P
*	.	80	AE12

NOTE: Pins marked with * must be connected to Vcc or GND.

XC95216 Programming Signal Definitions

Pin Type	160 PQFP	208 HQPF	352 BGA
GND	.	81	G
A16	62	82	AD12
*	63	83	AC12
*	64	84	AF11
*	65	85	AE11
*	66	86	AE9
*	67	87	AD9
*	68	88	AC10
*	69	89	AF7
*	.	90	AE8
*	.	91	AD8
Vcc	.	92	P
GND	70	93	G
*	71	94	AF6
*	72	95	AD7
*	73	96	AE6
*	74	97	AE5
*	75	98	AD6
*	76	99	AC7
D0	77	100	AE3
*	.	101	AD4
*	78	102	AC5
D1	79	103	AD3
GND	80	104	G
Vcc	81	105	P
*	.	106	AD2
*	.	107	AC3
GND	.	108	G
*	.	109	AD1
D2	82	110	AA4
*	83	111	AB2
*	84	112	AC1
*	85	113	AA2
*	86	114	AA1
*	87	115	Y1
*	88	116	V4
*	89	117	V3
D3	90	118	W2
*	.	119	U4
*	.	120	U3

Pin Type	160 PQFP	208 HQPF	352 BGA
*	91	121	V2
D4	92	122	U2
*	93	123	T2
Vcc	94	124	P
D5	95	125	R4
*	96	126	R3
D6	97	127	R2
D7	98	128	R1
GND	99	129	G
GND	100	130	G
*	101	131	P1
Vcc	.	132	P
*	102	133	N2
*	103	134	N4
*	104	135	N3
*	105	136	M1
*	106	137	M3
*	107	138	M4
*	108	139	L1
*	109	140	L2
GND	110	141	G
*	.	142	L3
*	.	143	J1
*	.	144	K3
*	111	145	G1
*	112	146	H2
*	113	147	H3
*	114	148	J4
*	115	149	G2
*	116	150	G3
*	.	151	F2
*	117	152	E2
Vcc	.	153	P
*	118	154	D2
*	119	155	F4
GND	120	156	G
Vcc	121	157	P
*	122	158	B3
*	123	159	A3
*	124	160	D6

NOTE: Pins marked with * must be connected to Vcc or GND.

XC95216 Programming Signal Definitions

Pin Type	160 PQFP	208 HQPF	352 BGA
*	125	161	C6
*	126	162	B5
GND	127	163	G
*	128	164	B6
*	.	165	A6
*	129	166	D8
*	130	167	B7
*	.	168	A7
*	.	169	D9
*	131	170	C10
*	132	171	B9
Vcc	.	172	P
*	133	173	A9
*	134	174	D11
*	135	175	B11
*	136	176	D12
GND	137	177	G
*	138	178	C12
*	139	179	B12
*	140	180	A12
Vcc	141	181	P
A0	142	182	A13
*	.	183	B14
Vcc	.	184	P
A1	143	185	C14
A2	144	186	A15
*	145	187	B15
A3	146	188	C15
*	.	189	D15
GND	.	190	G
*	147	191	A16
A4	148	192	C16
*	149	193	C17
*	150	194	B18
*	.	195	A20
*	.	196	B19
*	151	197	C19
A5	152	198	D18
*	153	199	A21
A6	154	200	B20

Pin Type	160 PQFP	208 HQPF	352 BGA
*	155	201	C20
A7	156	202	B22
*	.	203	D20
Vcc	157	204	P
*	158	205	B24
*	159	206	C23
GND	160	207	G
*	.	208	D22

NOTE: Pins marked with * must be connected to Vcc or GND.

XC95216 Power, Ground and No Connect Pins for 352 BGA

Power Pins	Ground Pins	No Connect	No Connect	No Connect
A10	A1	A4	E4	AC4
A17	A2	A11	F1	AC6
B2	A5	A18	F3	AC11
B25	A8	A23	F23	AC15
C22	A14	A24	F25	AC16
D7	A19	B4	G25	AC18
D13	A22	B8	J2	AC21
D19	A25	B10	J3	AC22
G4	A26	B13	J23	AC23
G23	B1	B16	J24	AC24
H4	B26	B17	J26	AC25
K1	C7	B21	K2	AD5
K26	E1	B23	K4	AD10
N23	E26	C1	L4	AD11
P4	H1	C2	L23	AD14
T1	H26	C3	L25	AD15
U1	N1	C4	M2	AD16
U26	P3	C5	M23	AD17
W23	P26	C8	N24	AD20
Y4	V23	C9	P2	AD21
AC8	W1	C11	R23	AD22
AC14	W26	C13	R25	AD24
AC20	AB1	C18	W3	AD26
AE25	AB4	C21	W4	AE2
AF10	AB26	C24	W24	AE4
AF17	AC9	C25	U25	AE7
AF23	AC17	D1	V1	AE10
	AE1	D3	V24	AE15
	AE26	D4	V25	AE18
	AF1	D5	W3	AE19
	AF2	D10	W4	AF3
	AF5	D14	W24	AF4
	AF8	D16	Y2	AF9
	AF13	D17	Y3	AF12
	AF19	D21	Y25	AF15
	AF20	D23	AA3	
	AF22	D24	AA25	
	AF25	D25	AB3	
	AF26	D26	AB23	
		E3	AC2	

XC95288 Programming Signal Definitions

Pin Type	208 HQPF	352 BGA
Vcc	1	P
GND	2	G
*	3	E23
*	4	C26
*	5	E24
*	6	F24
*	7	E25
*	.	D26
*	8	G24
*	.	F25
*	9	F26
*	10	H23
Vpp	11	H24
*	12	G26
GND	13	G
*	14	H25
Vcc	.	P
*	15	K23
*	16	K24
VFYEN	17	J25
*	18	L24
*	19	K25
*	.	L25
*	20	L26
*	.	M23
ADSTB	21	M24
PGMEN	22	M25
*	23	M26
GND	24	G
TSTEN	25	N25
Vcc	26	P
GND	27	G
*	28	N26
*	29	P25
*	30	P23
TS0	31	P24
TS1	32	R26
*	.	R25
*	33	R24
*	.	R23

Pin Type	208 HQPF	352 BGA
TS2	34	T26
*	35	T25
TS3	36	T23
*	37	V26
*	38	U24
*	39	U23
*	40	Y26
*	41	W25
GND	42	G
*	43	AA26
*	.	Y25
*	44	Y24
*	.	AA25
*	45	AB25
*	46	AA24
*	47	Y23
*	48	AC26
*	49	AA23
*	50	AB24
*	51	AD25
GND	52	G
Vcc	53	P
*	54	AE24
*	55	AD23
*	.	AC22
*	56	AF24
*	.	AD22
A8	57	AE23
*	58	AE22
Vcc	59	P
A9	60	AE21
*	61	AF21
*	62	AC19
A10	63	AD19
*	64	AE20
Vcc	65	P
*	66	AC18
*	67	AD18
*	.	AE19
GND	68	G

Pin Type	208 HQPF	352 BGA
*	69	AD17
*	.	AE18
*	70	AF18
*	71	AE17
A11	72	AE16
*	73	AF16
A12	74	AE14
*	75	AF14
A13	76	AE13
A14	77	AC13
A15	78	AD13
Vcc	79	P
*	.	AF12
*	80	AE12
GND	81	G
A16	82	AD12
*	83	AC12
*	84	AF11
*	85	AE11
*	86	AE9
*	87	AD9
*	88	AC10
*	89	AF7
*	90	AE8
*	91	AD8
Vcc	92	P
GND	93	G
*	94	AF6
*	.	AE7
*	95	AD7
*	96	AE6
*	97	AE5
*	98	AD6
*	99	AC7
D0	100	AE3
*	101	AD4
*	102	AC5
D1	103	AD3
GND	104	G
Vcc	105	P

NOTE: Pins marked with * must be connected to Vcc or GND.

XC95288 Programming Signal Definitions

Pin Type	208 HQPF	352 BGA
*	106	AD2
*	107	AC3
GND	108	G
*	109	AD1
D2	110	AA4
*	.	AA3
*	111	AB2
*	112	AC1
*	113	AA2
*	114	AA1
*	115	Y1
*	116	V4
*	117	V3
D3	118	W2
*	119	U4
*	120	U3
*	121	V2
*	.	V1
D4	122	U2
*	123	T2
Vcc	124	P
D5	125	R4
*	126	R3
D6	127	R2
D7	128	R1
GND	129	G
GND	130	G
*	131	P1
Vcc	132	P
*	133	N2
*	134	N4
*	135	N3
*	136	M1
*	.	M2
*	137	M3
*	138	M4
*	139	L1
*	140	L2
GND	141	G
*	142	L3

Pin Type	208 HQPF	352 BGA
*	143	J1
*	144	K3
*	145	G1
*	146	H2
*	147	H3
*	148	J4
*	.	F1
*	149	G2
*	150	G3
*	151	F2
*	152	E2
Vcc	153	P
*	154	D2
*	155	F4
GND	156	G
Vcc	157	P
*	158	B3
*	159	A3
*	160	D6
*	161	C6
*	162	B5
*	.	A4
GND	163	G
*	164	B6
*	165	A6
*	166	D8
*	167	B7
*	168	A7
*	169	D9
*	170	C10
*	171	B9
Vcc	172	P
*	173	A9
*	174	D11
*	175	B11
*	.	A11
*	176	D12
GND	177	G
*	178	C12
*	179	B12

Pin Type	208 HQPF	352 BGA
*	180	A12
Vcc	181	P
A0	182	A13
*	183	B14
Vcc	184	P
A1	185	C14
A2	186	A15
*	187	B15
A3	188	C15
*	189	D15
GND	190	G
*	191	A16
*	.	B16
A4	192	C16
*	.	B17
*	193	C17
*	194	B18
*	195	A20
*	196	B19
*	197	C19
A5	198	D18
*	199	A21
A6	200	B20
*	201	C20
*	.	B21
A7	202	B22
*	.	C21
*	203	D20
Vcc	204	P
*	205	B24
*	206	C23
GND	207	G
*	208	D22

NOTE: Pins marked with * must be connected to Vcc or GND.

XC95288 Power, Ground and No Connect Pins for 352 BGA

Power Pins	Ground Pins	Ground Pins	No Connect	No Connect
A10	A1	AF2	A18	V25
A17	A2	AF5	A23	W3
B2	A5	AF8	A24	W24
B13	A8	AF13	B4	Y2
B25	A14	AF19	B8	AB3
C22	A19	AF22	B10	AB23
D5	A22	AF25	B23	AC2
D7	A25	AF26	C1	AC4
D10	A26		C2	AC6
D13	B1		C3	AC11
D17	B26		C4	AC16
D19	C7		C5	AC17
G4	C9		C8	AC21
G23	C13		C11	AC23
H4	C18		C24	AC24
J3	D24		C25	AC25
J23	E1		D1	AD16
K1	E26		D3	AD21
K26	H1		D4	AD24
N23	H26		D14	AD26
P4	K4		D16	AE2
T1	N1		D21	AE4
U1	N24		D23	AE10
U26	P3		D25	AE15
V24	P26		E3	AF3
W23	V23		E4	AF4
Y3	W1		F3	AF9
Y4	W4		F23	AF20
AC8	W26		G25	
AC14	AB1		J2	
AC15	AB4		J24	
AC20	AB26		J26	
AD5	AC9		K2	
AD11	AD10		L4	
AE25	AD14		L23	
AF10	AD15		P2	
AF15	AD20		T3	
AF17	AE1		T4	
AF23	AE26		T24	
	AF1		U25	