XILINX®

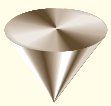
ONLINE

XEPLD
REFERENCE GUIDE

FOR WINDOWS

TABLE OF CONTENTS

INDEX



GO TO OTHER BOOKS

XACT™ STEP

0401306

XEPLD Reference Guide

Design Flow

Using the Design Manager

Controlling Design Implementation

Controlling Design Timing

Timing Analysis

Preface

About This Manual

This manual describes the Xilinx XEPLD programs used for implementing logic designs into Xilinx EPLD devices. The Xilinx Design Manager, a graphical user interface for XEPLD, is also described along with various other software tools used for processing and verifying your designs

This manual explains:

- How to bring up the system and use each menu command.
- How to import designs created with behavioral, schematic, and VHDL front-end tools.
- How to select and use various tools for implementation control, multi-chip partitioning, and timing analysis.
- How to control design implementation from within your logic design source files.
- How to manage your design files.
- How to verify your design timing.

Manual Contents

This manual includes the following chapters:

- Chapter 1, “Design Flow,” gives an overview of design translation, with diagrams, procedures, and a quick tutorial.

- Chapter 2, “Using the Design Manager”, describes the Design Manager screen appearance, commands, and data structure.
- Chapter 3, “Controlling Design Implementation”, explains how to choose a device, assign logic to specific macrocells, assign signals to specific pins, reserve resources, and optimize for speed or density.
- Chapter 4, “Controlling Design Timing”, describes how to include timing specifications in your design file.
- Chapter 5, “Timing Analysis”, shows how to view and interpret static timing information generated by the device fitting process.

Other Reference Material

Other Xilinx publications you can consult for related information:

- *XEPLD Schematic Design Guide.*
- *EZTag User Guide*
- *Libraries Guide.*

Conventions

The following conventions are used in syntactical statements:

`Courier font regular`	System messages or program files appear in regular Courier font.
`Courier font bold`	Literal commands that you must enter in syntax statements are in bold Courier font.
italic font	Variables that you replace in syntax statements are in italic font.
`[ ]`	Square brackets denote optional items or parameters. However, in bus specifications, such as bus [7:0], they are required.
`{ }`	Braces enclose a list of items from which you must choose one or more.
. . .	A vertical ellipsis indicates material that has been omitted.
. . .	A horizontal ellipsis indicates that the preceding can be repeated one or more times.
|	A vertical bar separates items in a list of choices.
↵	This symbol denotes a carriage return.

Contents

About This Manual i
Manual Contents i
Other Reference Material ii
Conventions

Chapter 1 Design Flow

Overview of Design Processing 1-1
Design Entry 1-1
Project Creation 1-2
Design Translation 1-3
Design Implementation and Device Programming 1-4
Report Generation 1-4
Timing Analysis 1-5
Quick Tutorial 1-6
Enter the Design 1-6
Create a New Project 1-7
Implement the Design 1-12
Use the Report Browser 1-13
Use the Timing Analyzer 1-14

Chapter 2 Using The Design Manager

Design Manager Fundamentals 2-1
Managing Projects 2-2
Managing Design Versions 2-2
Managing Device Implementations 2-3
Managing Implementation Revisions 2-3
Design Management Procedure 2-3
The Initial Design Manager Window 2-5
File Menu 2-6
File — New Project 2-6
File — Open Project 2-10
File — Save Project 2-11
File — Close Project 2-11
File — Delete Project 2-11

File — File name 2-12
File — Exit 2-12
Design Menu 2-12
Design — Translate 2-13
Design — Implement 2-14
Design — Export 2-17
Design — New Device 2-18
Design — New Revision 2-19
Design — Copy Revision 2-19
Design — Browse Revision 2-20
Design — Rename 2-23
Design — Delete Revision 2-23
Tools Menu 2-24
Tools — Flow Engine 2-24
Tools — Timing Analyzer 2-24
Tools — EZTag Programmer 2-25
Utilities Menu 2-25
Utilities — Report Browser 2-25
Utilities — Command History 2-26
Utilities — Project Notes 2-27
Utilities — Template Manager 2-27
Help Menu 2-33
Help — Contents 2-34
Help — Search 2-35
Help — Tutorial 2-35
Help — About Design Manager 2-35
Setting Up The Process Flow 2-37
Using a Constraints File (to Define T-Specs) 2-37
Using a Guide File (to Re-Use Pinouts) 2-37
Flow Engine Menu Commands 2-37
Flow Engine — Flow 2-37
Flow Engine — Setup 2-38
Flow Engine — Utilities 2-42
Flow Engine — Help 2-42

Chapter 3 Controlling Design Implementation

Design Implementation Overview 3-1
Design Manager — Single Device Selection 3-4
Software Device Selection Criteria 3-4
Manual Logic Placement 3-5
Manual Pin Assignment 3-5

Design Manager — Design Optimization Control 3-6
Timing 3-8
Global Output Enable 3-8
Global Clock 3-9
Power Management 3-9
Design Manager — Power Management 3-9
Slewrate Control 3-11
Initial State Control 3-11
Design Manager — Resource Reservation 3-12
Reserved Input Pins 3-14
Reserved Output Pins 3-14
Reserved Bidirectional Pins 3-14
Reserved Macrocells 3-14

Chapter 4 Controlling Design Timing

Design Manager — Timing Control 4-1
Schematic — Timing Control 4-3
Defining Timing Specifications 4-3
The TIMESPEC Primitive 4-3
TIMESPEC Attribute Syntax 4-4
Defining Timing Path End Points 4-4
Using Predefined Groups 4-5
Creating Arbitrary Groups Using TNMs 4-5
Creating New Groups from Existing Groups 4-9
The TIMEGRP Primitive 4-9
Combining Multiple Groups into One 4-10
Creating Groups by Exclusion 4-11
Creating Groups by Pattern Matching 4-11
Using Wildcards to Specify Signal Names 4-12
Multiple Specifications Applied to the Same Path 4-12
Ignoring Selected Paths 4-13
Breaking Combinational Loops 4-13
Specifying Relative TS Attribute Delays 4-13
Specifying Time Delay Units 4-15
Example Schematic Using TNMs and TIMEGRPs 4-15
Timing Control Syntax Summary 4-16
TNM Attributes 4-17
TIMEGRP Attributes 4-17
TIMESPEC Attributes 4-17
Timing Control using a Timing Constraints File 4-17
Constraints File Syntax Conventions 4-18

TIMESPEC Constraint Statement Syntax 4-19
TIMEGRP Constraint Statement Syntax 4-20
Creating a Constraints File 4-21

Chapter 5 Timing Analysis

Timing Analysis Procedure 5-1
Timing Analysis Window Features 5-2
Generating Reports 5-3
Standard Report Header 5-3
Performance to Timespecs Report 5-3
Performance Summary Report 5-4
Detailed Path Report 5-6
Check for Asynchronous Logic 5-8
Show Clocks 5-8
Show Settings 5-8
Report Window Commands 5-9
Report Paths Failing Timespec 5-11
Report Paths with No Timespec 5-11
Ignore Timespecs 5-12
Select Sources and Select Destinations 5-13
Select Path Types 5-16
Include or Exclude Paths with Nets 5-18
Break Logic Loops 5-21
Reset Path Filters 5-23
Selecting Additional Options (Optional) 5-24
Set Speed Grade 5-24
Set Delay Margins for I/O 5-24
Report Options 5-26

Chapter 1

Design Flow

This chapter gives an introduction to the Design Manager design flow, including:

- How to prepare behavioral, schematic, and VHDL designs.
- How to translate designs into the required format.
- How to fit designs into a target device (or devices).
- Alternatives for simulation, programming, and reporting of designs that have been processed.
- A quick tutorial with a simple design example.

Overview of Design Processing

There are seven basic steps in processing your design:

1. Design Entry to create your design source file.
2. Project Creation to open a new project file.
3. Translation of your design file into Xilinx's internal .XFF format.
4. Implementation of your design into a specific target device.
5. Export of your design for timing simulation and programming.
6. Report Generation showing the status of your design.
7. Timing Analysis for design verification.

Design Entry

You can use a variety of schematic and behavioral tools to create your design.

The currently supported schematic entry tools are:

- Viewlogic.

The currently supported behavioral entry tools are:

- Xilinx ABEL.
- PLUSASM.

Prepare your design for input to the Design Manager as follows:

- For schematic designs — Save your design using the native file extension (.1 for Viewlogic).
- For Xilinx ABEL designs — Generate an EPLD equation file for a stand-alone design (this saves the design as a .PLD file).

Project Creation

This step is only done once for each project, to create the files which will contain all information about your design. Design translation, which is explained in the next section, is performed automatically when you create a new project file.

To create a new project do the following, after you have created a design source file:

1. Start the Design Manager.
2. Select the New Project command from the File menu. The New Project window appears.
3. Select XC9500 or XC7000 as the Target Family.
4. Select the Browse button to the right of the Input Design field. The Open browser window appears.
5. Change the List Files of Type value to Any File (*.*).
   - PLUSASM and compiled ABEL files have a .PLD extension.
   - Viewlogic schematic files have a .1 extension.
   - All other files have an .XNF extension.
6. Select the drive if necessary, the directory, and the design file. (Viewlogic designs use the WIR directory.)
7. Select the OK button to close the browser.

8. Select the Translate button to close the New Project window.
9. The Translate Options window appears. If you did not specify the device type in the design file using the PART attribute, select the Read Part from Design box to remove the check. Click OK.
10. A translation window appears, which shows the translation of the design file into a standard Xilinx .XFF format, ready for processing. When these translations are complete, a message box appears telling you that the translation completed successfully. Click OK.

Design Translation

You must first translate your source design into the standard Xilinx data format (.XFF) before the software can process your design. For new projects, design translation is performed automatically when the project is first created. For existing projects, you must do design translation each time you make a change to your design source file. Figure 1-1 shows the basic flow.

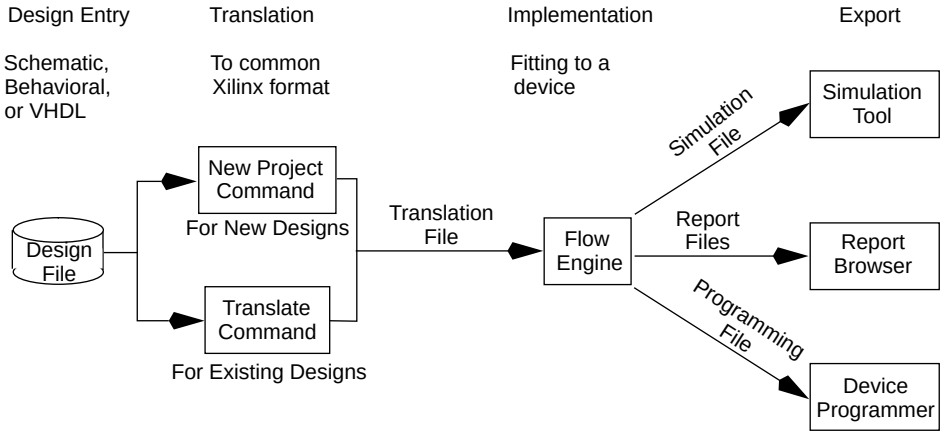


Figure 1-1 Design Manager Design Flow

To translate your design (after making changes to your source file) do the following:

1. Start the Design Manager.

2. Select the Translate command from the Design menu. The Translate Options window appears.
   - If you want the software to read the target device part type from your design file, select Read Part From Design.
   - If you want to select a specific target device type, click Select Part and you will see the Part Selector window. From here you can choose any available device.

Design Implementation and Device Programming

Design implementation is the process of fitting your design into a target device. To implement your design:

1. Select the Implement command from the Design menu. The Design Implementation Dialog box appears with the following options:
   - Produce Timing Report — If this box is checked, a timing report showing the calculated worst-case timing for your design is created.
   - Produce Timing Simulation Data — If this box is checked, the Flow Engine produces a timing simulation file in the appropriate format and copies this file into your design directory.
   - Produce Configuration Data — If this box is checked, the Flow Engine produces a JEDEC file that you can use to program your device.
2. Select the Run button to start the Flow Engine. The Flow Engine window appears, displaying the stages in the design processing.

See Chapter 2 for more information about the Design Manager and the Flow Engine. For information about simulation, see the Interface User Guide for your system.

Report Generation

The Flow Engine produces several reports, which are described in more detail in the “Reports” chapter.

- Translation Report — Shows the results of the translation process.

- Fitter Report — Lists the device resources used by the design and the resources remaining; shows how the external nets in your design were mapped to the device pins; tells you how the logic in the design was mapped to the device; and shows the allocation of Function Block resources.
- Timing Report — Shows the calculated worst-case timing for the logic paths in your design.
- Timespec Report — Tells you if you have made any errors in assigning T-Spec attributes in your design and lists the T-Specs that the fitter used.

Timing Analysis

You can analyze the timing of your implemented design using the Timing Analyzer. To open the Timing Analyzer, double click on its icon; the current design in the Design Manager is automatically loaded.

You can choose from the following timing reports, which are listed on the Analyze menu:

- Performance to TimeSpecs — Compares the implementation of the design with the imposed timing constraints. (For more information about timing constraints, see the “Controlling Design Timing” chapter.)
- Performance Summary — Summarizes the overall design performance.
- Detailed Path Report — Lists worst-case path delay information for all paths in the design that have not been excluded by filters.
- Check for Asynchronous Logic — Lists signals that are possibly asynchronous and the product-term clock signals that control them.
- Show Clocks — Lists the clock signals in the design.
- Show Settings — Lists the current settings of the timing analyzer, including which path filters have been applied.

You can apply filters to include in the reports only the paths you are interested in. You can also change other options that affect timing, such as the speed grade of the device. For more information, see

Chapter 5.

Quick Tutorial

This section shows you how a 4-bit Johnson counter design is processed through the Design Manager. The schematic version of this design is shown in Figure 1-2.

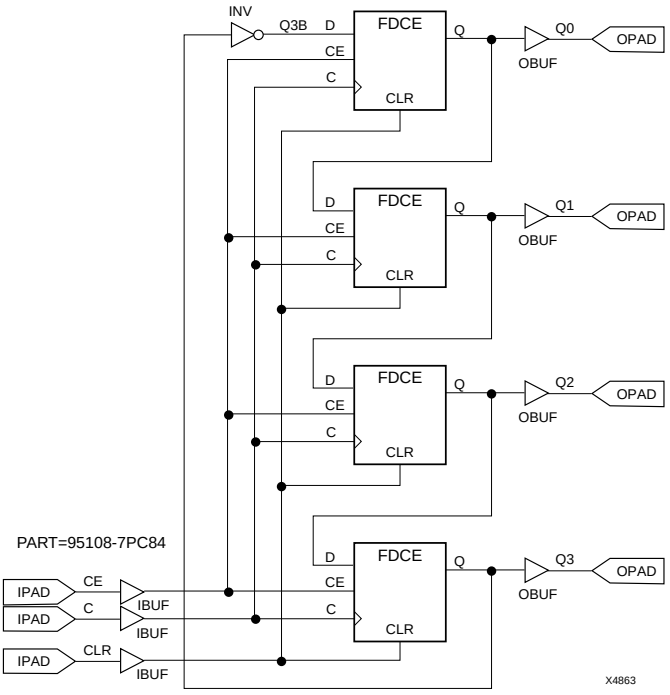


Figure 1-2 Example 4-Bit Johnson Counter Design (jcount)

Enter the Design

Create the design in your design entry tool and save it to a file named "jcount." Be sure to include the target device part type in your source file. The design entry software will add the appropriate file extension to the design file.

Create a New Project

1. Start the Design Manager. The initial Design Manager window, before you have opened a design, looks as shown in Figure 1-3.

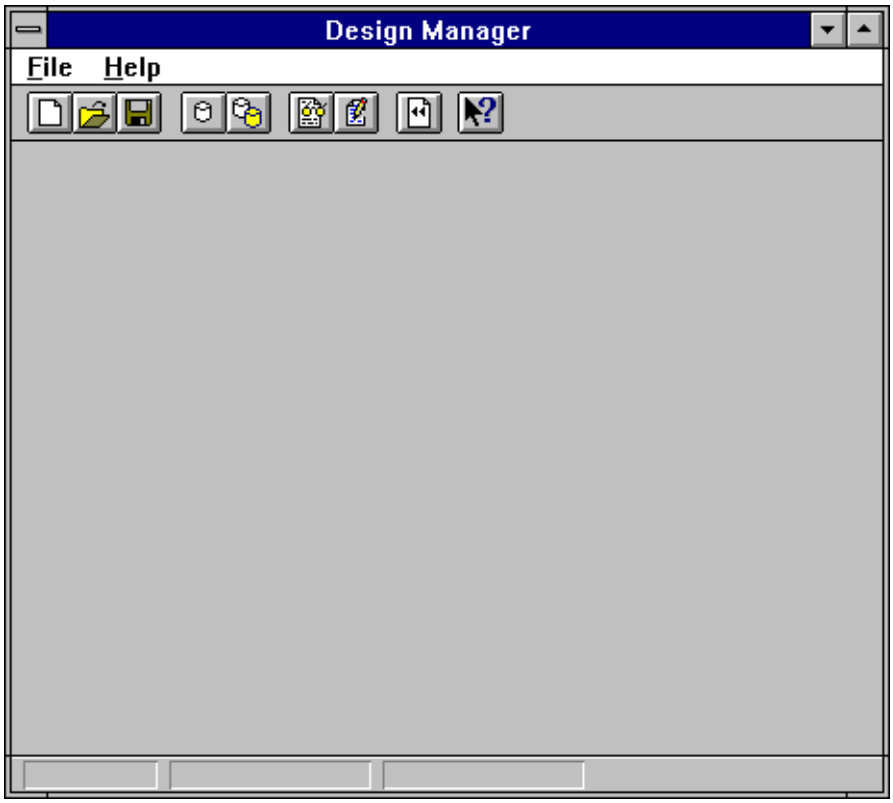


Figure 1-3 The Design Manager Window with No Design

2. Select the New Project command from the File menu. The New Project window appears as shown in Figure 1-4.

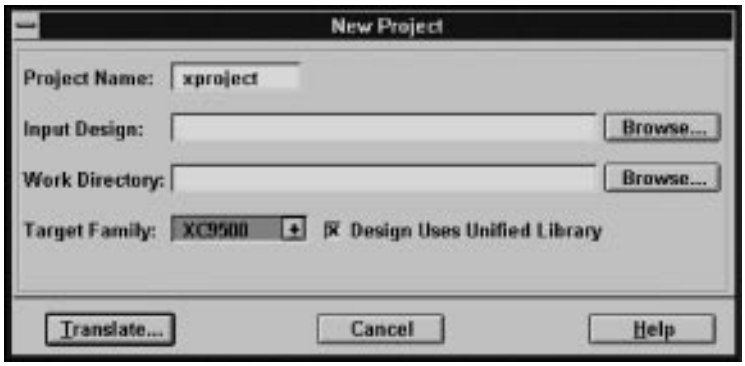


Figure 1-4 New Project Window

3. Select XC9500 or XC7000 as the Target Family.
4. Select the Browse button to the right of the Input Design field. The Open browser window appears as in Figure 1-5.

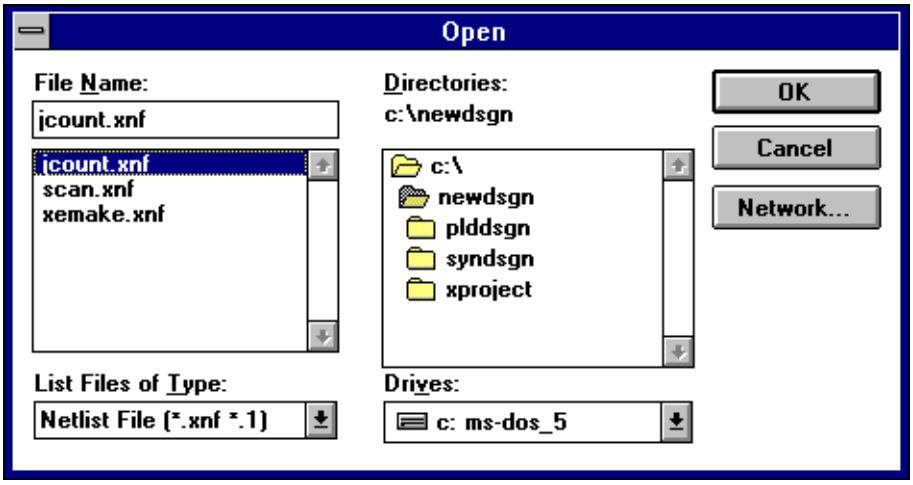


Figure 1-5 New Project Browser

5. For a behavioral design, change the List Files of Type value to Any File (*.*). PLUSASM files have a .PLD extension. Other design files

have extensions of .1 (for Viewlogic) or .XNF (generic).

6. Select the drive if necessary, the directory (the WIR directory for a Viewlogic design), and the design file.
7. Select the OK button to close the browser. Select the Translate button to close the New Project window.
8. The Translate Options window appears as in Figure 1-6:

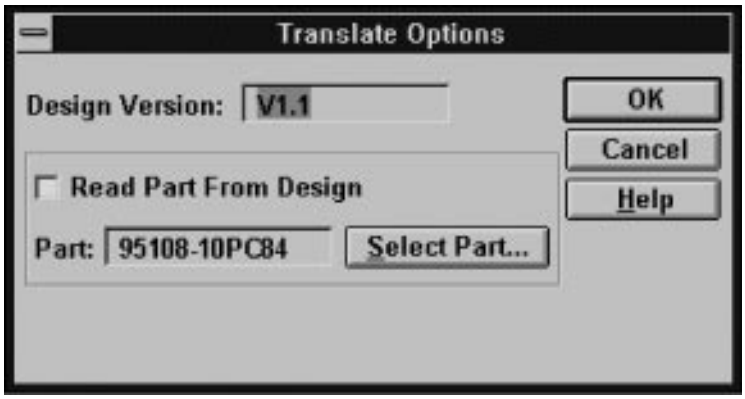


Figure 1-6 Translate Options Window

- If you specified a target device in your source file (and you want to use that device) select Read Part From Design.
- If you did not specify the device type in your design source file, remove the “X” from the Read Part From Design box. Then, specify the target device type by clicking on Select Part.

You will see the Part Selector window as shown in Figure 1-7.

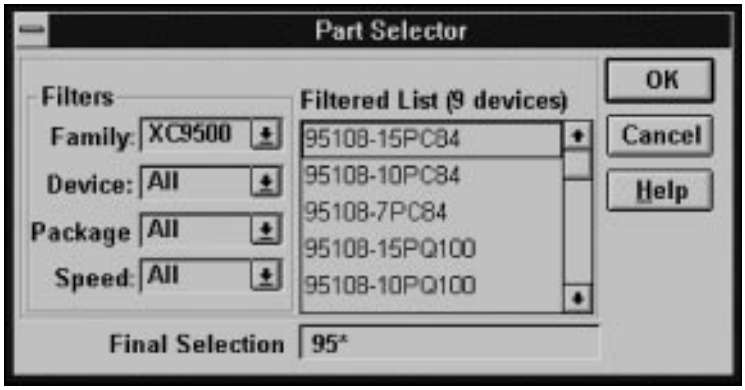


Figure 1-7 Part Selector

Select XC95108PC84-7 and click OK.

9. A translation window appears, which translates the design file into an .XNF and an .XFF file. When these translations are complete, a message box appears telling you that the translation completed successfully. Select the OK button.

After your design has been loaded, the Design Manager window looks as shown in Figure 1-8.

Figure 1-8 The Design Manager Window with a Design Loaded

Implement the Design

To implement the design, follow these steps:

1. Select the Implement command from the Design menu. The Design Implementation Dialog box appears as shown in Figure 1-9.

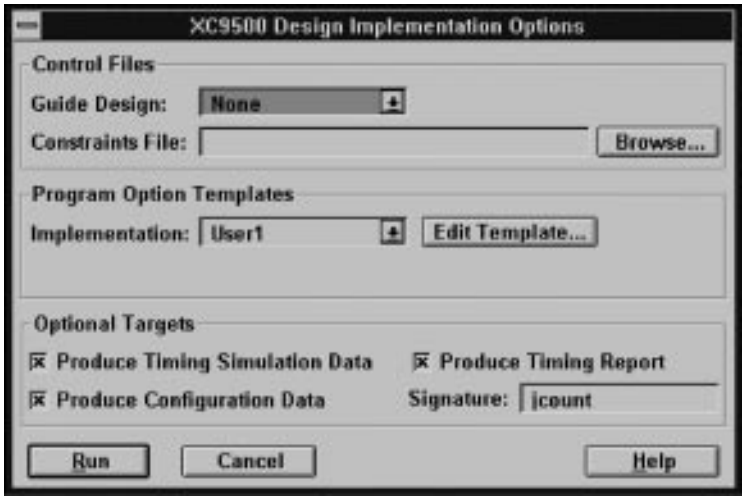


Figure 1-9 Design Implementation Dialog Box

2. Select Produce Timing Report, Produce Timing Simulation Data, and Produce Configuration Data options.
3. Click Run to implement the design. The Flow Engine window appears as in Figure 1-10, displaying the stages in the design processing. As reports are generated, you see their icons appear in the Report Browser window.

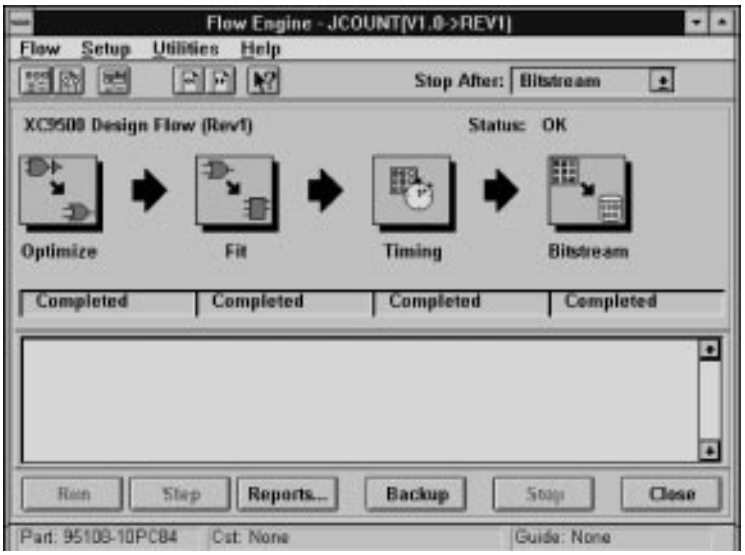


Figure 1-10 Flow Engine Window (Non-Interactive)

4. When processing is complete, you can view the fitter reports (including the timing report) as described in the next section, perform timing simulation, and program the device. Timing simulation is described in the Interface User Guide for your system.

Use the Report Browser

The Report Browser opens automatically when you select the Implement command. (To manually open the report browser, select the Report Browser command from the Utilities menu.) The Report Browser window appears as shown in Figure 1-11.

Figure 1-11 Report Browser

Double click on the Fitting Report icon. The report appears in its own window, as shown in Figure 1-12.

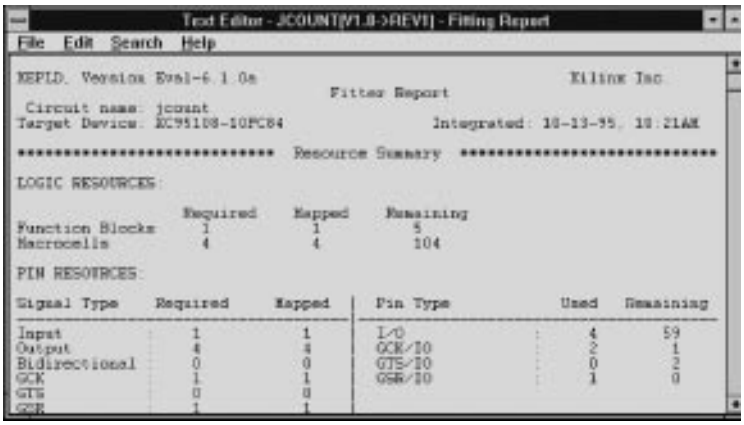


Figure 1-12 Fitting Report Window

You can save the report to an ASCII file using the File-Save As command, print the report using File-Print, or close the report window using File-Exit. Select these commands from the report window, not the main Design Manager window.

Use the Timing Analyzer

Double click on the Timing Analyzer icon in the Tools sub-window, as shown in Figure 1-13.

Figure 1-13 Timing Analyzer Icon

The Timing Analyzer main window opens as shown in Figure 1-14,

and the jcount design is loaded automatically.

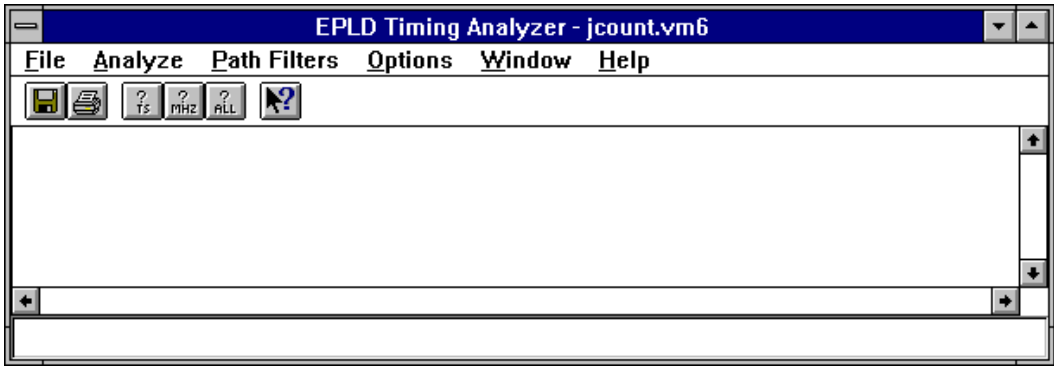


Figure 1-14 Timing Analyzer Main Window

Select the Performance Summary command from the Analyze menu. A report window appears containing the following report:

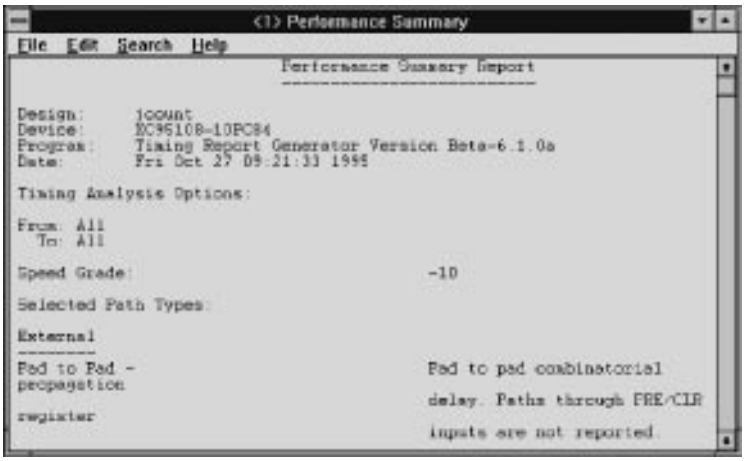


Figure 1-15 Report Summary

To close the report window, select the File-Exit command in the report window. To close the Timing Analyzer, select the File-Exit command in the main Timing Analyzer window.

Chapter 2

Using The Design Manager

This chapter shows you how to manage your design files and how to control your design process flow. Each menu command is described and procedures for common tasks are provided. A typical Design Manager Window is illustrated below.

Figure 2-1 The Design Manager Window

Design Manager Fundamentals

There are four main functions of design management that are addressed by the Design Manager:

- Grouping all related Design Files (project). The Design Manager

window displays all files related to a single project. The hierarchical file structure shows you the relationships of the files to each other.

- Maintaining Design Versions (logic). Each time you change the logic of your design a new version is created. This allows you to try modified versions of your design and easily keep track of them. Old versions can be deleted as desired.
- Selecting Device Implementations (target devices). Each version of your design can have multiple implementations (target devices) in which fitting can be attempted.
- Maintaining Implementation Revisions (fitting strategies). You can have multiple fitting strategies (revisions) for each device implementation. This allows you to optimize your design for speed and density while retaining your data.

The Design Manager Window, showing your design versions, implementations, and revisions appears when you have chosen an existing project in which to work or have opened a new project. In addition, within the Design Manager User Interface, there are three tools:

- The Flow Engine, used to control the fitting of your design.
- The Partitioner, used to manage multiple device partitioning.
- The Timing Analyzer, used to verify your design timing.

Managing Projects

A project includes all design versions, device implementations, and implementation revisions that are created as you develop your design. The Design Manager Window shown in Figure 2-1 displays the data associated with a single project. You can work with multiple projects (designs) but only one at a time is displayed.

Managing Design Versions

You create your design using third party front-end tools such as schematic editors, behavioral equation editors, and VHDL. These tools output either an .XNF or .PLD file that describes the logic of your design. You create a new .XNF or PLD file each time you change your source design and import that new design to the Design

Manager.

Each new .XNF file you import becomes a new design version and is assigned a version number by the Design Manager. You can choose any one of the available versions for processing and for each version you may choose multiple target device implementations and different fitting strategies. The Design Manager also allows you to delete versions that are no longer useful.

Managing Device Implementations

You can fit your design into any number of different target devices; each is called an implementation. You can specify devices explicitly or you can specify a range of devices from which the software can choose the best one. For example, you could specify a device family and package type only, allowing the software to choose the best device type and speed grade for your design. For a description of the automatic device selection process, see Chapter 3.

For each version of your design you can have multiple implementations using different target devices or different fitting strategies.

Managing Implementation Revisions

After you have created a design version by inputting an .XNF file, and you have chosen a target device (or devices), you can try different fitting strategies on that design. This allows you to vary how your design is implemented in order to achieve your design objectives. For example, you can maximize speed and density for specific functions in your design by controlling the fitting process. Each of these fitting strategies is called a design revision.

Each design revision contains the output files and reports that are created based on a specific set of fitting strategies. the Design Manager also allows you to delete revisions that are no longer useful.

Design Management Procedure

The typical procedure for managing a design is as follows:

1. Create your design using a third-party front-end tool such as those available from Viewlogic and Data I/O. Your design is

output as an .XNF, .1, or .PLD file, depending on the tool you are using.

2. Open an existing project file; or create a new project file in which to import your logic design.
3. Import your logic design. Your source file is converted into the Xilinx internal data base format (.XFF).
4. Choose a target device (or devices) in which to implement your design. Or, allow the software to automatically choose target devices based on your selection criteria.
5. Define option templates to control your design process flow. Or, use the default template settings.
6. Process (fit) your design and:
   - Create timing simulation files (optional).
   - Create a device programming file (optional)
7. Review your design reports to verify that your design fits within the target device and that your timing requirements are met.
8. If your design requirements are not met you can do the following and process your design again:
   - Change your logic design.
   - Choose a different target device, package, or speed grade.
   - Define a different set of fitting options (option templates).

Using the Design Manager

This section describes the Design Manager menu commands and provides the procedures for using them.

The Initial Design Manager Window

When you first run the Design Manager you will see the initial Design Manager window as shown in Figure 2-2.

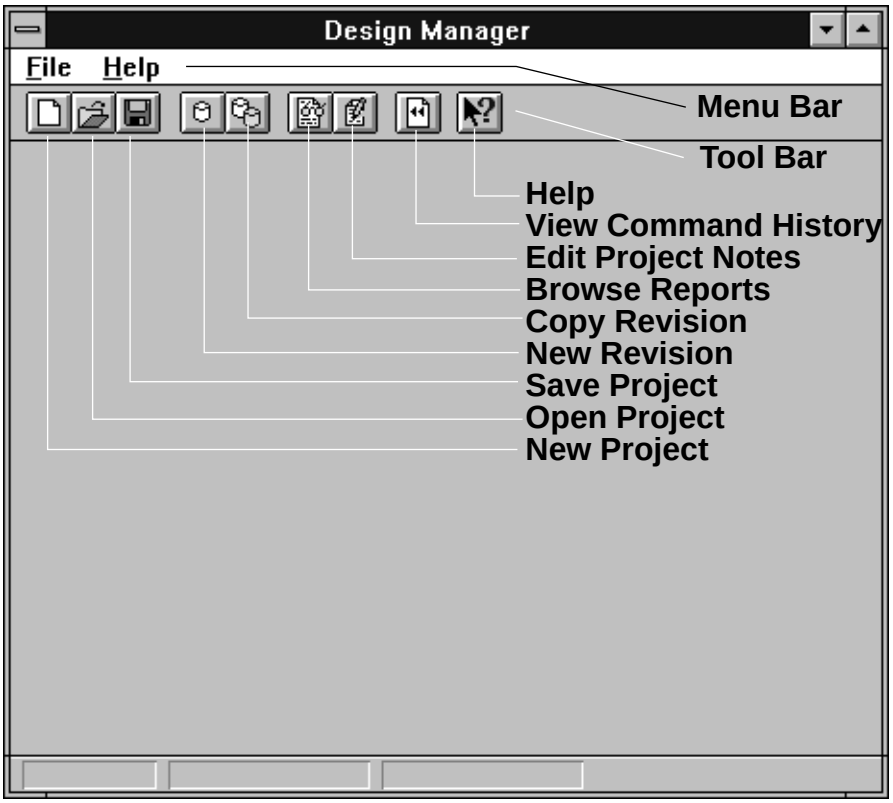


Figure 2-2 The Initial Design Manager Window

The Menu bar contains the primary menu commands arranged according to the types of functions you need to perform. When you click a Menu Bar selection, you see a sub-menu with more

commands. In the initial Design Manager Window (Figure 2-2) you see only the File and Help commands because these are all you need until you have opened a project. After a project is opened, you will see the full Menu Bar with all available menu commands as shown in Figure 2-1.

The Tool Bar contains icons that represent commonly used functions such as Help, for quick access. Each of these functions is also accessible through the Menu Bar sub commands.

Each menu command is described in the following sections.

File Menu

Use the File menu to manage projects and to exit the Design Manager. When you select File, you see the menu shown in Figure 2-3.

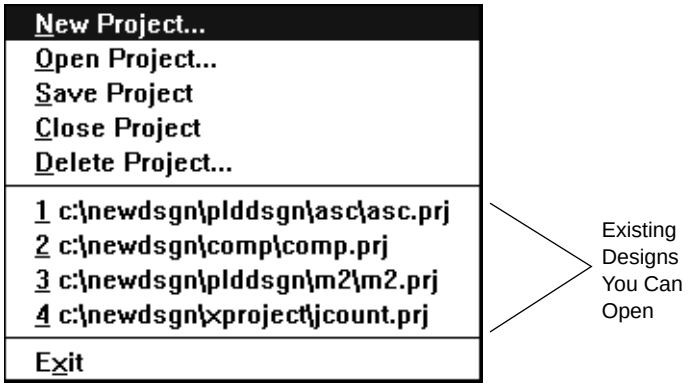


Figure 2-3 The File Menu

File — New Project

Select New Project to create an empty project directory to receive a new design; you will see the New Project dialog window as shown in Figure 2-4.

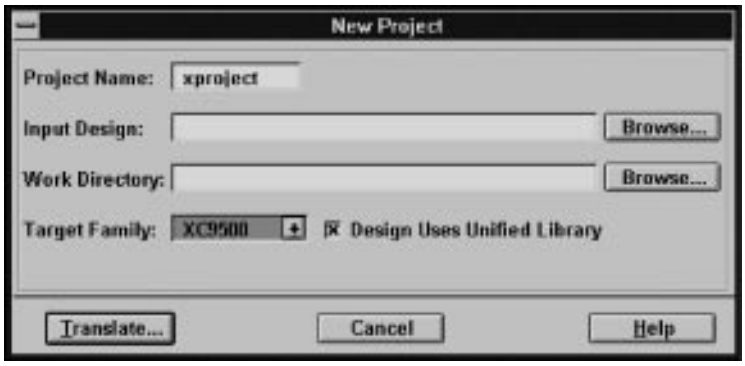


Figure 2-4 The New Project Dialog Window

To open a new project, follow these steps:

1. Enter a project name in the Input Design dialog box. Or, click on Browse and you will see the Open dialog window as shown in Figure 2-5. From here you can select a design file to input.

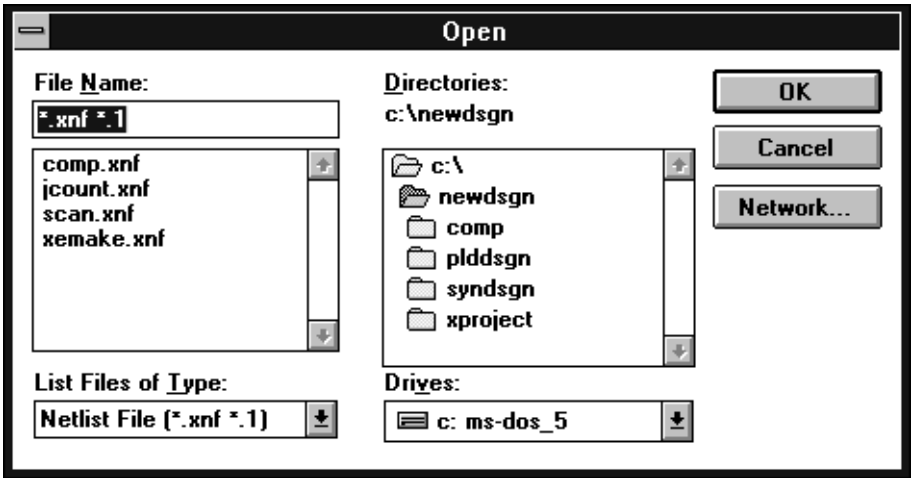


Figure 2-5 The Open Dialog Window

Note that the List of File Types in the Open Dialog Window is already set to find all .XNF files for you; .XNF is the most common input file

type. You can change this to .PLD or any other file type for which you want to search.

2. Select the target device family from the Target Family pull-down dialog box. Select XC9500 or XC7000 to target Xilinx EPLDs. The other selections are for Xilinx FPGA devices.

3. Specify if your design is targeted to one device (Single Chip Design) or to multiple devices (Multi-Chip design).

Note: Use Single Chip Design only; multi-chip partitioning is not available in this beta release.

4. Specify your working directory. You can browse through the available directories by clicking on Browse, which brings up the dialog window as shown in Figure 2-6. From here, select the working directory and click OK.

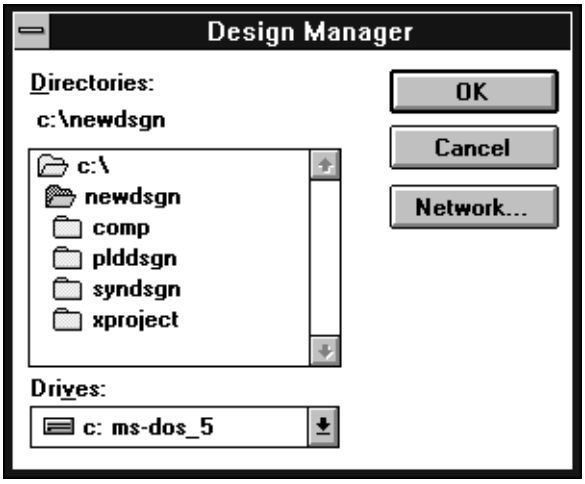


Figure 2-6 The Work Directory Browse Dialog Window

5. After you have specified the project name, device family, and working directory, you can input (translate) your logic design by clicking on the Translate button. You will see the Translate Options dialog window as shown in Figure 2-7.

6. From the Translate Options dialog window you can choose a design version number or accept the default version number. You can also specify whether the software is to read the device information contained in your source file or use the part you have selected. To select a Part click Select Part and you see the Part Selector window from which you can specify a target device as shown in Figure 2-8. Click OK when done.

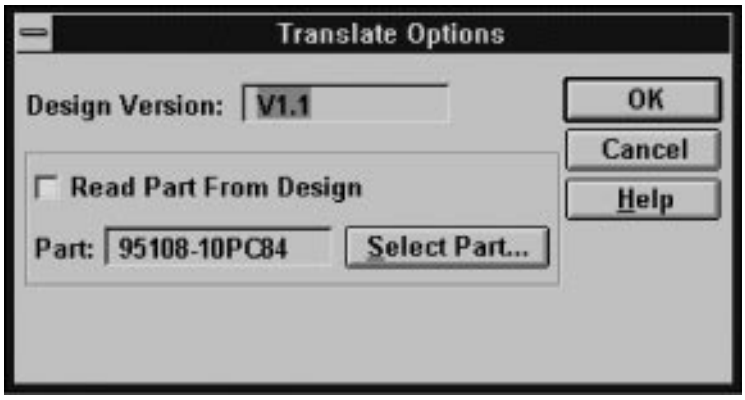


Figure 2-7 Import Design Translation Flow Window

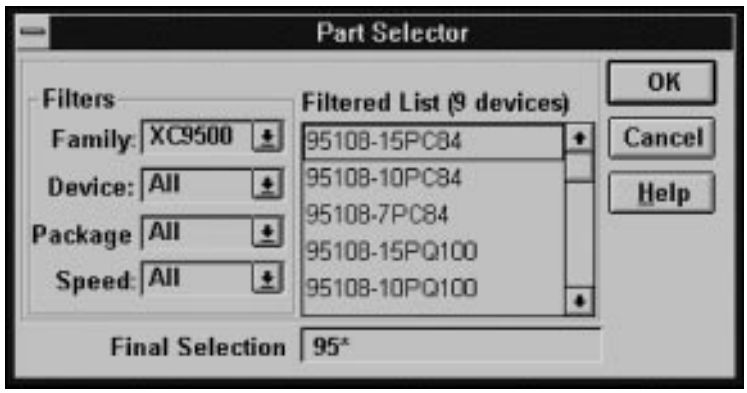


Figure 2-8 Part Selector

After you have selected the Translate Options, click OK and your design file is input and converted to the Xilinx .XFF internal database format, ready for processing.

When the translation is complete, you see the Translate Confirmation Dialog Window as shown in Figure 2-9.

Figure 2-9 Translate Confirmation Dialog Window

7. From here, if you select Review log, you will see the Translation log report as shown in Figure 2-10.

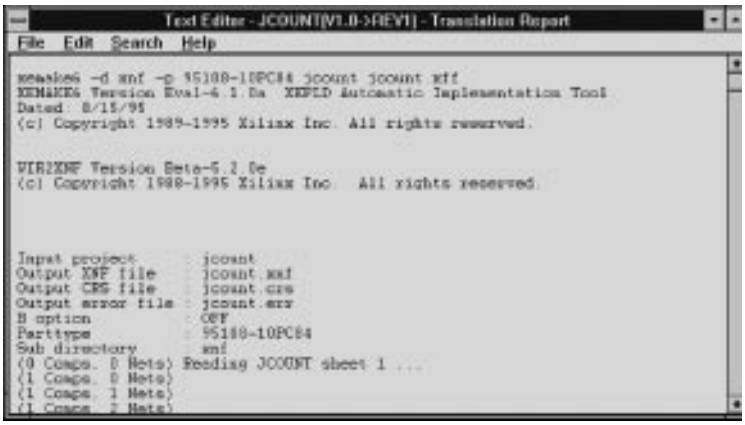


Figure 2-10 Translation Log Report

This log report shows you the commands that were executed in the translation of your design as well as any warnings or error messages.

File — Open Project

Select Open Project to open an existing project. You will see the

following dialog box, which displays all available projects:

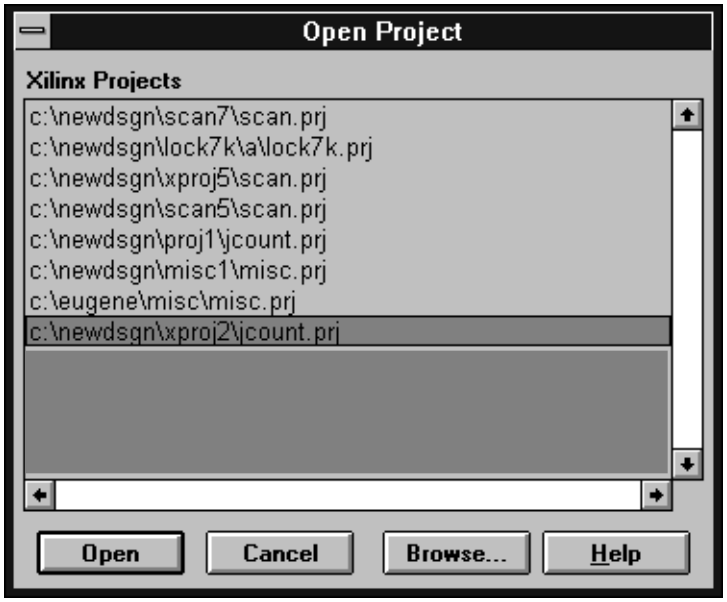


Figure 2-11 The Open Project Dialog Window

If you double-click a project, or highlight a project and click Open, the project file opens and you will be returned to the Design Manager window with the project hierarchy displayed.

File — Save Project

Select Save Project to save all files associated with your current project.

File — Close Project

Use Close Project to close and save all files associated with the current project.

File — Delete Project

Select Delete Project to remove a project from your list of active

projects and you will see the dialog window shown in Figure 2-12.

Figure 2-12 The Xilinx Projects Dialog Window

Double-click on the project you want to delete, or highlight the project and click the Delete button.

If you do not wish to delete a project at this time, click Cancel and you are returned to the Design Manager window.

File — File name

The File menu automatically lists all available project names. You can open any listed project by simply clicking the name.

File — Exit

Select Exit to close your design and exit the Design Manager. Your project is saved automatically

Design Menu

Select Design from the menu bar and you see the menu as shown in

Figure 2-13.

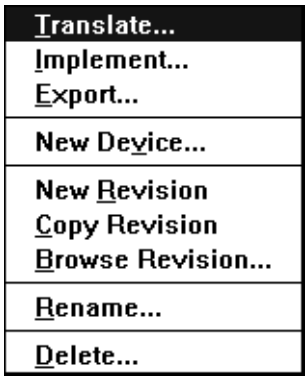


Figure 2-13 The Design Menu

Design — Translate

Select Translate to input your logic design and convert it to the Xilinx internal database format (.XFF) ready for processing. You will see the Translate Options dialog window as shown in Figure 2-14.

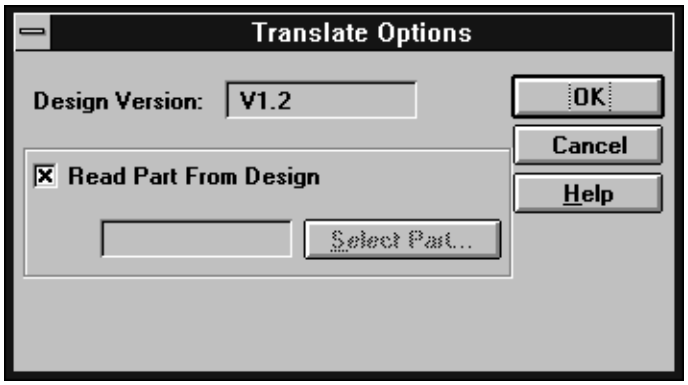


Figure 2-14 Import Design Translation Flow Window

From the Translate Options dialog window you can choose a design version number or accept the default version number. You can also specify if the software is to read the device information contained in your source file.

After you have selected the Translate Options, click OK and your design file is input and converted to a Xilinx .XFF internal database format.

The supported input formats are:

- .XNF — Xilinx Netlist Format, supported by most tools.
- .1 — ViewLogic schematic output format.
- .PLD — PAL and PLD files.

When the translation is complete you see the Translate Confirmation Dialog Window as shown in Figure 2-15.

Figure 2-15 Translate Confirmation Dialog Window

From here, if you select Review log, you will see the Translation log report as shown previously in Figure 2-10. Select OK and you are returned to the previous menu.

Design — Implement

Select Implement and you see the Design Implementation Dialog Window as shown in Figure 2-16. Use this dialog window to control the fitting process by specifying control files, program option templates, and optional target files for your design.

To implement your design follow these guidelines:

- Guide Design: If you want to use the pinouts from a previous implementation, click on the Guide Design scroll arrow to see a

list of all available Guide Files (.GYD). A guide file is created each time you fit your design and you can reuse this pinout information to maintain design consistency. For more information on using Guide Files see Chapter 3.

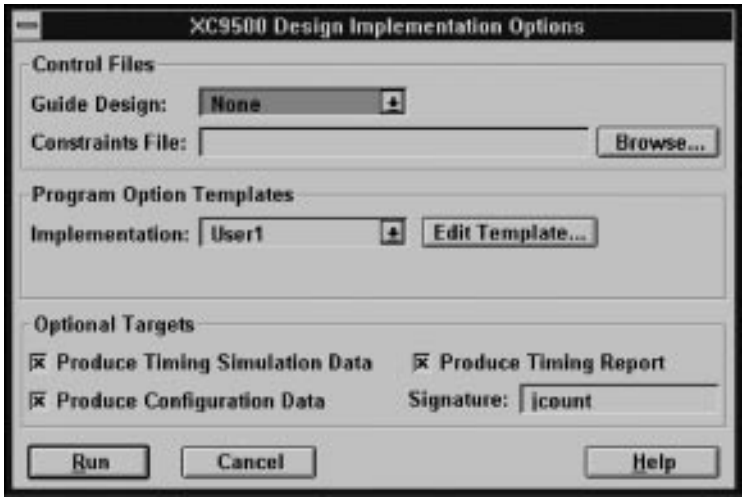


Figure 2-16 The Design Implementation Dialog Window

- Constraints File: If you want to use timing-driven optimization, enter a constraints file name or click on the Browse button to see a list of all available timing constraints files. For information on how to create a constraints file, see Chapter 4.
- Implementation: If you want to use a Program Option Template, (a set of fitter options that control your design processing), click on the Implementation scroll arrow to see a list of all available Program Option Templates. Click Edit Template if you want to change the template parameters. See the “Template Manager” section (Figure 2-33) for more information on how to create and edit Option Templates.
- Produce Timing Report: If you want to produce a timing summary report click this check box; an X appears to indicate that the option is selected. For a more detailed timing analysis, you can use the static timing analyzer after the design is implemented. See Chapter 6 for more information on Timing Reports.

- Produce Timing Simulation Data: If you want to produce timing simulation data, click this check box. Check this option if you intend to use a third party timing simulator to verify your design.
- Produce Configuration Data: If you want to output configuration data (a device programming file), click this check box. You will also need to enter a unique text string in the Signature dialog box to identify this file.
- Run: When all options are entered, click the Run button to implement your design. You will see the simplified Flow engine Dialog window along with the Report browser, as shown in Figure 2-17. As the simplified Flow Engine processes your design, you will see the reports highlighted as they are created.

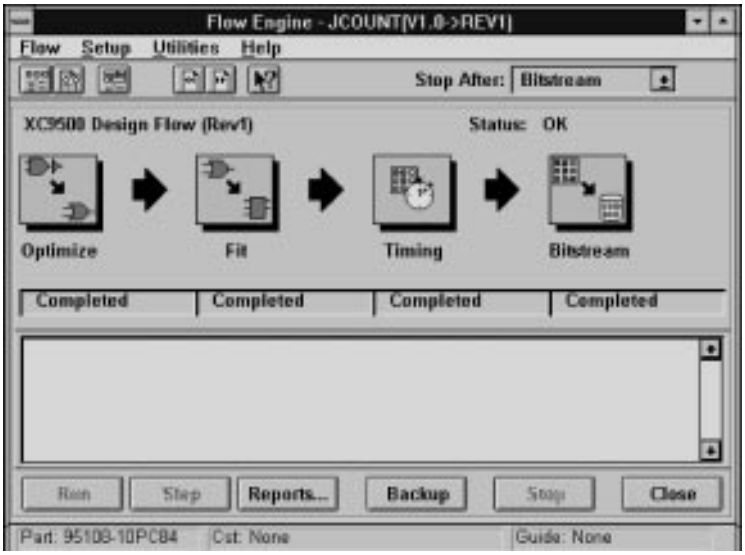


Figure 2-17 The Simplified Flow Engine with Report Browser

Note: When you implement your design from the Design menu, you see the simplified Flow Engine shown above. The simplified Flow Engine has a limited set of options. If you want the full set of options, to control the operation of the Flow Engine, select the Flow Engine from the tools menu or from its icon in the Design Manager Toolbox.

Design — Export

Select Export to control the types of output data produced by the software.

Figure 2-18 The Export Data Dialog Window

- Physical Design Data: Select this option to export a guide file (.GYD) containing your pinout information. This file is used to recreate you existing pinout after making design changes.
- Timing Simulation Data: Select this option to export a simulation file (.XNF) for third-party simulators such as those available from Viewlogic (ViewSim).
- Configuration Data: Select this option to export a device programming file (.JED).
- Files To Export: Here you see all files that match the data type you have selected for export.
- Export To: Enter the full path of the file to which you are exporting the data. Select Browse to see a list of all available files as shown in Figure 2-19.

Click OK when you are ready to export the data.

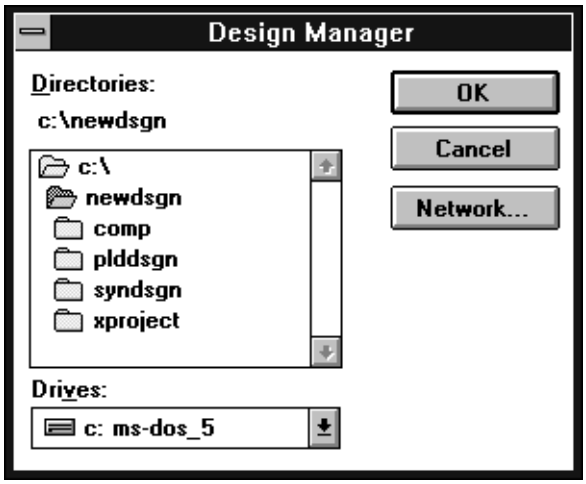


Figure 2-19 The Export Data Browse Dialog Window

Design — New Device

Select New Device to add a new target device under the selected version hierarchy. This allows you to try different devices (and fitting strategies) for a specific version of your design. You can either specify a single device or a range of possible devices from which the software can choose the best one. The device selection procedure is described as follows:

1. Select the version under which the new target device is to be added.
2. Select New Device from the Design menu. You will see the Part Selector dialog window as shown in Figure 2-20.

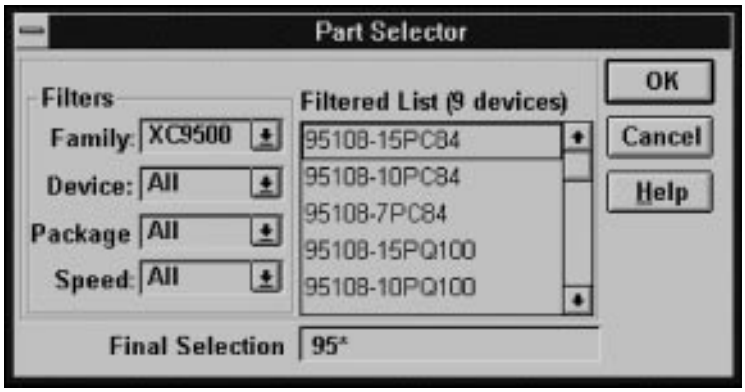


Figure 2-20 Part Selector Window

3. If you know the specific device you want to use, select the part type, package type, and speed grade by scrolling through the available options as shown in Figure 2-20. For EPLD designs select the XC9500 family or the XC7000 family.
4. If you want to allow the software to choose the best device for your design, specify only those parameters that you require. For example, you can specify the PC84 package and leave the device type and speed grade unspecified. The unspecified parameters are shown as an asterisk (*) in the Final Selection window and on the Design Manager window.

   Click OK and the specified device (or set of devices) is added to the design hierarchy as shown in Figure 2-1.

Design — New Revision

Select New Revision to create a new (translated) revision of your design in .XFF format. This does not save any of your previous implementation data.

Design — Copy Revision

Select a revision in the Design Manager window and Select Copy Revision to make a copy of that revision. You will see the new revision (a copy) displayed in the Design Manager window using the

next Rev number. For example, if Rev 1, Rev 2, and Rev3 already exist and you make a copy (of any one), Rev 4 will be created. Usually you copy a revision in order to modify the fitting strategy it contains. A revision copy contains the previous implementation data.

Design — Browse Revision

Select Browse Revision to edit, copy, move, rename, or delete the files contained within a revision; you see the Revision Browser dialog window as shown in Figure 2-21.

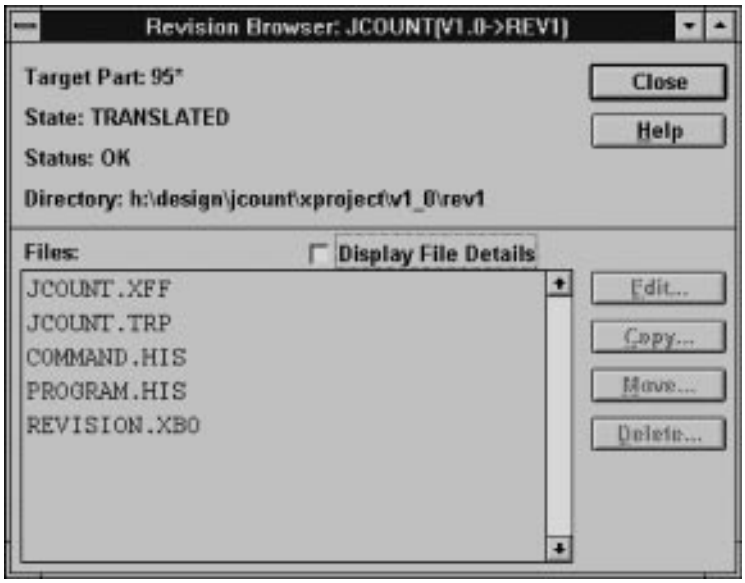


Figure 2-21 The Revision Browser Dialog Window

This dialog window shows you the following information:

- Target Part: The device to which the selected revision is targeted.
- State: The last completed process step for the selected revision, which is either: TRANSLATED, OPTIMIZED, FIT, TIMING, or PROGRAMMED.
- Status: The status of the design processing up to the current state:
  - OK — The software generated no errors or warnings.

- Warning — The software encountered a situation that may require your attention.
- Error — The software encountered a processing error.

- Directory: The directory in which the selected revision resides.
- Files: This scroll box shows you all the files contained within the selected revision. If you want to display the file details (creation date, creation time, and so on), select the Display File Details check box.
- Edit: If you want to modify a file, select the file and click Edit; you will see the dialog window shown in Figure 2-22:

Figure 2-22 The Browse Revision Edit Dialog Window

Use this file editor to make changes to the selected file.

- Copy: If you want to copy a file, click Copy and you see the

following Save As Dialog window as shown in Figure 2-23.

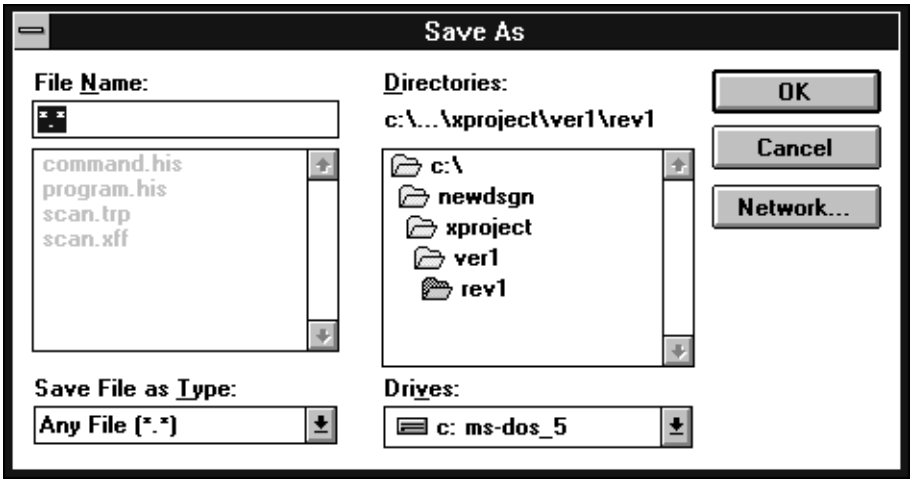


Figure 2-23 The Save As Dialog Window

- Move: If you want to move a file, highlight the file name in the Revision Browser window and click Move; you will see the same Save As dialog window as shown in Figure 2-23.
- Delete: If you want to delete a file, select the file name in the Revision Browser window and click Delete; you will see the delete confirmation window shown in Figure 2-24.

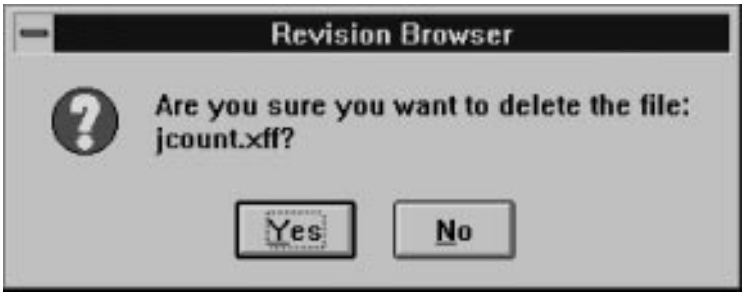


Figure 2-24 The Delete Confirmation Window

Click Yes and the file is deleted. Click No and you are returned to the previous menu.

Design — Rename

Highlight the revision in the Design Manager window and then select Name Revision to assign a name to the selected revision; you will see the Name Revision dialog window as shown in Figure 2-25.

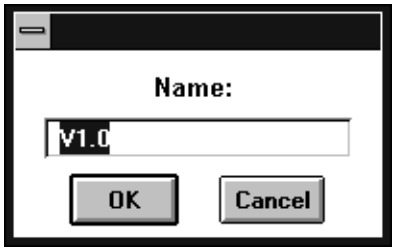


Figure 2-25 Name Revision Dialog Window

Enter the revision name in the dialog box and click OK to apply that name to the selected revision. The name you enter will replace the Rev number. For example, if you select “Rev 1 (Translated)” to rename and enter the name “MyRev8”, you will see the name change to “MyRev8 (Translated)”. Click Cancel to return to the Design Manager window.

Design — Delete Revision

Highlight a revision in the Design Manager window and then select Delete Revision and you will see the dialog window as shown in Figure 2-26.

Figure 2-26 Delete Revision Dialog Window

Click Yes and the highlighted revision is deleted. Click No and you are returned to the Implementation menu.

Tools Menu

Use the Tools menu to select the Flow Engine, the Timing Analyzer, or the Multi-Chip Partitioner, and you see the menu as shown in Figure 2-27.

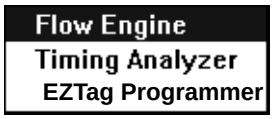


Figure 2-27 The Tools Menu

Tools — Flow Engine

The Flow Engine is used to control the processing of your design including optimization, fitting, timing simulation data generation, and device programming file generation. See “Using the Flow Engine” later in this chapter, for more information.

Tools — Timing Analyzer

The Timing Analyzer is used to verify the critical path timing in your design, as shown in Figure 2-28. See Chapter 5 for more information on how to use the Timing Analyzer.

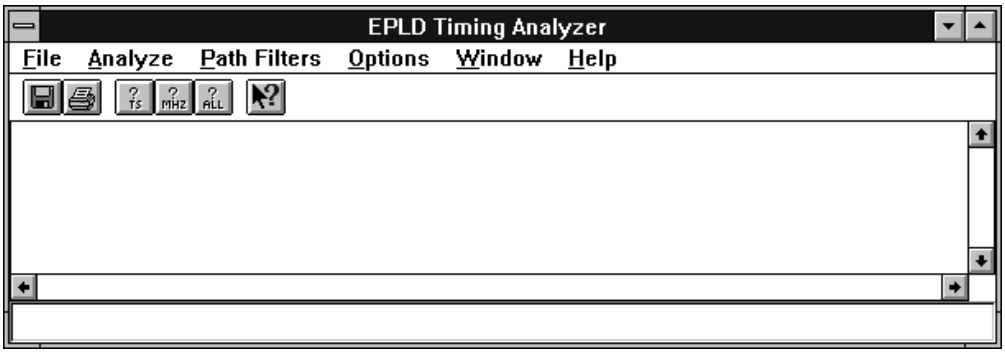


Figure 2-28 Timing Analyzer

Tools — EZTag Programmer

The EZTag Programmer is used to download the configuration data produced by the fitter (.jed file) to the FastFLASH EPLD device via the JTAG interface pins. This allows in-system programming and testing of XC9500 parts. See the *EZTag User Guide* found in the On-line Documents for more information.

Utilities Menu

Use the Utilities Menu to access the various Design Manager utilities as shown in Figure 2-29.

Figure 2-29 The Utilities Menu

Utilities — Report Browser

Select Report Browser to view and edit your design reports; you will

see the Report Browser window as shown in Figure 2-30.

Figure 2-30 The Report Browser Window

Double click on a report icon to view the report. For more information on the Report Browser, see Chapter 6.

Utilities — Command History

Select Command History to view the commands that were previously executed when you implemented your design; you will see the Command History window as shown in Figure 2-31.

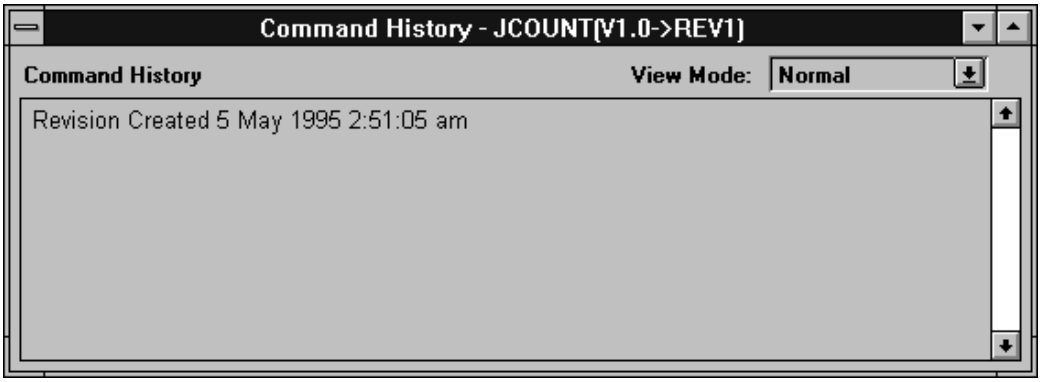


Figure 2-31 The Command History Window

You can view the commands in either Normal mode, which displays only the command names; or Primitive mode, which displays the command name and the associated control parameters.

Utilities — Project Notes

Select Project Notes to document your project; you will see the Project Notes dialog window as shown in Figure 2-32.

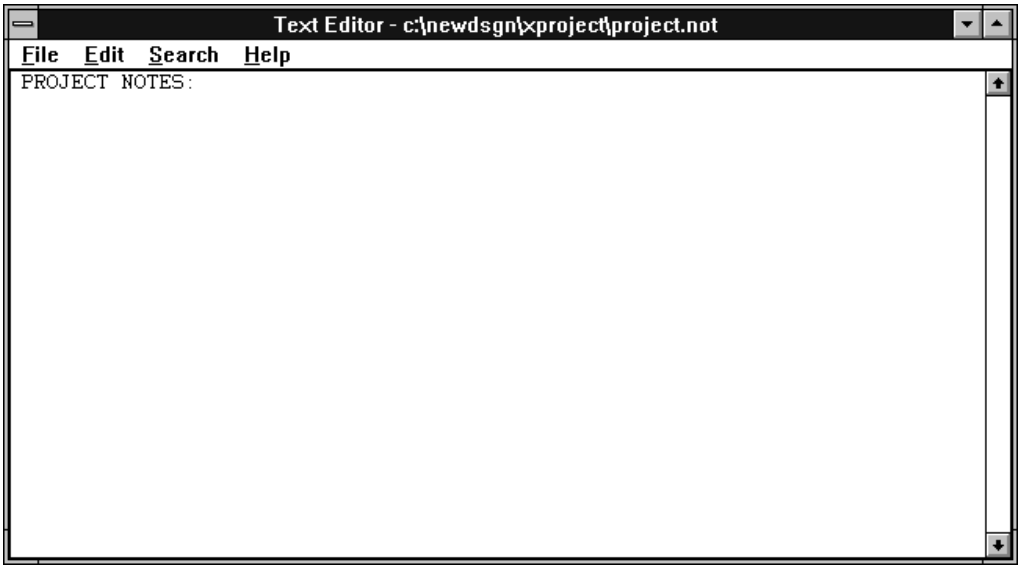


Figure 2-32 The Project Notes Window

You can enter any text into this basic text editor. Project notes are usually used to document the revisions, implementations, and versions of your design.

Utilities — Template Manager

Select Template Manager to create, edit, and delete implementation option templates, which control the processing of your design; you will see the Template Manager dialog window as shown in Figure 2-33.

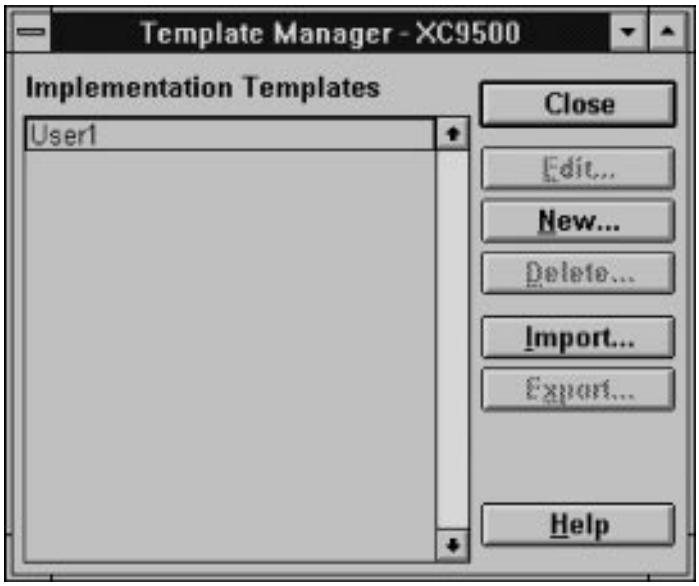


Figure 2-33 The Template Manager Window

Utilities — Template Manager — Close

Click Close to close the Template Manager and return to the Flow Engine dialog window.

Utilities — Template Manager — Edit

After you have highlighted one of the option templates, click Edit to open the following templates for controlling Fitting options, Optimization options, and Resource reservation options.

When you click Edit you will see the Fitting Template, as shown in Figure 2-34.

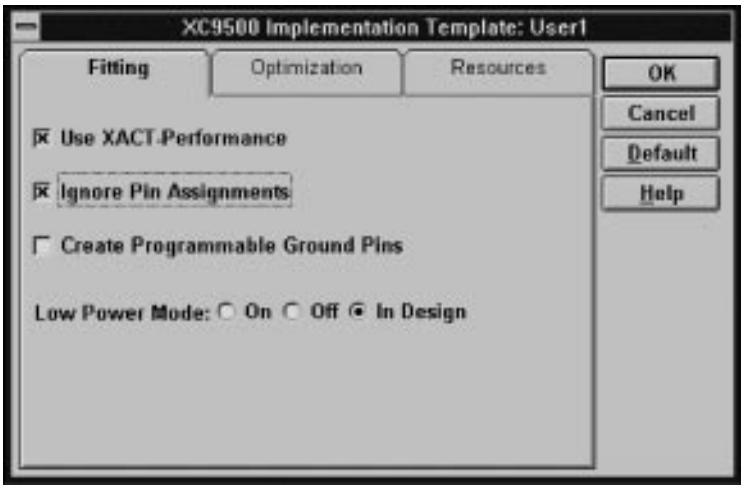


Figure 2-34 The Fitting Options Template

The Fitting Template allows you to control the fitting options, which are set as follows:

- Use XACT-Performance: This indicates that you want the software to use your T-Spec information and perform timing-driven optimization in the fitting of your design. For this option to be useful, you must have previously created a timing constraints file or you must have placed T-Spec information on your schematic. See Chapter 4 for information on using T-Specs.
- Ignore Pin Assignments: This indicates that you do not want to use any pinout information that may be in the design file. This allows the fitter to place pins anywhere.
- Create Programmable Ground Pins: This indicates that you want all unused I/O pads to be actively driven to ground by on-chip circuitry, providing additional grounding pins for the device. See the device data sheet for more information about I/O pads.
- Low Power Mode: Controls device power consumption:
  - On — Set Low Power mode for the entire design.
  - Off — Set high performance (higher power mode) for the entire design.

- In Design — Allow the power mode to be controlled by old-style global attribute in your design. The default is OFF.

Click OK to accept the template, click Cancel to return to the previous menu, click Default to set the default options, or click Help to open the on-line help system.

Click Optimization and you will see the Optimization Template as shown in Figure 2-35.

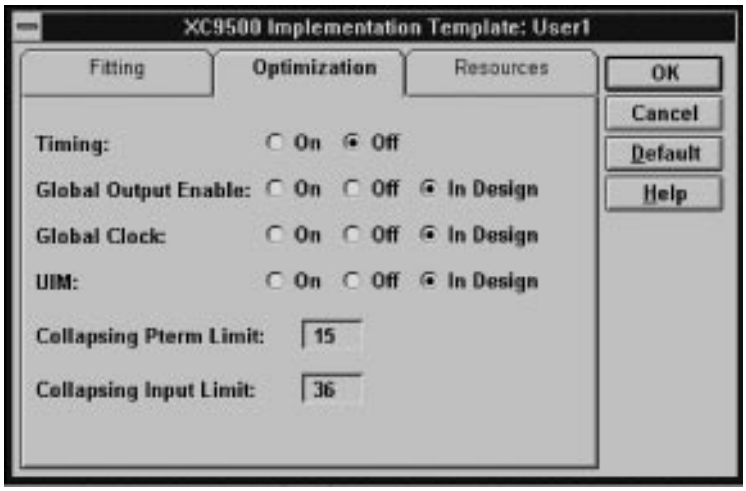


Figure 2-35 The Optimization Options Template

From the Optimization Template you can control the optimization options which are set as follows:

- On — The option is activated for the whole design and corresponding schematic attributes, behavioral commands, or VHDL commands are ignored.
- Off — The option is turned off for the whole design and corresponding schematic attributes, behavioral commands, or VHDL commands are ignored.
- In Design — The option is controlled by old-style global attributes in your design. The default for GTS and GCK optimization is ON.

The options are:

- Timing — Determines if the fitter will try to optimize your design to achieve the best possible timing for your critical paths. If this option is off, the fitter will not spend time optimizing your timing paths, and may require less logic resources to implement your design.

  This timing optimization is controlled independently from the timing-driven optimization of XACT Performance, which was described in a previous section.

- Global Output Enable— Determines if output enable signals can use the dedicated high speed GTS nets.

- Global Clock — Determines if clocks can use the dedicated GCK nets.

Click OK to accept the template, click Cancel to return to the previous menu, click Default to set the default options, or click Help to open the on-line help system.

Click Resources and you see the Resources Template as shown in Figure 2-36.

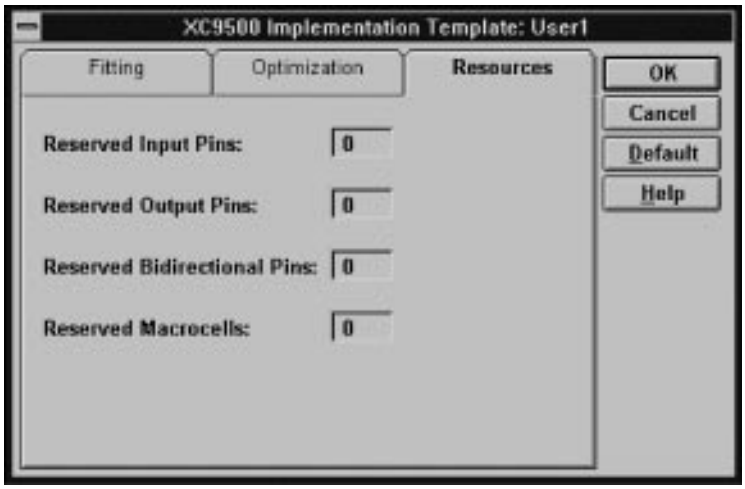


Figure 2-36 The Resource Reservation Template

From the Resources Template you can control the amount of device

resources reserved for future use as follows:

- Reserved Input Pins — Specifies the number of input pins to leave unused.
- Reserved Output Pins — Specifies the number of Output pins to leave unused.
- Reserved Bidirectional Pins — Specifies the number of I/O pins to leave unused.
- Reserved Macrocells — Specifies the number of Function Block macrocells to reserve.

Click OK to accept the Resources template, click Cancel to return to the previous menu, click Default to set the default options, or click Help to open the on-line help system.

Utilities — Template Manager — New

Click New to create a new template and you will see the dialog window as shown in Figure 2-37.

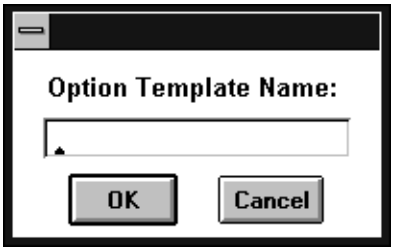


Figure 2-37 The New Template Name Dialog Window

Enter the new template name and click OK; you will see the new name added to the list of option templates. This new template will have default settings that you can change as required.

Utilities — Template Manager — Delete

Click Delete to remove a selected option template from the list. You will see the Delete Confirmation dialog window as shown in Figure

2-38.

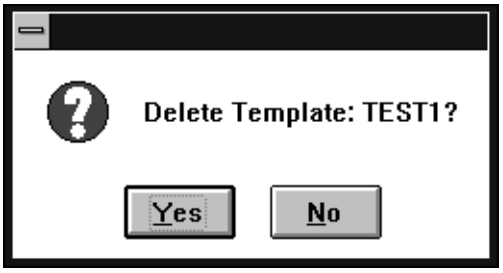


Figure 2-38 Delete Confirmation Dialog Window

Utilities — Template Manager — Import

Use Import to transfer a template file (created by Export as shown below) to a new design.

Utilities — Template Manager — Export

Use export to create a template file for outputting template information to another design.

Utilities — Template Manager — Help

Click Help to bring up the on-line help system.

Help Menu

Use the Help menu to get quick answers to questions about using the Design Manager. You will see the Help menu as shown in Figure 2-39.

Figure 2-39 The Help Menu

Help — Contents

Select contents to view the available help topics and you see the Help window as shown in Figure 2-40. Click on any topic to see the help it contains.

Figure 2-40 Help Contents

Help — Search

Select Search to search for help on any keyword you choose; you will see the search dialog window as shown in Figure 2-41.

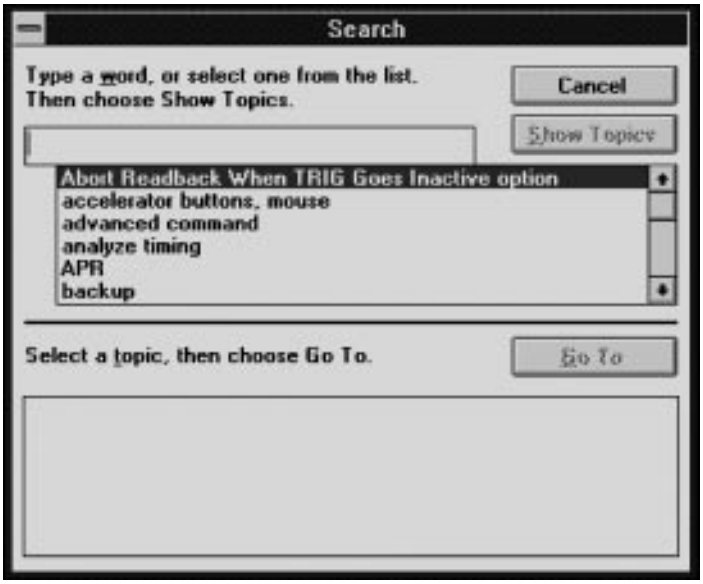


Figure 2-41 Help Search

Help — Tutorial

Select Tutorial to see a step-by-step procedure for using Design Manager.

Help — About Design Manager

Select About Design Manager and you see the Xilinx address, phone number, and software copyright notice.

Using the Flow Engine

The Flow Engine allows you to easily manage the process flow of your design. Select the Flow Engine from the Design Manager Tools menu or by double clicking the Flow Engine icon:

You will see the Flow Engine Window as shown in Figure 2-42.

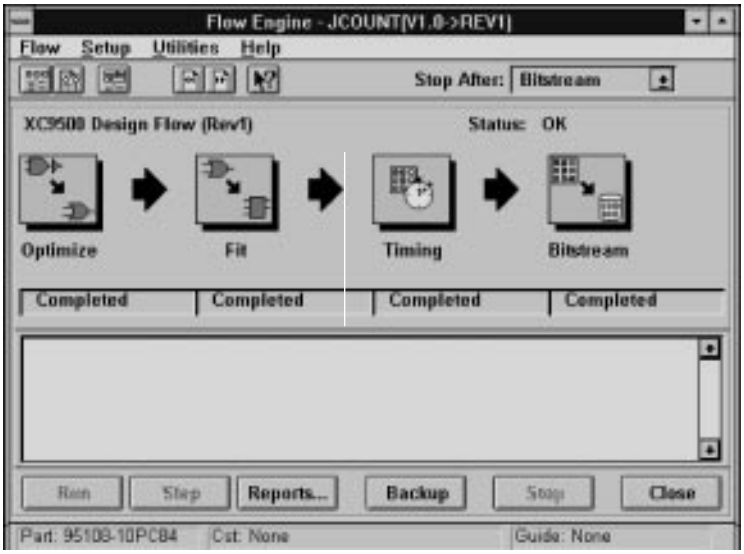


Figure 2-42 The Flow Engine Window

The Process Indicators show you the various software functions that are available for processing your design. You control how far your design is processed by using the Stop After pull down dialog box. For example if you want to optimize and fit your design, but not create a timing simulation file or device programming file, select Stop After Fit. You will see a stop sign indicator verifying where the process will stop.

The Progress Bars show you the status of each processing step and the arrows between each step turn black after the previous step is completed.

Setting Up The Process Flow

The Flow Engine allows you to interact with the process flow in several ways. For example, if you are new to Xilinx software or just want to run a quick “sanity check” on your design, you can simply click run and your design is processed using default fitting parameters. However, if you are an experienced user and want to fine tune your design to get the best possible speed or density, you can control each function in the process. These controls are located under the Setup menu.

Using a Constraints File (to Define T-Specs)

You can create timing specifications, which control the implementation of your design, as described in Chapter 4. These T-Specs may be described in a constraints file (*design_name*.cst). If you want to use a constraints file to control the implementation of your design, you can specify this file in the Flow Engine. The implementation software will then try to fit your design to meet the specified timing requirements. If the specified timing cannot be satisfied, the process flow is terminated.

Using a Guide File (to Re-Use Pinouts)

Each time you fit your design, a guide file is created (*design_name*.gyd) which contains your pinout information. You can re-use this file in subsequent iterations of your design if you want to keep the same pinouts. If you specify a valid guide file name in the Flow Engine window, the pinouts from that file will be used when the design is processed.

Flow Engine Menu Commands

This section describes each Flow engine menu command.

Flow Engine — Flow

The Flow menu contains basic flow control commands as shown in Figure 2-43. Each of these menu commands performs the same function as the corresponding button at the bottom of the Flow

Engine dialog window.

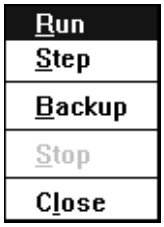


Figure 2-43 The Flow Menu

- **R**un: Select Run to begin the processing of your design. Processing will proceed until the Flow Engine encounters the Stop sign, until the last process is complete, or until a process error has occurred.
- Step: Select Step to process your design one process at a time. After each process is complete, you must click Step again to run the next process.
- Backup: Select Backup to cause the Flow Engine to return to the previous process step as indicated by the process indicator bars. Use this feature to save processing time by backing up to, and re-running, only those steps that you want to change.
- Stop: Select Stop to stop the processing of your design at any time.
- Close: Select Close to close the Flow Engine.

Flow Engine — Setup

Select Setup to specify the Flow Engine options, and you see the menu as shown in Figure 2-44.

Figure 2-44 The Setup Menu

Flow Engine — Setup — Options

Select Options and you see the Design Implementation Dialog

Window as shown in Figure 2-45.

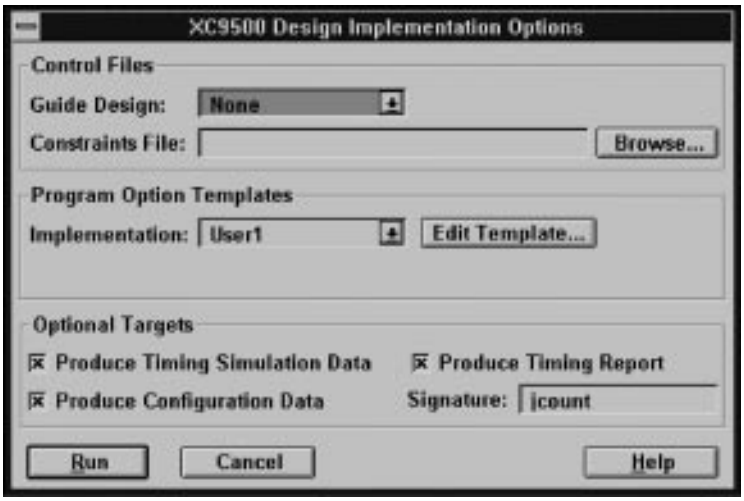


Figure 2-45 The Options Window

See the previous section “Design – Implementation” (Figure 2-16) for more information.

Flow Engine — Setup — Font

Select Font and you see the Font Dialog Window as shown below.

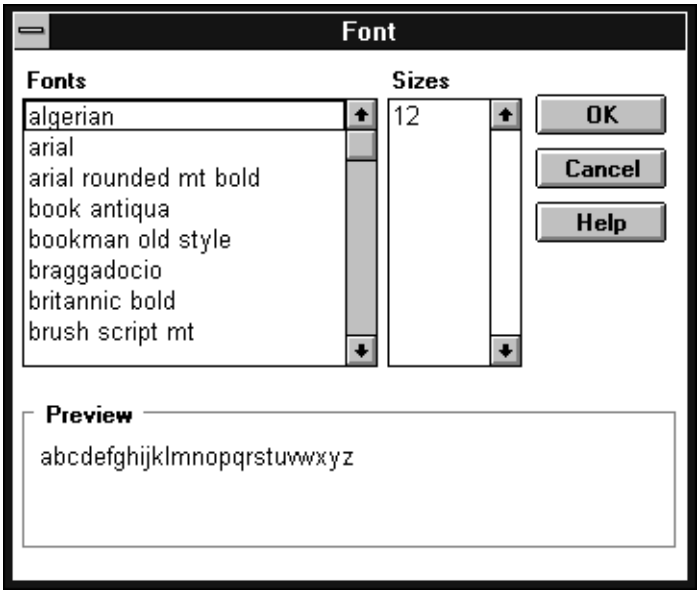


Figure 2-46 The Font Dialog Window

Use this dialog window to select the font type and font size used for displaying messages in the Flow Engine message window.

Flow Engine — Setup — Advanced

Select Advanced and you see the Flow Configuration Dialog Window as shown in Figure 2-47.

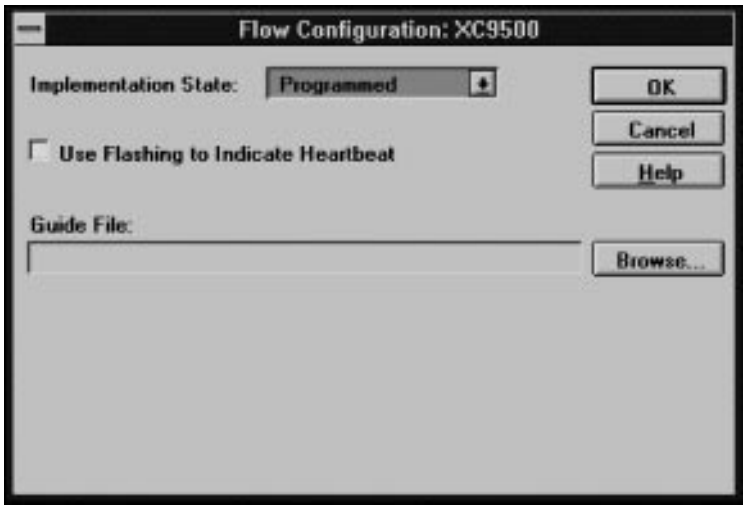


Figure 2-47 The Flow Configuration Dialog Window

From here you can specify the flow control options as follows:

- Implementation State: This allows you to control the state at which the Flow Engine is stopped. The data must already be available in the specified state in order for the Flow Engine to back-up to that state.
- Use Flashing to Indicate Heartbeat: This causes the Process Indicators to flash as the software processes your design.
- Guide File: If you want to use the pinouts from a previous run of your design, specify that guide file here. Click Browse and you see the Open dialog window as shown in Figure 2-48.

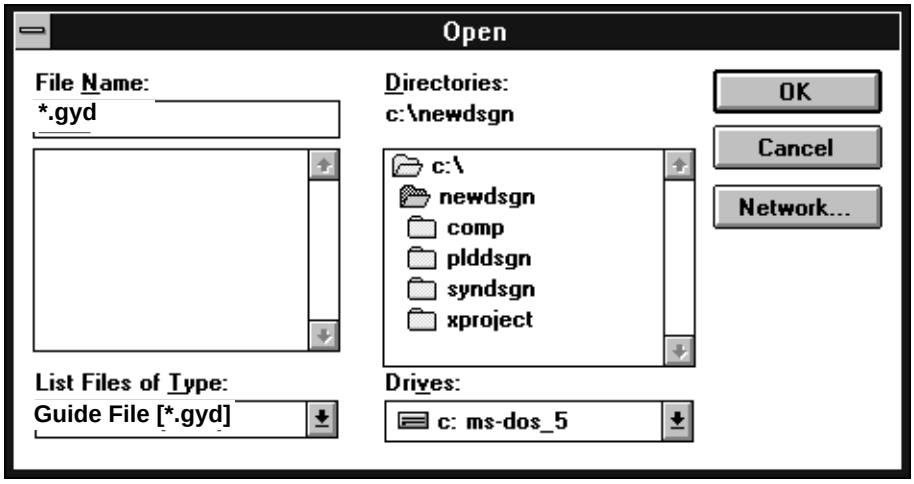


Figure 2-48 The Open Dialog WIndow

Flow Engine — Utilities

Open the Utilities menu and you see the options shown in Figure 2-49. These utilities are the same as those described in the previous section “Design Manager Utilities” (Figure 2-29). See this section for details.

Figure 2-49 The Utilities Menu

Flow Engine — Help

Click Help to bring up the on-line help system.

Chapter 3

Controlling Design Implementation

This chapter shows you how to use the Design Manager to specify fitter guidelines. It also describes the design implementation control options that you can use within behavioral and schematic designs.

Design Implementation Overview

A typical design process is composed of three phases:

1. The fundamental logic design.
2. The implementation of your logic into a target device.
3. The design verification.

Design implementation is controlled during the logic design phase by using schematic attributes and behavioral commands. After your logic design is completed, including any design implementation information, you process your design in the Design Manager environment which provides additional implementation control through Design Manager menu selections.

During design implementation you provide guidelines to the software for:

- Selecting a device or devices to contain your design.
- Placing logic to achieve the most compact design.
- Assigning signals to specific device pin locations.
- Controlling various design optimization options for density or speed improvement.
- Controlling the device power consumption.
- Controlling the slewrate of device output buffers.

- Controlling the initial states of registers.
- Reserving device resources for future design iterations.

The following table shows you the types of design control options and the environments from which they are applied:

Design Control Options	Design Environment		
	Design Manager	Schematic Attributes	Behavioral Commands
Single Device Selection - Manual	X	X	X
Single Device Selection - Automatic	X		
Logic Placement & Pin Assignment	Note 1	X	X
Design Optimization	Note 2	X	X
Device Power Management	Note 3	X	X
Output Buffer Slewrate		X	X
Register Initial State		X	X
Resource Reservation	X		

Note 1: Allows you to ignore values in the design.

Note 2: Allows you to set the global default on or off.

Note 3: Global timing optimization is controlled by the Design Manager.

EPLD Device Selection

During design implementation you must manually select target devices or provide a range of devices from which the software can automatically select the best ones to contain your design. The package options are:

- BG — Ball-Grid-Array.
- PC — Leaded Chip Carrier.
- PG — Pin-Grid-Array.
- PQ — Quad Flat Pak.
- VQ — Very Thin Quad Flat Pak.

Working With Single Devices

This section shows you how to specify a single target device in which to implement your design. You can choose one specific device or you can specify a set of possible target devices from which the software will automatically select the most appropriate one.

Design Manager — Single Device Selection

After you have opened a design, select New Device from the Implementation menu; the device selection menu appears, as shown in Figure 3-1.

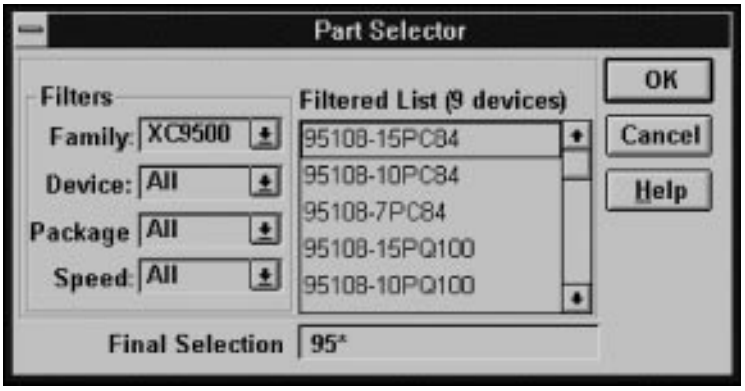


Figure 3-1 Device Selection Menu

From this menu, specify the target device parameters that you want for your design. For example if you choose “All” for all Filters fields the software is free to choose any device in the XC9500 or XC7000 families.

Note: You can also specify a part number in you design source file. This is described in the following sections.

Software Device Selection Criteria

If you select “All” for any device Filters field the software tries to fit your design within the range of possible devices you have selected by using the following selection criteria:

1. First, the software selects the smallest die.

2. Second, the software selects the smallest package.
3. Third, the software selects the slowest available device that meets your specified timing constraints.

The software will continue to try fitting your design into one of the possible range of selected devices until the first usable one is found or until there are no more devices to try.

Manual Logic Placement

The following Design Manager menus contain options that globally affect logic placement:

- Design - Implement
- Utilities - Template Manager

For information on theses menus and their options see Chapter 2.

Note: For most designs you will achieve optimal speed and density if you allow the software to place logic automatically without restrictions. However, in some cases you may want to manually place logic to achieve the optimal density. To achieve optimal timing it is usually best to use T-Specs, as described in Chapter 4, rather than manually placing logic.

Manual Pin Assignment

The software always saves the pinout of your design, in a file named *design_name*.gyd, which can be used later as a guide file if you choose. You specify a guide design by using the Design-Implementation dialog window or by using the Flow Engine-Setup-Options dialog window.

See the *Schematic Design Guide* found in On-line Documentation for information on manual attributes that will assign logic to specific pins.

For most designs you will achieve optimal speed and density if you allow the software to assign pins automatically, without restrictions.

Design Optimization Control

There are a number of optimization control options the software can use before fitting your design. Each of these options is described in this section.

Design Manager — Design Optimization Control

To access the Design Manager global design optimization control options, do the following:

1. Open the DESIGN MANAGER window.
2. Select Design from the menu bar.
3. Select Implement from the Implementation menu, which brings up the Design Implementation Dialog Window, as follows:

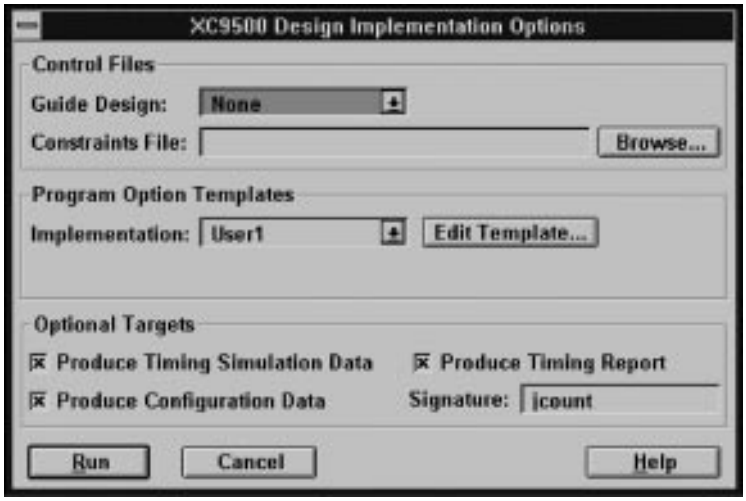


Figure 3-2 Design Implementation Dialog Window

4. Select Edit Template which brings up the Implementation Template Window (for Fitting), as follows:

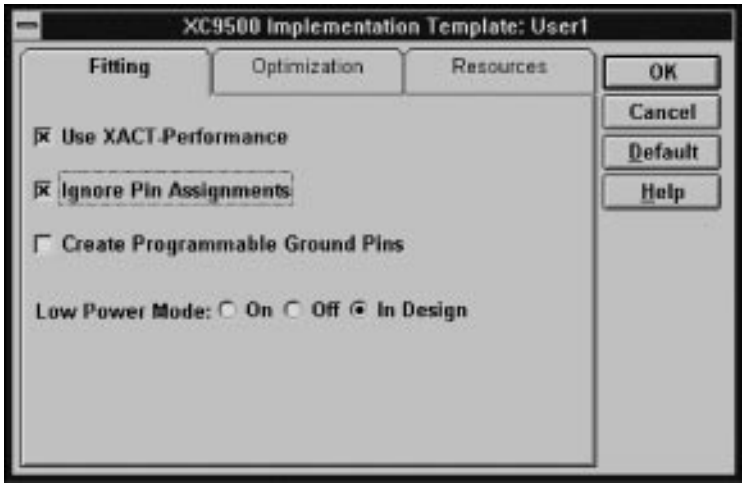


Figure 3-3 Implementation Template — Fitting

5. Select Optimization, which brings up the optimization window, as

follows:

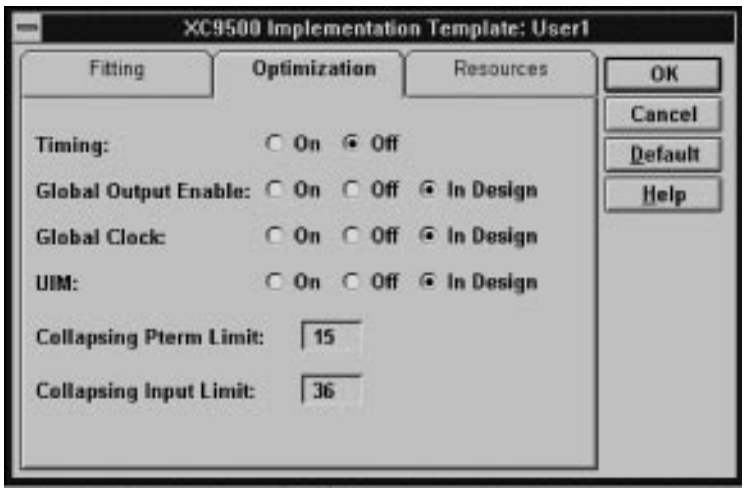


Figure 3-4 Implementation Template — Optimization

From here you can control the global design optimization options.

The Optimization options are described as follows:

Timing

The Timing option determines if the fitter will try to optimize your design to achieve the best possible timing for your critical paths. If this option is off, the fitter will not spend time optimizing your timing paths, and may require less logic resources to implement your design.

This timing optimization is controlled independently from the timing-driven optimization of XACT Performance, which was described in Chapter 2.

Global Output Enable

The Global Output Enable option controls GTS (Global Tri-State) optimization for the entire design. ON is the default.

GTS optimization changes a product-term 3-state signal to an GTS global control signal. This reduces the number of product terms required by each Function Block.

Global Clock

The Global Clock option controls GCK optimization for the entire design. ON is the default.

GCK optimization changes a product-term clock to a GCK global signal, which reduces the number of product terms required by each Function Block.

Power Management

You can control the power consumption and speed of each component in your design. If you select low power, your speed is decreased. If you select high speed, power consumption is increased. These options can be applied to individual components by using Schematic attributes.

Design Manager — Power Management

To access the Design Manager global Low Power Mode option, do the following:

1. Open the DESIGN MANAGER window.
2. Select Design from the tool bar.
3. Select Implement from the Design menu, which brings up the Design Implementation Dialog Window, as shown in Figure 3-5.

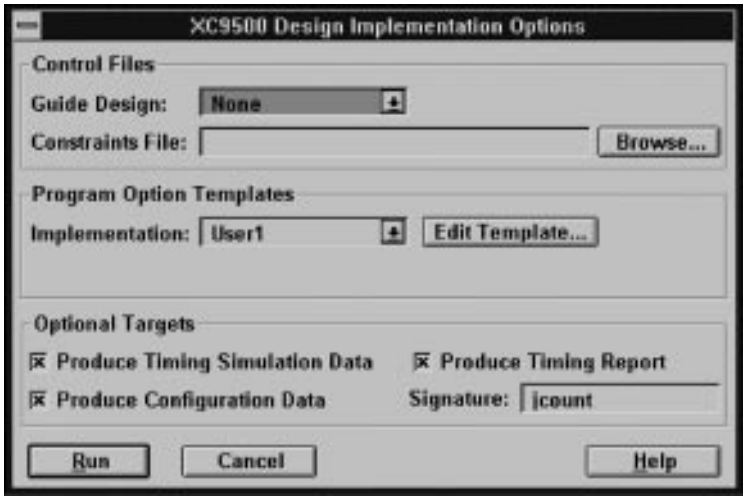


Figure 3-5 Design Implementation Dialog Window

4. Select Edit Template which brings up the Implementation Template Window for Fitting, as follows:

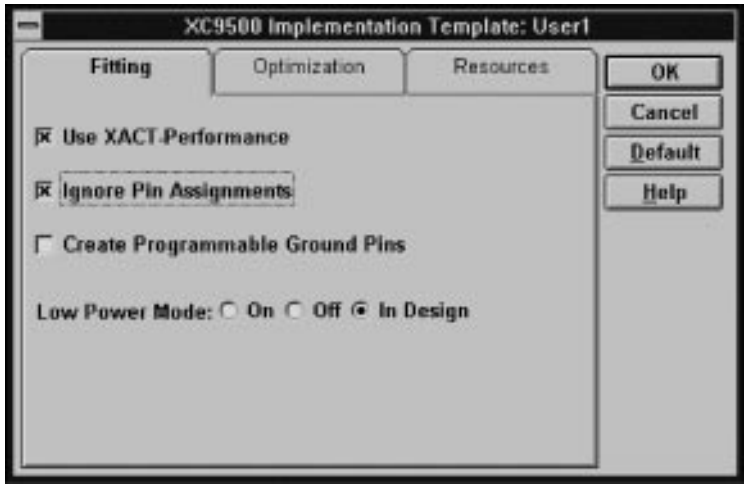


Figure 3-6 Implementation Template — Fitting

From here you can control the Low Power Mode option.

into the FastConnect.

Slewrate Control

You can control the slew rate of your the output buffers in you design by using schematic attributes commands only. See the Schematic Design Guide found in the On-line Documentation for information on using the FAST attribute.

Initial State Control

The INIT=R (for a 0 value) or INIT=S (for a 1 value) component attributes specify the preload value of the registered component to which they are attached. The default preload value for all registers in XEPLD designs is 0 (reset). See the *Schematic Design Guide* found in On-line Documentation for more information on using attributes.

Resource Reservation for Design Iteration

This section shows you how to reserve macrocells for design iteration and device selection.

Design Manager — Resource Reservation

To access the Design Manager Resources options, do the following:

1. Open the DESIGN MANAGER window.
2. Select Design from the tool bar.
3. Select Implement from the Design menu, which brings up the Design Implementation Dialog Window, as follows:

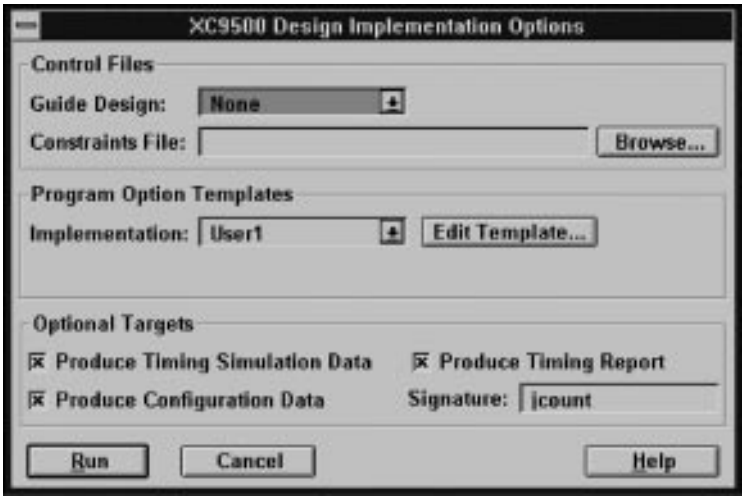


Figure 3-7 Design Implementation Dialog Window

4. Select Edit Template which brings up the Implementation

Window for Fitting, as follows:

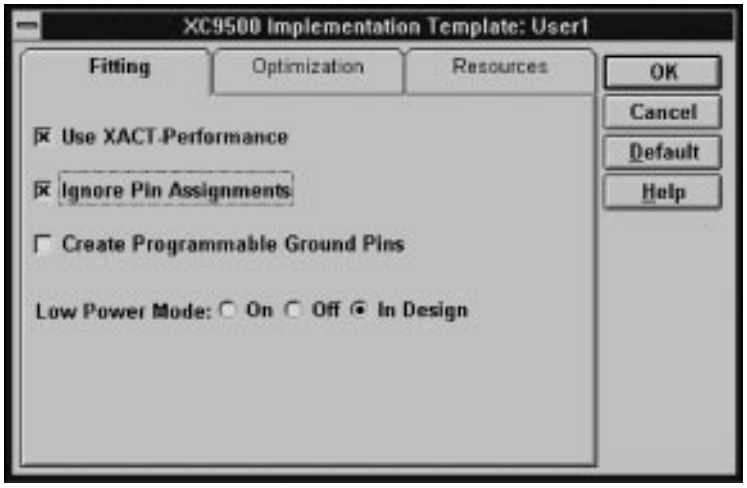


Figure 3-8 Implementation Template — Fitting

5. Select Resources which brings up the following window:

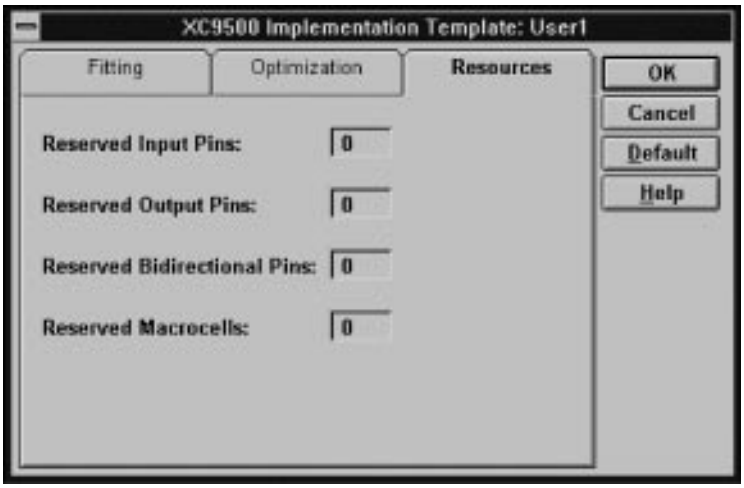


Figure 3-9 Resources Dialog Window

From here you can control the amount of device resources that will be

left unused in each device. If your design uses more than one device, these resource reservations are applied to each device; the resource reservations are not divided among the total number of devices used. The resource reservation options are:

Reserved Input Pins

This specifies the total number of reserved input pins that are reserved in each device.

Reserved Output Pins

This specifies the total number of output pins reserved in each device.

Reserved Bidirectional Pins

This specifies the total number of I/O pins reserved in each device.

Reserved Macrocells

This specifies the total number of macrocells reserved in each device.

Chapter 4

Controlling Design Timing

You can use Timing Specifications (T-Specs) to specify the maximum allowable delay between groups of components in your design. The software then places and routes your design to achieve the timing defined by these specifications. This Xilinx EPLD timing-driven optimization is called XACT-Performance.

T-Specs can be applied directly to a schematic design or they can be specified in a constraints file for behavioral designs. You can then globally enable or disable T-Specs through Design Manager menu options.

Design Manager — Timing Control

To enable global timing-driven optimization (XACT-Performance), do the following:

1. Open the DESIGN MANAGER window.
2. Select Design from the menu bar.
3. Select Implement from the Implementation menu, which brings up the Design Implementation Dialog Window as follows:

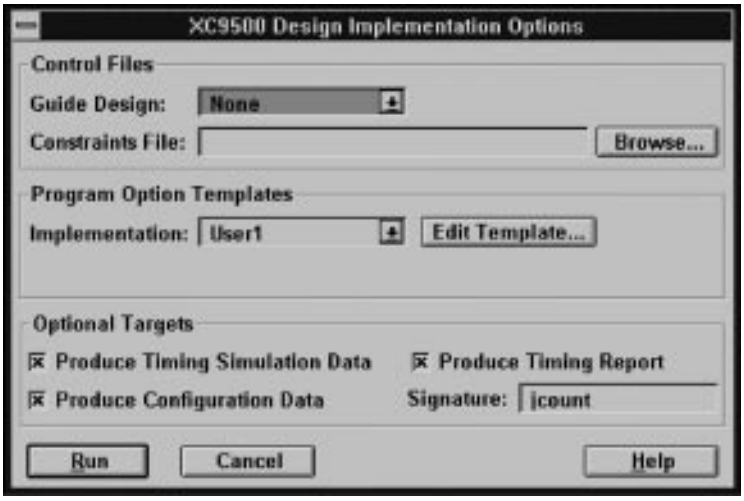


Figure 4-1 Design Implementation Dialog Window

4. Select Edit Template, which brings up the Implementation Template Window for Fitting as follows:

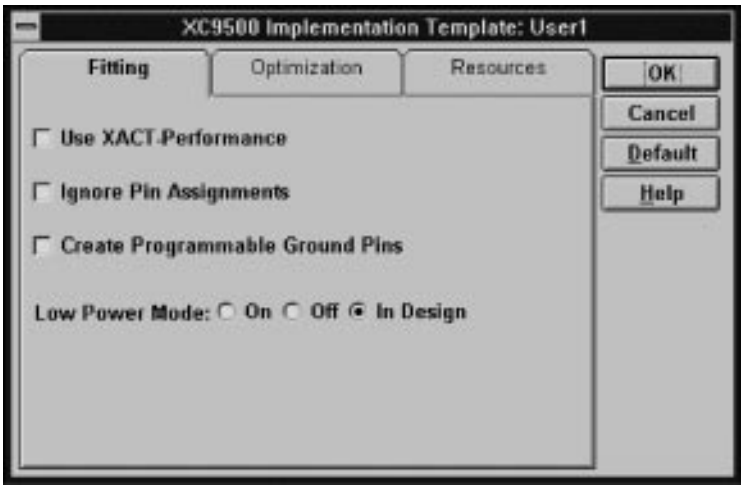


Figure 4-2 Implementation Template — Fitting

5. If you place an X on **Use XACT Performance** the software will use your T-Spec information (if it exists) when fitting your design. If you do not select this option, the software will ignore all T-Spec information.

Schematic — Timing Control

This section shows you how to specify timing control information in schematic designs.

Defining Timing Specifications

Timing specifications are placed on your schematic using a TIMESPEC primitive that contains the Time Spec Attribute Definitions, which control the timing for paths between defined groups of components.

The TIMESPEC Primitive

The TIMESPEC primitive, as illustrated in Figure 4-3, is 30 characters wide and contains TS attribute definitions. Each TIMESPEC primitive can hold up to eight TS attribute definitions. If you want to include more than eight TS attribute definitions, you can use multiple TIMESPEC primitives in your schematic.

Note: Though the TIMESPEC primitive is only 30 characters wide, you can create TS attribute definitions of any length by continuing on the next line.

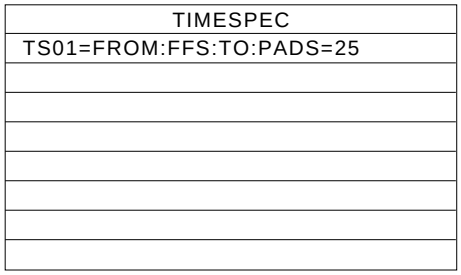


Figure 4-3 TIMESPEC Primitive

How you add a TIMESPEC primitive to your schematic depends on your specific schematic-entry software. Refer to the appropriate Xilinx Interface User Guide for step-by-step instructions.

TIMESPEC Attribute Syntax

The TIMESPEC attribute definitions specify the maximum delay between groups of components. They begin with the letters "TS" and a unique identifier that can consist of letters, numbers, or the underscore character (_). The From-To statement specifies the timing requirements between specific end points. The full syntax is shown as follows:

TS*identifier***=FROM:***group1***:TO:***group2***=***delay*

The parameters *group1* and *group2* can be any of the following:

- Predefined groups consisting of FFS or PADS, which are discussed in the "Using Predefined Groups" section.
- Previously created TNM identifiers, which are introduced in the "Creating Arbitrary Groups Using TNMs" section.
- Groups defined in TIMEGRP symbols, which are introduced in the "Creating New Groups from Existing Groups" section.

The *delay* parameter defines the maximum delay for the attribute, using nanoseconds as the default unit of measurement. Other units of measurement such as MHZ may also be used; see the section "Specifying Time Delay Units" later in this chapter.

Note: Keywords, such as FROM and TO, appear in this document in upper case; however, you can enter them in the TIMESPEC primitive in either upper or lower case.

The following examples show typical TIMESPEC attribute definitions:

```
TS01=FROM:FFS:TO:FFS=30
TS_OTHER=FROM:PADS:TO:FFS=25
```

Defining Timing Path End Points

Specify the start and end points of your timing paths using one of the following methods:

- Refer to a predefined group by specifying one of the corresponding keywords — FFS or PADS.
- Create arbitrary groups within a predefined group by tagging symbols with TNM (pronounced *tee-name*) attributes.
- Create groups that are combinations of existing groups by using TIMEGRP symbols.
- Create groups by pattern matching on signal names.

The following sections discuss each method in detail.

Using Predefined Groups

You can refer to a group of flip-flops, input latches, or I/O pads, by using the corresponding keywords:

Keyword	Group
FFS	Macrocell flip-flops
PADS	input/output pads

These predefined groups represent all symbols of that type. For example the following TS Attribute means that the delay between any two flip-flops must be no greater than 30 ns.

```
TS01=FROM:FFS:TO:FFS=30
```

And the following TS attribute means that the delay between any I/O pad and any flip-flop must be no greater than 25ns.

```
TS_OTHER=FROM:PADS:TO:FFS=25
```

To create groups that are more specific, see the next section, “Creating Arbitrary Groups Using TNMs.”

Creating Arbitrary Groups Using TNMs

A TNM (T-Name or timing name) is a flag that you place directly on your schematic to tag specific pads, flip-flops, or input latches. All symbols tagged with the TNM identifier are considered a group. Place TNM attributes directly on your schematic using the following syntax:

TNM=*identifier*

where *identifier* is a value that consists of any combination of letters, numbers, or underscores. It is usually a good idea to keep the TNM short for convenience and clarity. For example:

```
TNM=grp_1
```

Warning: Do not use reserved words, such as FFS, LATCHES, or PADS, for TNM identifiers.

You can specify as many groups of end points as you need.

You can tag groups of end points by placing TNM identifiers on:

- primitive symbols
- macro symbols
- signals or pins

The method you choose depends on how the path end points are related in your design.

Placing TNMs on Primitive Symbols

You can group individual logic primitives explicitly by flagging each symbol, as illustrated in the following figure:

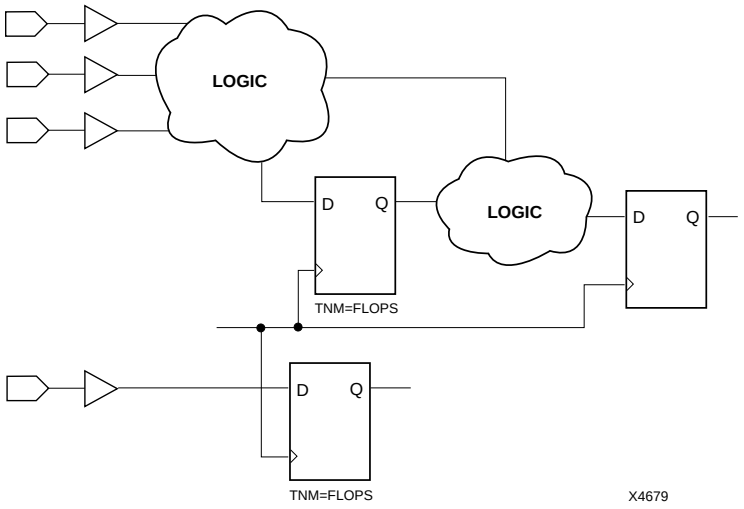


Figure 4-4 Placing a TNM on Primitive Symbols

In Figure 4-4, the flip-flops tagged with the TNM form a group called "FLOPS." The untagged flip-flop is not part of the group.

Note: You cannot use TNMs to group instances of incompatible symbols; for example, it is incorrect to tag a pad and a flip-flop with the same TNM.

Place only *one* TNM on each symbol. If you want to assign more than one identifier to the same symbol, include all identifiers on the right side of the equal sign (=) separated by a semicolon (;), as follows:

```
TNM=joe;fred
```

Placing TNMs on Macro Symbols

When a macro contains only one symbol type, you can place a TNM directly on the macro. If the macro contains only flip-flops, all the flip-flips are identified by the given TNM.

When a macro contains more than one symbol type, use the TNM identifier in conjunction with one of the predefined groups: FFS or PADS as indicated by the following syntax examples:

TNM=FFS:*identifier*
TNM=PADS:*identifier*

If you want to place an identifier on more than one symbol type, separate each symbol type and identifier with a semicolon (;) as illustrated by the following examples:

```
TNM=FFS:FLOPS_1;PADS:OPADS_6
```

Placing TNMs on Signals or Pins to Group Flip-Flops

You can easily group flip-flops by flagging a common input signal, typically either a clock signal or an enable signal. If you attach a TNM to a signal or load pin, that TNM applies to all flip-flops and / or input latches that are reached through the signal or pin. The software traces forward on that path, through any number of gates or buffers, until it reaches a flip-flop or input latch and adds that element to the specified TNM group. This mechanism is called forward tracing.

Placing a TNM on a signal is equivalent to placing that TNM attribute on every load pin of the signal. Use pin TNM attributes when you need finer control.

Figure 4-5 illustrates the use of a TNM on a net that traces forward to create a group of flip-flops. The TNM traces forward to the first two

flip-flops, which form a group called FLOPS. The bottom flip-flop is not part of the group FLOPS.

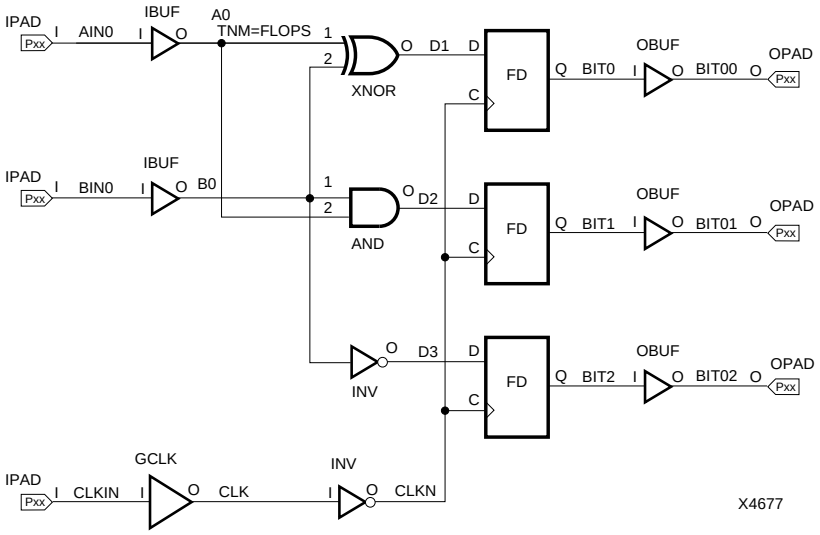


Figure 4-5 Placing a TNM on Signals to Group Flip-Flops

Figure 4-6 illustrates placing a TNM on a clock pin, which traces forward to all three flip-flops and forms the group Q_FLOPS:

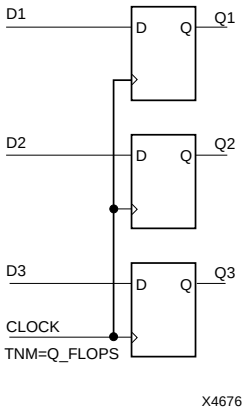


Figure 4-6 Placing a TNM on a Clock Pin to Group Flip-Flops

Creating New Groups from Existing Groups

In addition to naming groups using the TNM identifier, you can also define groups in terms of other groups. You can create a group that is a combination of existing groups by defining a TIMEGRP attribute as follows:

newgroup=*existing_grp1*:*existing_grp2* [:*existing_grp3* . . .]

where *newgroup* is a newly created group that consists of existing groups which were created via TNMs, predefined groups, or other TIMEGRP attributes.

The TIMEGRP Primitive

TIMEGRP attributes reside in the TIMEGRP primitive, as illustrated in Figure 4-7. After you create a TIMEGRP attribute definition within a TIMEGRP primitive, you can use it in the TIMESPEC primitive.

Each TIMEGRP primitive can hold up to eight group definitions and you can use multiple TIMEGRP primitives.

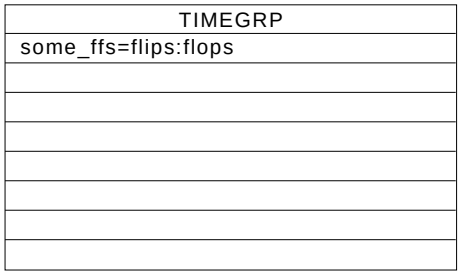


Figure 4-7 TIMEGRP Primitive

You can place TIMEGRP attributes either in the TIMEGRP primitive on the schematic as discussed in this section or in the constraints (CST) file.

You can use TIMEGRP attributes to create groups using the following methods:

- Combining multiple groups into one
- Creating groups by exclusion

The following sections discuss each method in detail.

Combining Multiple Groups into One

You can define a group by combining other groups. The following syntax example illustrates the simple combining of two groups:

```
big_group=small_group:medium_group
```

In this syntax example, small_group and medium_group are existing groups defined using a TNM or TIMEGRP attribute. Within the TIMEGRP primitive, TIMEGRP attributes can be listed in any order; that is, you can create a TIMEGRP attribute that references another TIMEGRP attribute that appears after the initial definition.

Note: A circular definition, as shown below, causes an error.

```
many_ffs=ffs1:ffs2
ffs1=many_ffs:ffs3
```

Creating Groups by Exclusion

You can define a group that includes all elements of one group except the elements that belong to another group, as illustrated by the following syntax examples:

group1=*group2*:**EXCEPT**:*group3*

where *group1* represents the group being defined; *group2* and *group3* can be a valid TNM, predefined group, or TIMEGRP attribute.

As illustrated by the following example, you can specify multiple groups to include or exclude when creating the new group.

group1=*group2*:*group3*:**EXCEPT**:*group4*:*group5*

Note: Do not use reserved words, such as FFS, PADS, RISING, FALLING, or EXCEPT, as group names or TNMs.

Creating Groups by Pattern Matching

You can use wildcard characters to define groups of symbols whose associated signal names match a specific pattern as follows:

group=predefined_group(pattern)

where *predefined_group* can only be one of the following predefined groups — FFS or PADS. A *pattern* is any string of characters used in conjunction with one or more wildcard characters.

Note: When specifying a signal name, you must use its full hierarchical path name so the software can find the signal in the flattened design.

For flip-flops, specify the output signal name. For pads, specify the external signal name.

In XACT-Performance, any place you specify a predefined group, you can specify a predefined group qualified by a pattern as follows:

TS*identifier*=**FROM**:*group(pattern)*:**TO**:*group(pattern)*=*delay*

The following example illustrates creating a group that includes the flip-flops that source signals whose names begin with $1I3/FRED:

```
group1=ffs($1I3/FRED*)
```

The following example illustrates a group that excludes certain flip-flops whose output signal names match the specified pattern:

```
group_23=ffs:EXCEPT:ffs(a*)
```

In this example, group_23 includes all flip-flops except those whose output signal names begin with the letter “a.”

Using Wildcards to Specify Signal Names

The wildcard characters “*” and “?”, enable you to select a group of symbols whose output signal names match a specific string or pattern. The asterisk (*) represents any character string. The question mark (?) indicates a single character.

For example, DATA* indicates any signal name that begins with “DATA,” such as DATA1, DATA22, DATABASE, and so on. The string NUMBER? specifies any signal names that begin with ‘‘NUMBER” and end with one single character, for example, NUMBER1 and NUMBERS, but not NUMBER12.

You can also specify more than one wildcard character. For example, *OR? specifies any signal names that begin with any series of characters followed by “OR” and end with any one character such as NOR1, OR2, and MULTIPLEXOR5.

Multiple Specifications Applied to the Same Path

When you apply more than one From-To specification to the paths between a given pair of end points, the software analyzes all of them. In this case, the software chooses the fastest one, which might not be the specification you want. For example, suppose you have the following timing requirements:

```
TS_ALL=FROM:PADS:TO:FFS:=30
TS_SLOWER=FROM:PADS:TO:SLOW_FFS=40
```

For TS_SLOWER to control the paths to SLOW_FFS, it would have to disable TS_ALL on these paths; however, no specification can disable another. Therefore, the TS_SLOWER paths are specified faster than intended. You can avoid this problem by either of two methods:

- Make sure your broad specifications are always the slowest ones. You could create a FAST_FFS group instead of a SLOW_FFS group, as follows:

  ```
  TS_ALL=FROM:PADS:TO:FFS=40
  TS_FASTER=FROM:PADS:TO:FAST_FFS=30
  ```

- Explicitly exclude slower paths from faster, more general specifications by using a TIMEGRP EXCEPT statement, as explained in the previous section.

  Using this method, you could create a TIMEGRP attribute to define the FAST_FFS group as a complement of the SLOW_FFS group as follows:

  ```
  FAST_FFS=FFS:EXCEPT:SLOW_FFS
  ```

  In the TIMESPEC primitive, you can define two non-overlapping specifications:

  ```
  TS_FASTER=FROM:PADS:TO:FAST_FFS=30
  TS_SLOWER=FROM:PADS:TO:SLOW_FFS=40
  ```

Ignoring Selected Paths

Timing paths that are never used during time-critical operations do not require path analysis and any timing requirement placed on these paths will unnecessarily restrict the software and may result in failure to meet the overall timing requirements. You can use IGNORE to disable any paths that you do not need to control by using the following syntax within the TIMESPEC primitive:

TS*id*=IGNORE

Attaching this to a net or load pin causes the timing analysis software to ignore any paths that include the net or load pin and this makes your design easier to route.

Breaking Combinational Loops

The software cannot perform timing path analysis on combinational loops and therefore it automatically ignores certain connections in order to break the loops. By using IGNORE, you can direct the software to ignore specific nets or load pins, consequently controlling how loops are broken.

Specifying Relative TS Attribute Delays

Instead of specifying time or frequency in a TS attribute definition, you can specify timing as a multiple or division of another TS attribute. This is useful in a system where all clocks are derived from

a master clock; in this situation, changing the timing specification for the master clock changes the specification for all clocks in the system.

Use the following syntax to specify a relative TS attribute delay:

TS*identifier***=***specification***:***reference_TS_attribute***[*,/]***number*

where *number* can be either a whole number or a decimal. The *specification* can be any From-To statement as illustrated by the following examples:

```
FROM:PADS:TO:PADS
FROM:group1:TO:group2
FROM:tnm_identifier:TO:FFS
```

Use "*" to represent multiplication and " / " to represent division. The specification type of the reference TS attribute does not need to be the same as the TS attribute being defined. However, it must not be specified in terms of AUTO or IGNORE.

Examples of specifying relative TS attributes are described as follows. In these cases, assume that the reference attributes were specified as delays (not frequencies)

`TS08=FROM:FFS:TO:PADS= TS05*10`	The paths between flip-flops and pads are placed and routed so their delay is at most 10 times the delay specified in the TS05 attribute.
`TS1=FROM:PADS:TO:PADS= TS07/8`	The paths between input and output pads are placed and routed so their delay is at most one-eighth the delay specified in the TS07 attribute.

Note: When a reference attribute is specified as a frequency, a multiple represents a faster specification; a division represents a slower specification.

You can also specify relative TS attributes in terms of other relative TS attributes. The following example provides an illustration.

```
TS09=FROM:FFS:TO:FFS=50
TS10=FROM:FFS:TO:PADS=TS09*2
TS11=FROM:PADS:TO:PADS=TS10*4
```

Specifying Time Delay Units

Nanoseconds are the default units for specifying delay times in TS attributes. However, after specifying the maximum delay or minimum frequency numerically, you can enter the unit of measure by specifying the following:

- NS for nanoseconds
- MHZ for megahertz
- US for microseconds
- KHZ for kilohertz

The software converts all units to nanoseconds and rounds them to 0.1 ns accuracy.

Example Schematic Using TNMs and TIMEGRPs

TNM identifiers define symbols or groups of symbols that are used in timing specifications. They can also define other groups. Figure 4-8 shows an example of a TNM attribute attached to an individual symbol. In this circuit, the flip-flop D_FF has the attribute TNM=D_FF attached to it.

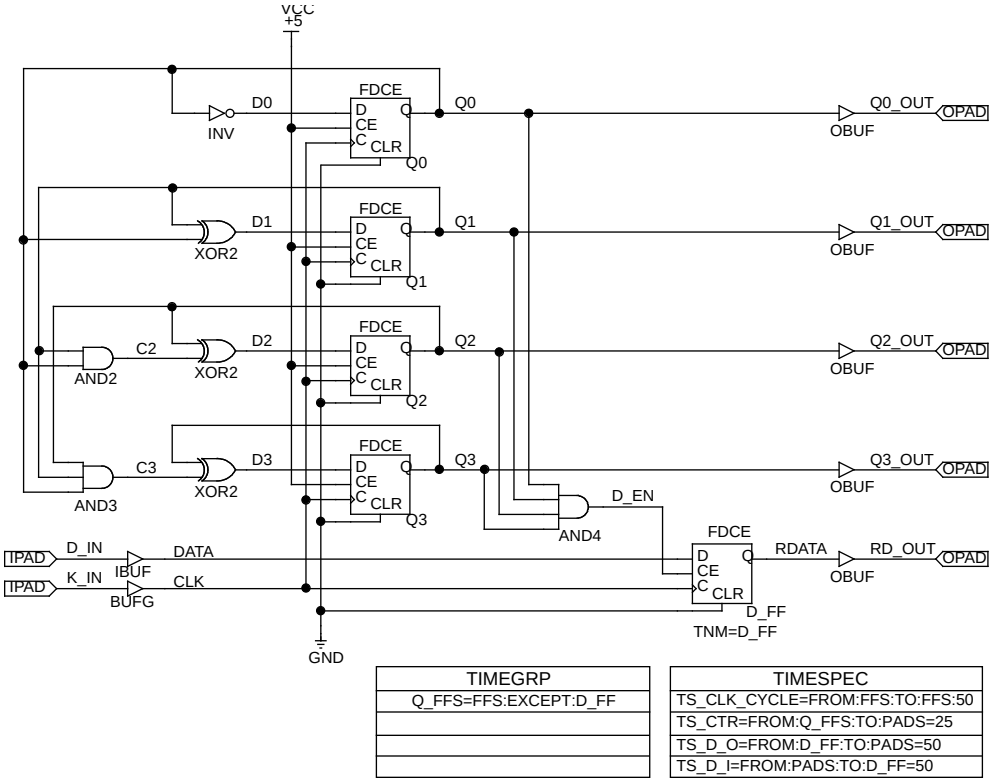


Figure 4-8 Using TNMs and TIMEGRPs in a Schematic

The TIMEGRP symbol contains an attribute that defines a group of flip-flops called Q_FFS, which includes all flip-flops in the schematic except the one labeled D_FF. You can then use the group Q_FFS to create timing specifications in the TIMESPEC primitive. The flip-flop D_FF has its clock enable driven at 1/16th of the clock frequency; therefore, its flip-flop to pad and pad to flip-flop timing specifications are longer than the flip-flop to pad specifications in the Q_FFS group.

Timing Control Syntax Summary

The following sections summarize the XACT-Performance syntax.

TNM Attributes

The following table lists the syntax used when creating TNMs, which you enter directly on the primitive symbol, macro symbol, signal, or load pin.

Flag Type	TNM Attribute Syntax
Symbol Macro symbol	**TNM**=*group1* [;*group2* . . .] **TNM**=*predefined_group*:*group1* [;*predefined_group*:*group2* . . .]
Signal	**TNM**=*group*
Load pin	**TNM**=*group*

TIMEGRP Attributes

The following lists the syntax used within the TIMEGRP primitive.

Group Type	TIMEGRP Attribute Syntax
Combine	*new_group*=*group1*:*group2* [:*group3* . . .]
Exclude	*new_group*=*group1*: [:*group2* . . .]:**EXCEPT**:*group3*: [:*group4* . . .]

TIMESPEC Attributes

The following lists the syntax used for parameters that define TS attributes, which reside in the TIMESPEC primitive.

Spec Type	TIMESPEC Attribute Syntax	TS Flag Required?
From-To	**TS***id*=**FROM**:*group*:**TO**:*group*=*delay*	No
Ignore	**TS***id*=**IGNORE**	Yes
Auto	**TS***id*=*path_type*:**AUTO**	Yes

Timing Control using a Timing Constraints File

For behavioral designs you can use a Constraints file (.CST) to specify timing requirements. The TIMESPEC and TIMEGRP constraints that apply to EPLD designs are described here.

Note: You can also use a constraints file with schematic designs. The Constraints file will override any T-Specs within the schematic.

Constraints File Syntax Conventions

The following conventions are used for .CST file entries:

- Lower-case words are case sensitive and must be lower case.
- [0-9] means a range of numbers between 0 and 9, inclusive.
- [a-z] means a range of characters between AA and Z, inclusive.
- % means “can be composed of.”
- | indicates alternatives, of which only one must be selected.
- { } means that you must choose one of the enclosed items.
- [ ] means that the enclosed items are optional, or that the enclosed items represent a range of possible values.
- *italics* represent variables.

TIMESPEC Constraint Statement Syntax

Use the following syntax for creating EPLD TIMESPEC statements:

TIMESPEC="*timespec_line*";

where *timespec_line* is composed of the following elements:

- *timespec_line* : := *tsIdentifier=timespec_statement*

  Example: from:FFS:to:FFS=10

- *tsIdentifier* : := TS*label*

  Example: TSmux_23

- *timespec_statement* : := {*default_spec* | *delay_spec* | *link* | ignore}

  Example: from:fred:to:joe:=15

- *tlabel* : := *alphanum* [*alphanum*...]

  Example: mux_3

- *alphanum* : := {[a-z] | [A-Z] | [0-9] | _}

  Example: Test_Mux_57

- *from_to* : := from:*group*:to:*group=max_delay*

  Example: from G_1:to:G_8=15

- *dmax_delay* : := {*requirement* | auto}

  Example: auto

- thi : := *float_number*

  Example: 5.5

- *group* : := {*tlabel* | *pattern* | *whole_class*}

  Example: mux_3

- *whole_class* : := {ffs | pads}

  Example: pads

- *max_delay* : := {*requirement* | auto}

  Example: max_delay : := 10.1 mhz

- *pattern* : := *whole_class* (*signame* {:*signame*})

  Example: input*

- *signame* : := {*alphanum* | * | ?} [{*alphanum* | * | ?} ...]

  Example: signame : := input*

- *requirement* : := {*float_number* [*unit*] | *reference*}

  Example: requirement : := 1.5 us

- *unit* : := {ns | us | mhz | khz}

  Example: unit : := mhz

- *reference* : := {*tsIdentifier operator float_number}*

  Example: reference : := TSa_5 * 10.3

- *operator* : := {* | / } (*note:* the * is a multiplier, not a wildcard)

  Example operator : := /

- *float_number* : := *number* [.*number*]

  Example: 45

TIMEGRP Constraint Statement Syntax

Use the following syntax for creating EPLD TIMEGRP statements:

TIMEGRP="*timegrp_line*";

where *timegrp_line* is composed of the following elements, in addition to those described in the previous section:

- *timegrp_line* : := *tlabel=derived_group*

  Example: mux_3=Test_mux_45:except:ff_23

- *derived_group* : := *compound* | *difference*

  Example: mux_3:Test_mux_45

- *compound* : := *group* [:*group*:*group* ...]

  Example: mux_3:Test_mux_45

- *difference* : := *compound*:except:*compound*

  Example: Test_mux_45:except:Reg_4

Creating a Constraints File

You can create a constraints file by using an ascii text editor. Save the file as *file_name*.CST in your design directory. An example of a constraints file is shown as follows:

```
TIMESPEC=”TS02=FROM:FF_1:TO:FF_4=20”;
TIMESPEC=”TS08=FROM:FFS:TO:PADS=TS05*10”;
TIMESPEC=”TS59=FROM:G_1A:TO:G_8C=15”;
TIMESPEC=”TS65=FROM:PADS:TO:PADS=18”;
TIMESPEC=”TS73=FROM:FFS(a*):TO:FFS(b*)=20”;
TIMEGRP=”many_ffs=ffs1:ffs2”;
TIMEGRP=”group1=ffs(ctr*)”;
TIMEGRP=”group2=group1:except:ffs(ctr0)”;
TIMEGRP=”ff1=FFS(a*)”;
```

Figure 4-9 Example .CST File

Chapter 5

Timing Analysis

After you have fitted your design, you can use the Timing Analyzer to find and report the timing of paths through the device. You can select specific paths or general types of paths to examine and you can choose from several report formats.

If you included time specification attributes in your design (also called TimeSpecs or T-Specs), you can use the Timing Analyzer to determine whether the XEPLD fitter was able to meet these specifications.

Timing Analysis Procedure

The typical procedure for using the Timing Analyzer is as follows:

1. Make sure the design you want to analyze is the current design in the Design Manager, then open the Timing Analyzer.
2. Choose the kind of report you want from the Analyzer menu.
3. Use the report window commands to view the report in more detail, save the report, and print the report.
4. (Optional) If having all the paths in your design reported is more information than you need, select filters from the Path Filters menu to determine which types of paths will be analyzed and reported. You can “filter out” paths you are not interested in. Then repeat step 2.
5. (Optional) Select options from the Options menu to fine-tune the analysis even more. Then repeat step 2.

These steps are described in more detail in the following sections.

Opening the Timing Analyzer

Open the Timing Analyzer by double clicking on the Timing Analysis icon in the Tools subwindow of the main Design Manager window. Figure 5-1 shows the icon.

Figure 5-1 Timing Analyzer Icon

The Timing Analysis window appears. The design that is loaded into the Timing Analyzer is the current design established in the Design Manager. To load a different design into the Timing Analyzer, exit to the Design Manager and load a different design from there.

Timing Analysis Window Features

The Timing Analysis window is shown in Figure 5-2.

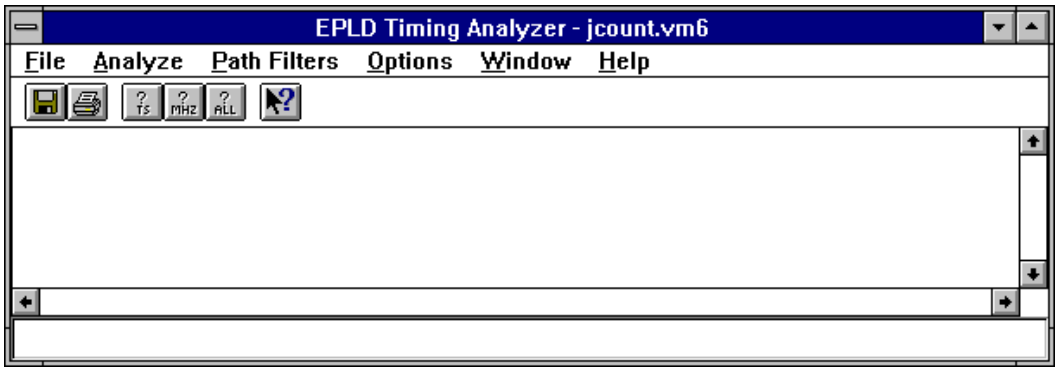


Figure 5-2 Timing Analysis Window

This Window controls the display of report windows generated by commands on the Analyze menu. Because the report windows can be moved and sized independently of the main Timing Analyzer window, the Cascade and Tile commands arrange report windows below and to the right of the main window rather than within it.

However, when you collapse report windows, their icons appear in the main Timing Analyzer window.

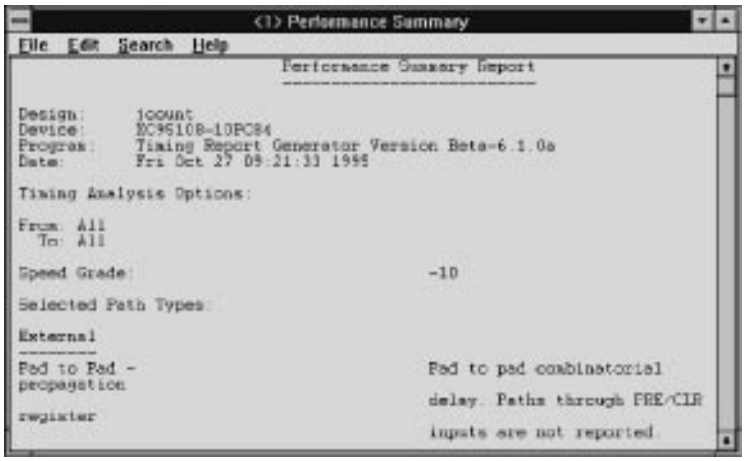
Generating Reports

To generate a report, select one of the commands on the Analyze menu; each of these commands generates a different timing report. If you have previously chosen path filters or other options, the report reflects these choices. After a report is generated, it appears in a separate window from which it can be saved and printed.

Double click on an icon in the main window to expand the report window. The selected report can be saved, printed, deleted, or closed. You can also save and print from the main window file menu by selecting the icon.

Standard Report Header

All Timing Analyzer reports have a header that summarizes the path filters and options that affect the report. Here is an example header for a Performance Summary report:



Performance to Timespecs Report

In the Performance to Timespecs report, timing is analyzed according to how well it matches the T-Specs you included in your design. Make sure the Report Paths Failing TimeSpec command on the Path

Filters menu is ON. The format of this report is exactly the same as that of the Detailed Path Report, except that only paths failing to meet the time specifications assigned to them are listed.

Note: The Performance to Timespecs report shows the source and destination for all paths with T-Specs; the filter for sources and destinations does not apply.

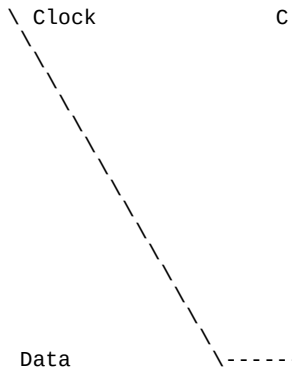
Performance Summary Report

In the Performance Summary report, general indexes of overall performance are reported, for example worst-case pad-to-pad delay, pad-to-setup, clock-to-pad, clock-to-setup, and maximum clock speed. The Select Path Types command partially determines the contents of this report. Here is an example report without the header:

```
Performance Summary:

Clock net 'C' path delays:

Worst case clock pad to output pad delay  :          4.5ns (1 macrocell levels)
(Includes an external input margin of 0.0ns.)
(Includes an external output margin of 0.0ns.)
Clock Pad 'C' to Output Pad 'Q0'                                    (Fast Clock)

Clock to Setup path delay                 :          5.0ns (1 macrocell levels)
Clock to Q, net '$1N5.Q.FFB.REG.Q' to DFF Setup(D) at '$1N5.Q.FFB.D' (Fast Clock)
Target FF drives output net '$1N5.Q'

Clock to Pad path delay                   :          3.0ns (1 macrocell levels)
(Includes an external output margin of 0.0ns.)
Clock to Q, net '$1N5.Q.FFB.REG.Q' to Pad 'Q0'                      (Fast Clock)

Pad to Setup path delay                   :          8.5ns (0 macrocell levels)
(Includes an external input margin of 0.0ns.)
Pad 'CE' to DFF Setup(D) at '$1N5.Q.FFB.D'                          (Fast Clock)
Target FF drives output net '$1N5.Q'

Pad Ending at Clock Pin path delay        :          1.5ns (0 macrocell levels)
(Includes an external input margin of 0.0ns.)
Clock Pad 'C' to DFF Clock Pin at '$1N16'                           (Fast Clock)

Setup to Clock at the Pad                 :          7.0ns (0 macrocell levels)
Data signal 'CE' to DFF D input Pin at '$1N5.Q.FFB.D'
Clock pad 'C' to DFF Clock Pin at '$1N16'                           (Fast Clock)

                        Minimum Clock Period: 5.0ns
                    Maximum Internal Clock Speed: 200.0Mhz
                           (Limited by Cycle Time)

                Estimated Maximum External Clock Speed: 142.8Mhz
                     (Limited by Setup to Clock at the Pad)

--------------------------------------------------------------------------------
                      Clock Pad to Output Pad Delays(nsec)
```

Q0	4.5
Q1	4.5
Q2	4.5
Q3	4.5

Setup to Clock at Pad Delays(nsec)



$1N5.Q.FFB.REG.Q	3.5
$1N6.Q.FFB.REG.Q	3.5
$1N7.Q.FFB.REG.Q	3.5
$1N8.Q.FFB.REG.Q	3.5
C	5.0
CE	7.0

Register to Register Delays(nsec)
(Clock: C)

\ From	$1N1.Q.FFB.REG.Q	$1N2.Q.FFB.REG.Q	$1N3.Q.FFB.REG.Q	$1N4.Q.FFB.REG.Q
$1N5.Q.FFB.REG.Q	3.5	3.5	3.5	3.5
$1N6.Q.FFB.REG.Q	3.5	3.5	3.5	3.5
$1N7.Q.FFB.REG.Q	3.5	3.5	3.5	3.5
$1N8.Q.FFB.REG.Q	3.5	3.5	3.5	3.5
C	5.0	5.0	5.0	5.0
CE	7.0	7.0	7.0	7.0

```
              \     Q     Q     Q     Q
  To           \-------------------------

$1N5.Q.FFB.D       5.0               5.0
$1N6.Q.FFB.D       5.0   5.0
$1N7.Q.FFB.D             5.0   5.0
$1N8.Q.FFB.D                   5.0   5.0
```

Detailed Path Report

In the Detailed Path report, the timing of every path in the design is analyzed in detail, with a breakdown of each segment in each path. The Sort On field of the Report Options command determines the order in which paths are listed.

This report tends to be long, even for fairly simple designs. You may want to use path filters, described in the "Applying Path Filters" section of this chapter, to eliminate report paths not of interest to you.

Here is an example report that has been edited for brevity, without the header:

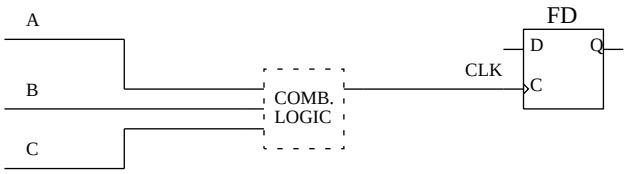
```
Report Only Longest Paths between Points: True

Output will be sorted by increasing path delays.
Logical Path                  Delay Type              Delay        Cumulative
------------                  ----------              -----        ----------
From: C                       -                     :  0.0ns        (0.0ns)
Thru: C/BUF0.OUT              MARGIN                :  0.0ns        (0.0ns)
  To: $1N16                   FCLK BUFFER + FB.DFF.FCLK:  1.5ns     (1.5ns)

Source clock net: $1N16
Worst case clock delay from origin C is 1.5ns
From: $1N5.Q                  FFB.DFF.tCO           :  1.0ns        (1.0ns)
Thru: Q0/OLDNODE              OUTPUT BUFFER         :  2.0ns        (3.0ns)
  To: Q0                      MARGIN                :  0.0ns        (3.0ns)

Source clock net: $1N16
Worst case clock delay from origin C is 1.5ns
From: $1N6.Q                  FFB.DFF.tCO           :  1.0ns        (1.0ns)
Thru: Q1/OLDNODE              OUTPUT BUFFER         :  2.0ns        (3.0ns)
  To: Q1                      MARGIN                :  0.0ns        (3.0ns)

Source clock net: $1N16
Worst case clock delay from origin C is 1.5ns
From: $1N7.Q                  FFB.DFF.tCO           :  1.0ns        (1.0ns)
Thru: Q2/OLDNODE              OUTPUT BUFFER         :  2.0ns        (3.0ns)
  To: Q2                      MARGIN                :  0.0ns        (3.0ns)

Source clock net: $1N16
Worst case clock delay from origin C is 1.5ns
From: $1N8.Q                  FFB.DFF.tCO           :  1.0ns        (1.0ns)
Thru: Q3/OLDNODE              OUTPUT BUFFER         :  2.0ns        (3.0ns)
  To: Q3                      MARGIN                :  0.0ns        (3.0ns)

...
```

```
From: C                         -                       :  0.0ns        (0.0ns)
Thru: C/BUF0.OUT                MARGIN                  :  0.0ns        (0.0ns)
Thru: $1N16                     FCLK BUFFER             :  1.5ns        (1.5ns)
Thru: $1N5.Q                    FFB                     :  1.0ns        (2.5ns)
Thru: Q0/OLDNODE                OUTPUT BUFFER           :  2.0ns        (4.5ns)
  To: Q0                        MARGIN                  :  0.0ns        (4.5ns)


Source clock net: $1N16
Worst case clock delay from origin C is 1.5ns
Destination clock net: $1N16
Worst case clock delay from origin C is 1.5ns
Source and destination clock skew: 0.0ns
From: $1N5.Q.FFB.FBK            -                       :  1.0ns        (1.0ns)
  To: $1N5.Q.FFB.D              FFB.DFF.D               :  4.0ns        (5.0ns)

...

Destination clock net: $1N16
Worst case clock delay from origin C is 1.5ns
From: C                         -                       :  0.0ns        (0.0ns)
Thru: C/BUF0.OUT                MARGIN                  :  0.0ns        (0.0ns)
Thru: $1N16                     FCLK BUFFER             :  1.5ns        (1.5ns)
Thru: $1N5.Q.FFB.FBK            FFB                     :  1.0ns        (2.5ns)
  To: $1N6.Q.FFB.D              FFB.DFF.D               :  4.0ns        (6.5ns)

...

Destination clock net: $1N16
Worst case clock delay from origin C is 1.5ns
From: C                         -                       :  0.0ns        (0.0ns)
Thru: C/BUF0.OUT                MARGIN                  :  0.0ns        (0.0ns)
Thru: $1N16                     FCLK BUFFER             :  1.5ns        (1.5ns)
Thru: $1N7.Q.FFB.FBK            FFB                     :  1.0ns        (2.5ns)
  To: $1N7.Q.FFB.D              FFB.DFF.D               :  4.0ns        (6.5ns)

...

From: CLR                       -                       :  0.0ns        (0.0ns)
Thru: CLR/BUF0.OUT              MARGIN                  :  0.0ns        (0.0ns)
Thru: $1N12                     INPUT BUFFER            :  1.5ns        (1.5ns)
  To: $1N6.Q.FFB.RSTF           UIM + FFB.DFF.S         :  6.5ns        (8.0ns)

Destination clock net: $1N16
Worst case clock delay from origin C is 1.5ns
From: CE                        -                       :  0.0ns        (0.0ns)
Thru: CE/BUF0.OUT               MARGIN                  :  0.0ns        (0.0ns)
Thru: $1N20                     INPUT BUFFER            :  1.5ns        (1.5ns)
  To: $1N6.Q.FFB.D              UIM + FFB.DFF.D         :  7.0ns        (8.5ns)

...

Destination clock net: $1N16
Worst case clock delay from origin C is 1.5ns
From: CE                        -                       :  0.0ns        (0.0ns)
Thru: CE/BUF0.OUT               MARGIN                  :  0.0ns        (0.0ns)
Thru: $1N20                     INPUT BUFFER            :  1.5ns        (1.5ns)
  To: $1N8.Q.FFB.D              UIM + FFB.DFF.D         :  7.0ns        (8.5ns)
```

Check for Asynchronous Logic

The Check for Asynchronous Logic command lists locations of signals that are possibly asynchronous and the product-term clock signals that control them. Two types of paths are considered possibly asynchronous:

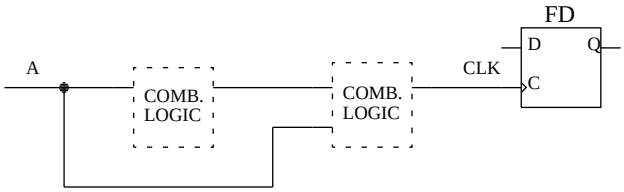
- A clock pin with multiple origins, as in the following example:



In this case, the following statement appears in the report:

```
clock pin CLK has multiple origins A, B, C:
possible asynchronous.
```

- A clock pin with multiple paths leading to it, as in the following example:



In this case, the following statement appears in the report:

```
clock pin CLK has multiple paths to its origin
A: possible asynchronous.
```

Show Clocks

The Show Clocks command lists the clock signals in the design.

Show Settings

The Show Settings command lists the Path Filter and Options settings you chose during this session of the Timing Analyzer.

Report Window Commands

After you select any command on the Analyze menu, the requested report appears in a new window. For example, here is a Performance Summary report window.

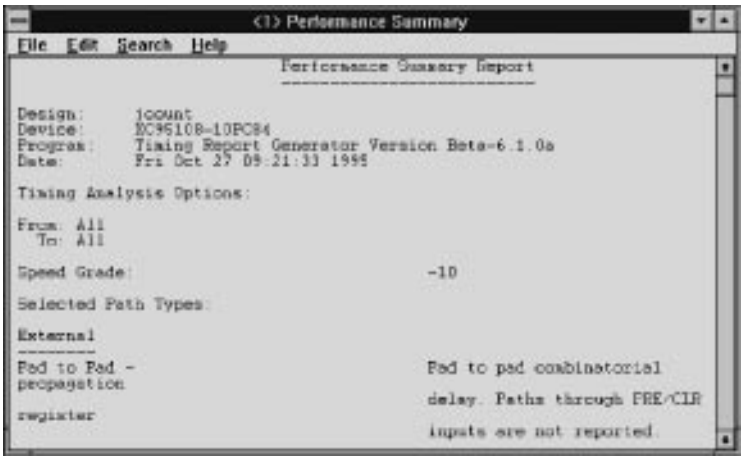


Figure 5-3 Report Window

The Window menu in the main Timing Analyzer window controls the display of report windows generated by commands on the Analyze menu. Because the report windows can be moved and sized independently of the main Timing Analyzer window, the Cascade and Tile commands arrange report windows below and to the right of the main window rather than within it.

However, when you collapse report windows, their icons appear in the main Timing Analyzer window.

Collapsing the main window collapses the report windows as well. Restoring the main window also restores the report windows.

Each report window has its own set of menu commands, which allow you to view the report in more detail, save the report, and print the report. The report window commands are as follows:

- File-Save As — Opens a file browser window and lets you save the report file.

- File-Print — Sends the report to the default printer. No dialog box is presented.
- Edit-Copy — Saves the selected text to the clipboard so you can copy it into another text file or document.
- Edit-Select All — Allows you to select all the text in the report at once. To copy the entire report, use this command followed by the Copy command.
- Edit-Word Wrap — When this option is on (the default), lines too long to fit in the window wrap to the next line. When this option is off, lines do not wrap regardless of length. Turning word wrap off is useful for viewing tables.
- Search-Find — Presents a dialog box that allows you to search for text. You can specify case sensitivity or whole word only matching, and you can search forward or backward.
- Search-Find Next — Searches for the text you specified last time you used the Find command.
- Zoom-Zoom In — Expands the text size and shows a smaller area of the report.
- Zoom-Zoom Out — Shrinks the text size and shows a larger area of the report.
- Zoom-Zoom Normal — Changes the text to its original size.

To close the report window, select the File-Exit command.

Applying Path Filters (Optional)

The Path Filters menu offers the following choices, which enable you to eliminate paths from the report and examine only the kinds of paths of greatest interest to you. By default, if you do not use any filters, all paths are included in whichever report you choose.

The Options menu commands, which are described in the "Selecting Additional Options" section of this chapter, also refine the contents of the reports you select.

Report Paths Failing Timespec

Use the Report Paths Failing TimeSpec command to view timing information for signals that do not meet your timing specifications. This command includes in the report paths that are slower than the time specification you assigned.

When this command is on, a check appears to the left of the command in the menu. The default setting is ON.

Report Paths with No Timespec

Use the Report Paths with No TimeSpec command to view timing information for all signals, including paths having no assigned time specification.

When this command is on, a check appears to the left of the command in the menu. The default setting is ON.

Ignore Timespecs

The Ignore TimeSpecs command deletes selected T-Specs from the report. Use this command to filter out signals that are not timing-critical. By default, all T-Specs are included.

When you select this command, the Ignore TimeSpec window appears as shown in Figure 5-4.

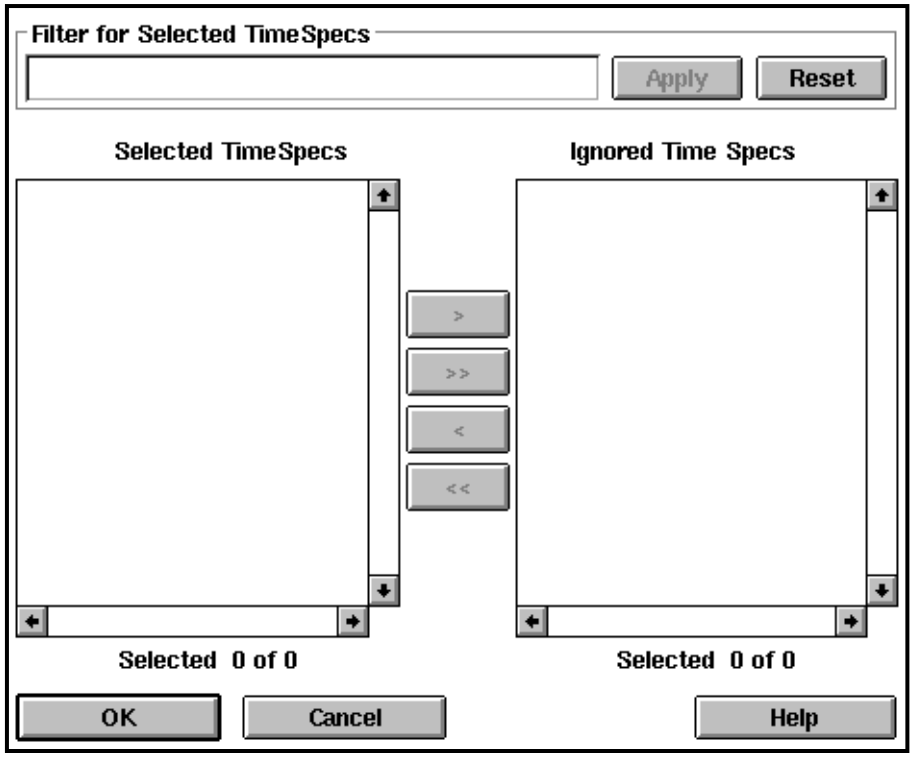


Figure 5-4 Ignore TimeSpec Window

Follow these steps to delete specific T-Specs from the report:

1. Type a name, partial name, or name with a wildcard in the Filter for Selected Timespecs field to select a subset of the T-Specs in the design. The ? is a single-character wildcard; the * is a multiple-

character wildcard. Select the Apply button to apply the filter. To select all T-Specs, leave this field blank or select the Reset button followed by the >> button. This filtering step is optional.

Note: The Reset button clears the current filter and includes all the T-Specs in the Selected TimeSpec list except the T-Specs you have already moved to the Ignored TimeSpec list.

2. To move a T-Specs into the Ignored TimeSpec list, select the T-Specs from the Selected TimeSpec list and select the > button. To move a all T-Specs into the Ignored TimeSpec list, use the >> button.
3. To move a T-Specs back into the Selected TimeSpec list (so it is NOT ignored), select the T-Specs from the Ignored TimeSpec list and select the < button. To move all T-Specs back into the Selected TimeSpec list, use the << button.

Note: After you move T-Specs to the Ignored TimeSpec list, the T-Specs remain highlighted so you can undo the move with a single mouse click on the < button.

4. When your Selected TimeSpec list and Ignored TimeSpec list are organized as you want them, select the OK button.

Select Sources and Select Destinations

The Select Sources and Select Destinations commands include paths having the sources and destinations you specify in the report. These sources and destinations can be nets, flip-flops, pads, clocks, or macrocells. The following figure shows the source and destination of a typical pad to setup path.

Figure 5-5 Source and Destination

By default, all pads and registers are included as sources and destinations. You can add sources or destinations to the included list or select sources or destinations you want to be removed from the included list.

When you select this command, the Select Sources or Select Destinations window appears. These two windows have exactly the same functions; the only difference is that Select Sources lists design elements that can be beginnings of paths and Select Destinations lists design elements that can be ends of paths.

Note: The Performance to Timespecs report shows the source and destination for all paths with T-Specs; the filter for sources and destinations does not apply.

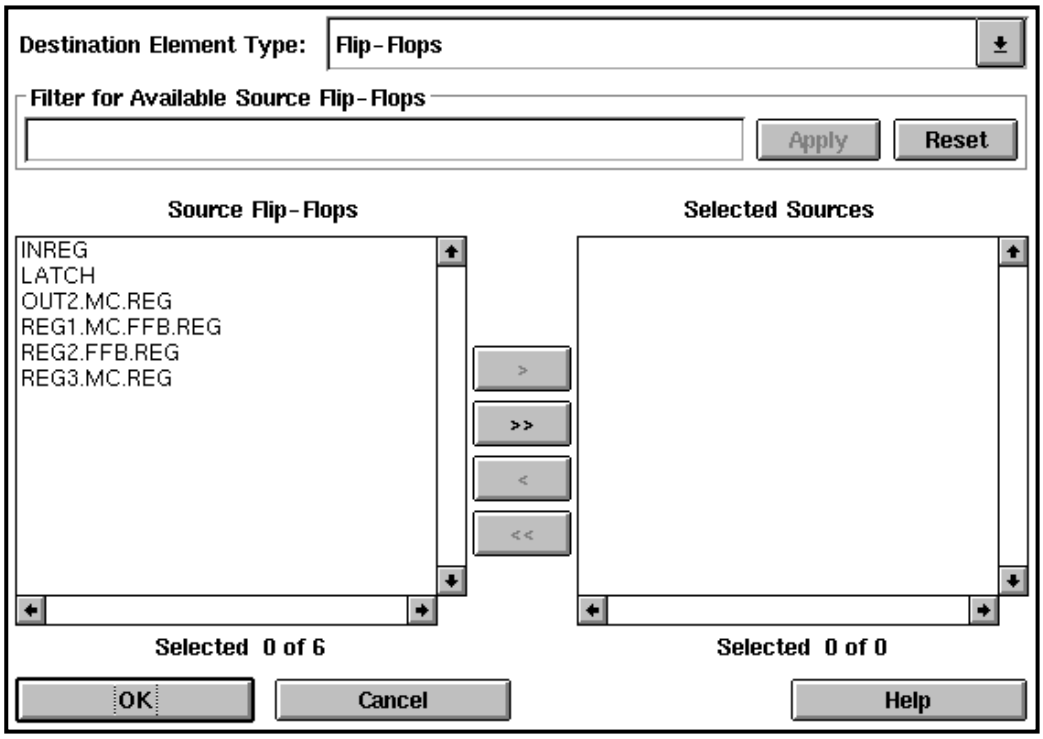


Figure 5-6 Select Sources Window

Follow these steps:

1. Select the type of source or destination element you are interested in from the Source Element Type or Destination Element Type field at the top of the window. Choices are All, Flip-flops, Pads, Clocks, Nets, or Macrocells. The All option, which is the default, means all pads and flip-flops, not all elements.

Note: If you select All, this text appears in the Source Elements or Destination Elements list: `*** All Sources***` or `***All Destinations***`. If you add this text to the Selected Sources or Selected Destinations list using the > button, you cannot add additional elements to the Selected Sources or Selected Destinations list. To add other types of elements, first select the All text in the Selected Sources or Selected Destinations list and click on the < button, then add the elements you want.

2. Type a name, partial name, or name with a wildcard in the Filter for Available Elements field to select a subset of the elements in the design to be excluded. The ? is a single-character wildcard; the * is a multiple-character wildcard. Select the Apply button to apply the filter. To select all elements, leave this field blank or select the Reset button followed by the >> button.

Note: The Reset button clears the current filter and includes all the elements in the Available Elements list except the elements you have already moved to the Source Elements or Destination Elements list.

3. The Source Elements or Destination Elements list contains the elements that will be included in the report. To remove an element from this list, select it and select the < button. The element moves to the list on the left.

   The > button moves an element from the list on the left back to the Source Elements or Destination Elements list. The >> and << buttons move all elements in one list to the other list.

Note: After you move elements to the Source Elements or Destination Elements list, the elements remain highlighted so you can undo the move with a single mouse click on the < button.

4. Select OK when your sources or destinations list is finished.

Select Path Types

The Select Path Types command specifies the types of paths to include in the report, for example, “clock to setup.” By default, all path types are listed.

When you select this command, the Select Path Type window appears.

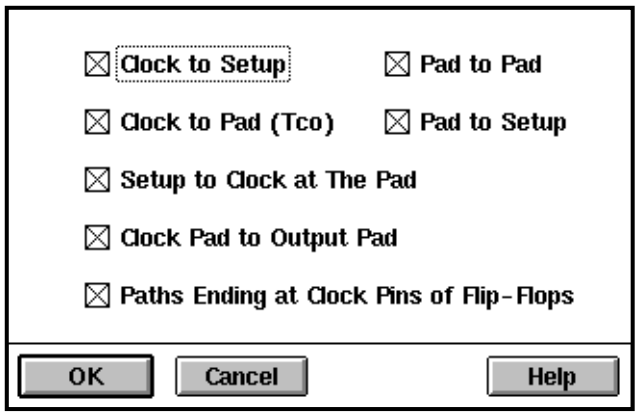


Figure 5-7 Select Path Type Window

If you wish to eliminate some path types from the report, click on them to remove the X’s from their boxes.

The path types are defined as follows:

- Clock to Setup — Register to register cycle time, including clock to output and setup delay.

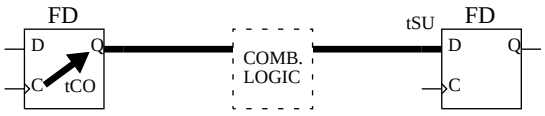


Figure 5-8 Clock to Setup Path

- Pad to Pad — Combinational pad to pad delay.

Figure 5-9 Pad to Pad Path

- Clock to Pad — Delay from the register clock input to the output pad.

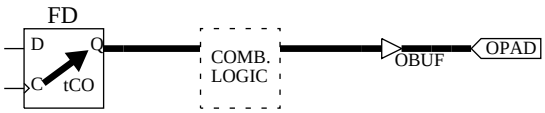


Figure 5-10 Clock to Pad Path

- Pad to Setup — Data path delay from the pad to the register data input. Includes the register setup time.

Figure 5-11 Pad to Setup Path

- Setup to Clock at the Pad — Setup time of data at the pad-to-clock at the pad. This path type includes only global clocks and product term clocks driven directly from input pads. If the data input is signal A and the clock input is signal CLK, the timing calculation for this type of path is as follows:

  Max(A to D) – Min(CLK to C)

  Max and Min are maximum and minimum propagation delays through the combinational logic.

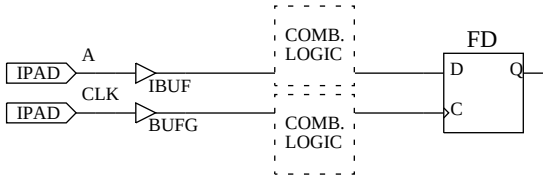


Figure 5-12 Setup to Clock at the Pad Path

- Clock Pad to Output Pad — Clock pad to output pad propagation delay. The clock can be a global or product term clock.

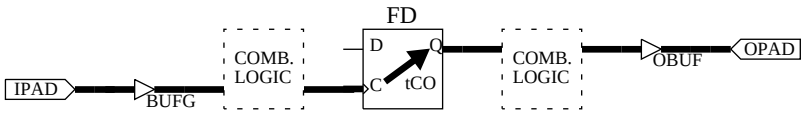


Figure 5-13 Clock Pad to Output Pad Path

- Paths Ending at Clock Pins of Flip-Flops — Delay from clock pad to register clock input. The clock can be a global or product term clock.

Figure 5-14 Path Ending at the Clock Pin of a Flip-Flop

Include or Exclude Paths with Nets

The Include and Exclude Paths with Nets commands are not opposites and can be used together.

The Include Paths with Nets command includes in the report only the paths that pass through at least one of the nets you specify; all other paths are excluded. By default all nets are included, so all paths are included in the report.

The Exclude Paths with Nets command excludes from the report the paths that pass through at least one of the nets you specify. Paths not

passing through any of the selected nets are not necessarily included, however. By default no nets are excluded.

You can use both of these commands together. First use Include Paths with Nets to select the set of paths you are interested in, then use Exclude Paths with Nets to refine this set of paths. A path that passes through both an included net and an excluded net is excluded.

When you select one of these commands, the Include Paths with Nets or Exclude Paths with Nets window appears. These two windows have the same layout of lists and buttons. You select paths to include or exclude in the same way; the only difference between these two commands is the results.

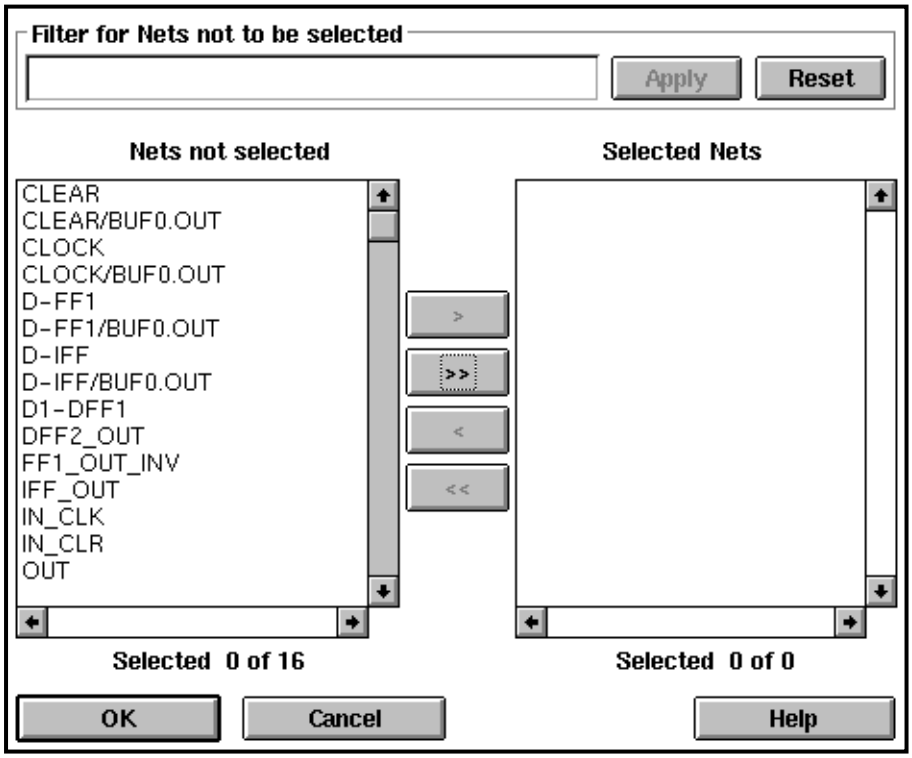


Figure 5-15 Include Path with Nets Window

Follow these steps:

1. Type a name, partial name, or name with a wildcard in the Filter for Nets not to be selected field to select a subset of the nets in the design. The ? is a single-character wildcard; the * is a multiple-character wildcard. Select the Apply button to apply the filter. To select all nets, leave this field blank or select the Reset button followed by the > button.

Note: The Reset button clears the current filter and includes all the elements in the Nets not selected list except the elements you have already moved to the Selected Nets list.

2. Select nets from the Nets not selected list and move them to the Selected Nets list by selecting the > button.

   To move a net back to the Nets not selected list, use the < button. The >> and << buttons move all nets in a list to the other list.

Note: After you move elements to the Nets not selected or Selected Nets list, the elements remain highlighted so you can undo the move with a single mouse click on the < button.

3. Select OK when your list of nets is as you want it.

Break Logic Loops

The Break Logic Loops command specifies feedback loops to be broken in the report. When you select this command, the Break Logic Loops window appears.

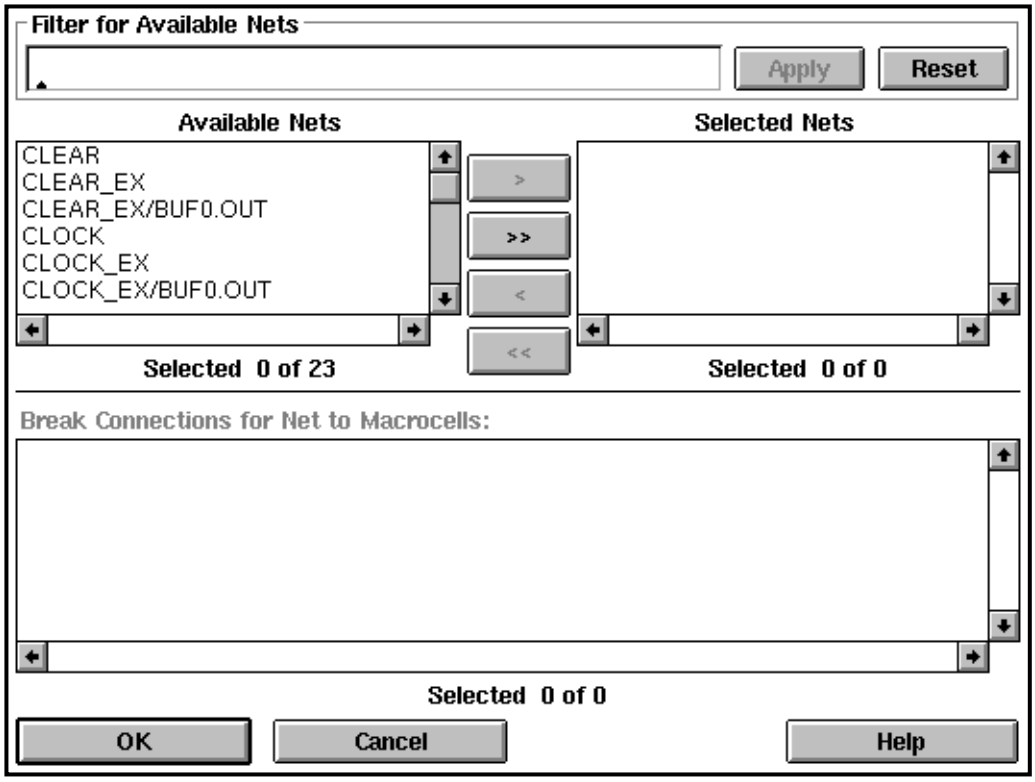


Figure 5-16 Break Logic Loops Window

Follow these steps:

1. Type a name, partial name, or name with a wildcard in the Filter for Available Nets field to select a subset of the nets in the design. The ? is a single-character wildcard; the * is a multiple-character wildcard. Select the Apply button to apply the filter. To select all nets, leave this field blank or select the Reset button followed by the > button.

Note: The Reset button clears the current filter and includes all the elements in the Nets not selected list except the elements you have already moved to the Selected Nets list.

2. Select nets from the Available Nets list and move them to the Selected Nets list by selecting the > button.

   To move a net back to the Nets not selected list, use the < button. The >> and << buttons move all nets in a list to the other list.

Note: After you move elements to the Nets not selected or Selected Nets list, the elements remain highlighted so you can undo the move with a single mouse click on the < button.

3. After you select a net, the macrocells fed by that net appear in the Break Connections for Net to Macrocells list with check marks on the left. Select the macrocell(s) to which the net does not feed back to remove the checks. If you remove all macrocells, the net is removed from the Selected Nets list.
4. Select another net and repeat the previous step.
5. Select OK when your list of nets and macrocells indicating feedback loops is as you want it.

Note: To specify a feedback path for a net, you must specify (leave checked) only the macrocell(s) to which the net feeds back. If you specify all macrocells fed by the net, all load pins of that net are broken, including those that are not feedback paths. It is a good idea to display your design file in another window so you can see the feedback paths and macrocells clearly.

For example, in the following figure, A is a signal that feeds back to Macrocell 1. If you break all the macrocells fed by signal A, the load pin of A that goes to Macrocell 2 is broken in addition to the signal that goes to Macrocell 1.

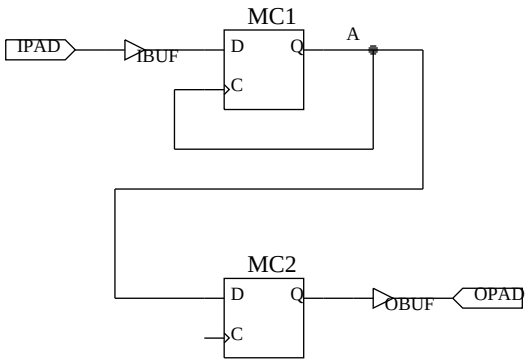


Figure 5-17 Break Logic Loops Example

Reset Path Filters

The Reset Path Filters command restores default path filters. In general, all paths are included in the report by default. More specifically, default filters are as follows:

- Report Paths Failing TimeSpec is ON.
- Report Paths with No TimeSpec is ON.
- Ignore TimeSpecs has no T-Specs selected, which means all paths are included.
- Select Sources includes all pads and flip flops.
- Select Destinations includes all pads and flip flops.
- Select Path Types includes all path types.
- Include Paths with Nets includes all nets.
- Exclude Paths with Nets includes no nets.
- Break Logic Loops includes no feedback paths, which means all feedback paths are included.

Selecting Additional Options (Optional)

The commands on the Options menu allow you to fine-tune your analysis.

Set Speed Grade

The Set Speed Grade command re-evaluates the timing based on a selected speed grade. When you select this command, the Set Speed Grade window appears.

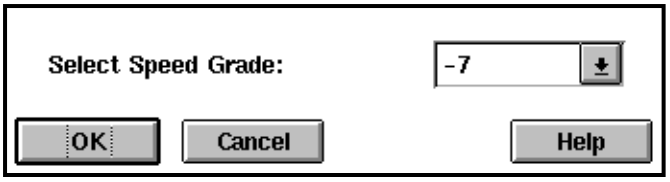


Figure 5-18 Set Speed Grade Window

The speed grades you can select are different for each device.

Set Delay Margins for I/O

The Set Delay Margins for I/O command adds the specified delays to pads to simulate delays due to lines on the PC board.

When you select this command, the Set Delay Margins for I/O window appears.

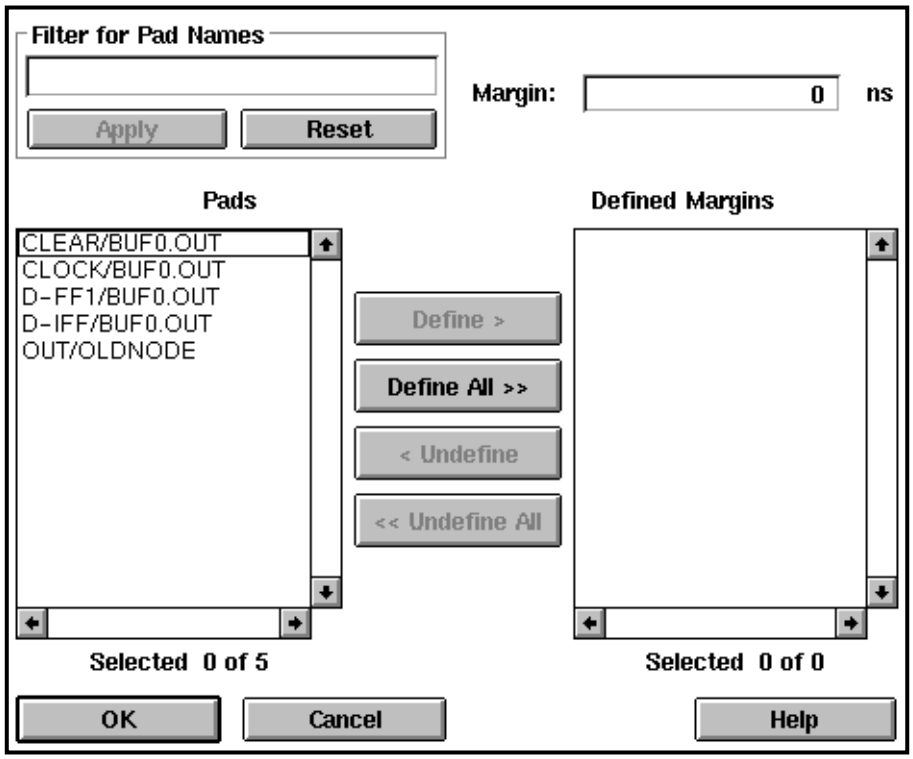


Figure 5-19 Set Delay Margins for I/O Window

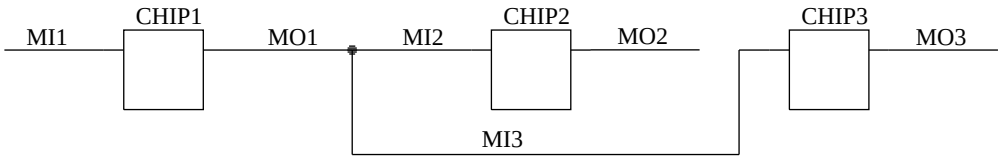
Follow these steps:

1. Type a name, partial name, or name with a wildcard in the Filter for Pad Names field to select a subset of the pads in the design. The ? is a single-character wildcard; the * is a multiple-character wildcard. Select the Apply button to apply the filter. To select all pads, leave this field blank or select the Reset button.
2. In the Margin field, type the number of nanoseconds additional delay you wish to add to the selected pads. If you enter an invalid value such as a negative number, an error message is displayed.
3. Select pads from the Pads list and transfer them to the Defined Margins list by selecting the Define > button. The delay you specified in step 2 applies to the pads in the Defined Margins list.

To remove a margin from a pad, select the pad in the Defined Margins list and then select the < Undefine button. The Define All >> and << Undefine All buttons transfer all pads in one list to the other list.

4. To apply a different delay to a different set of pads, repeat steps 1 through 3 with a different value in the Margin field.
5. Select OK when you have finished assigning delays to pads.

The following figure shows input, output, and interchip delays.



Interchip delays:

CHIP1 to CHIP2 = MO1 + MI2
CHIP1 to CHIP3 = MO1 + MI3

Figure 5-20 Margin Delays

Report Options

The Report Options command gives you additional filters for report information. When you select this command, the Report Options window appears, with the default values shown. Blank fields indicate that an infinite number are allowed. If you enter an invalid value such as a negative number, a warning is displayed.

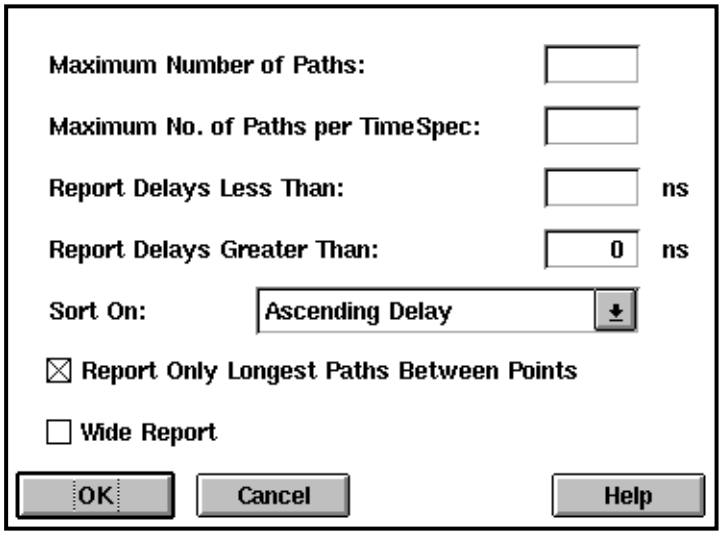


Figure 5-21 Report Options Window

The options are:

- *Maximum Number of Paths* — The maximum number of paths that will appear in the report.
- *Maximum No. of Paths per TimeSpec* — The maximum number of paths that will be reported for a specified T-Spec.
- *Report Delays Less Than* — Only those delays that are shorter than this specification are reported.
- *Report Delays Greater Than* — Only those delays that are longer than this specification are reported.
- *Sort On* — Determines how paths are listed in the report as follows:
  - Ascending Delay — Lists paths in order of their delay, with the shortest delay first and the longest last.
  - Descending Delay — Lists paths in order of their delay, with the longest delay first and the shortest last.

- Source Net — Lists paths alphabetically by the net at which they start.
- Destination Net — Lists paths alphabetically by the net at which they end.
- Source Clock Net — Lists paths alphabetically by the clock net at which they start.
- Destination Clock Net — Lists paths alphabetically by the clock net at which they end.

Index

Symbols

"*" used for multiplication, 4-14
"*" wildcard character, 4-12, 5-12
"/" used for division, 4-14
"?" wildcard character, 4-12, 5-12
.1 files, 1-9, 2-14
.cst files, 2-37
.gyd files, 2-15, 2-37, 3-5
.pld files, 1-2, 1-8, 2-14
.sch files, 2-14
.xff file, 1-10
.xff files, 1-3, 2-13
.xnf files, 1-3, 1-9, 2-7, 2-14

A

ABEL, Xilinx, 1-2

B

Break Logic Loops command, 5-21
Browse Revision command, 2-20

C

Cascade command, 5-9
Check for Asynchronous Logic command, 5-8
Close Project command, 2-11
combinational loops, 4-13
Command History command, 2-26
Configuration Data, 2-16, 2-17
Constraints file, 2-37
  conventions, 4-18
  creating, 4-17
  example, 4-21
  Syntax, 4-19
copy files, 2-21
Copy Revision command, 2-19

D

delete files, 2-22
Delete Project command, 2-11
Delete Revision command, 2-23
design
  control options table, 3-2
  export, 1-1
  flow, 1-1
  implementation, 1-1, 1-4, 1-12
  implementation overview, 3-1
  management, 2-3
  translation, 1-1, 1-3
Design Manager
  implementations, 2-2
  projects, 2-1
  revisions, 2-2
  single device selection, 3-4
  Tool Bar, 2-6
  tutorial, 1-6
  using, 2-5
  versions, 2-2
  window, 1-7, 1-11, 2-1, 2-5
Design Menu
  Browse Revision, 2-20
  Copy Revision, 2-19
  Delete Revision, 2-23
  Export, 2-17
  Implement, 1-4, 1-12, 2-14
  New Device, 2-18
  New Revision, 2-19
  Rename, 2-23
  Translate, 2-13

device selection
automatic selection criteria, 3-4
in Design Manager, 3-4
table, 3-3

E

Exclude Paths with Nets command, 5-18
Exit command, 2-12
Export command, 2-17
export, design, 1-1

F

Fast Output Enable optimization, 2-31
File Menu
Close Project, 2-11
Delete Project, 2-11
Exit, 2-12
File Name, 2-12
New Project, 1-8, 2-6
Open Project, 2-10
Save Project, 2-11
files
.1, 1-9, 2-14
.cst, 2-37
.gyd, 2-15, 2-37, 3-5
.pld, 1-2, 1-8, 2-14
.sch, 2-14
.xff, 1-3, 1-10, 2-13
.xnf, 1-3, 1-9, 2-7, 2-14
Constraints, 2-37, 4-17
copy, 2-21
delete, 2-22
editor, 2-21
guide, 2-15, 2-37
move, 2-22
filters, path, 5-6, 5-11
Flow command, 2-37
Flow Engine, 2-2
simplified, 2-16
using, 2-36
Flow Engine command, 2-24
Flow Engine Menu
Flow, 2-37
Help, 2-42
Setup, 2-38
Utilities, 2-42

G

Guide Files, 2-15, 2-37

H

Help command, 2-42
Help Menu
Contents, 2-34
Search, 2-35
Tutorial, 2-35

I

I/O pads, driving, 2-29
Ignore Timespecs command, 5-12
IGNORE, timing path, 4-13
Implement command, 2-14
implementation, design, 1-1, 1-4, 1-12, 2-15
Include Paths with Nets command, 5-18

L

Low Power Mode, 2-29

M

managing, designs, 2-3
move files, 2-22
Multi-Chip Designs, 2-8

N

New Device command, 2-18
New Project command, 2-6
New Revision command, 2-19

O

Open Project command, 2-10
optimization
Fast Output Enable, 2-31
timing driven, 2-31, 3-8
optimization control
Fast Clock, 3-9
Fast Output Enable, 3-8
in Design Manager, 3-6

Optimization Template, 2-30

P

Part Selector, 2-19
Partitioner, 2-2
path filters, 5-6
  applying, 5-11
Physical Design Data, 2-17
pin assignment, 2-29, 3-5
PLUSASM, 1-2, 1-8
power control, 2-29
power management
  in Design Manager, 3-9
predefined groups, T-Spec, 4-5
Program Option Templates, 2-15
project management, 2-2
Project Notes command, 2-27

R

Rename command, 2-23
Report Browser, 1-13
Report Browser command, 2-25
Report Options command, 5-26
Report Paths Failing Timespec command, 5-11
Report Paths with No Timespec command, 5-11
Reports, 1-4
  Detailed Path, 5-6
  Performance Summary, 5-4
  Performance to Timespecs, 5-3
Reset Path Filters command, 5-23
resource reservation
  in Design Manager, 3-12
Resources Template, 2-31

S

Save Project command, 2-11
Search command, 2-35
Select Destinations command, 5-13
Select Path Types command, 5-16
Select Sources command, 5-13
Set Delay Margins for I/O command, 5-24
Set Speed Grade command, 5-24
Setup command, 2-38
Show Clocks command, 5-8
Show Settings command, 5-8
Single-Chip designs, 2-8

T

Template Manager command, 2-27
Templates
  Fitting, 2-29, 3-7, 3-11, 3-13, 4-2
  Optimization, 2-30, 3-8
  Program Option, 2-15
  Resources, 2-31, 3-13
Tile command, 5-9
TIMEGRP
  attributes, table, 4-17
  primitive, 4-9
  symbols, 4-5
TIMEGRP attribute, 4-9
  combining multiple groups, 4-10
  grouping by exclusion, 4-11
  syntax, 4-9, 4-20
TIMESPEC attributes
  table, 4-17
TIMESPEC primitive, 4-3
  basic groups, 4-4
  FROM-TO statement, 4-4
  syntax, 4-4
Timing Analyzer, 1-5, 2-2
  icon, 5-2
  procedure, 5-1
  reports, 5-3
Timing Analyzer command, 2-24
Timing Analyzer tutorial, 1-14
timing control, 4-3
timing driven optimization, 2-31, 3-8
Timing Report, 2-15
Timing Simulation Data, 2-16, 2-17
TNM attribute, 4-5
  grouping flip–flops, 4-7
  incompatible symbols, 4-7
  on clock pins, 4-9

on macro symbols, 4-7
on primitive symbols, 4-6
on signal, 4-7
placement on schematic, 4-6
TNM attributes
table, 4-17
Tools Menu
Flow Engine, 2-24
Timing Analyzer, 1-14, 2-24
Translate command, 2-13
Translate Options Window, 1-9
translation
design, 1-1, 1-3
TS attribute, 4-3
delay, 4-13
length, 4-3
specifying, 4-13
time delay units, 4-15
T-Specs, 2-29, 2-37, 4-1, 5-1
tutorial, Design Manager, 1-6

U

Utilities command, 2-42
Utilities Menu
Command History, 2-26
Project Notes, 2-27
Report Browser, 1-13, 2-25
Template Manager, 2-27

V

ViewLogic, 1-9

X

XACT–Performance, 2-29, 4-1
combinational loops, 4-13
combining multiple groups, 4-10
creating new groups, 4-9
group by exclusion, 4-11
group by signal name, 4-11
ignore selected paths, 4-13
multiple specifications, 4-12
predefined groups, 4-5
sample schematic, 4-15
syntax, 4-16
TIMEGRP attribute, 4-9
TIMEGRP primitive, 4-10
TIMESPEC primitive, 4-3
TNMs, 4-5
TS attribute, 4-3
wildcards, 4-11
Xilinx ABEL, 1-2