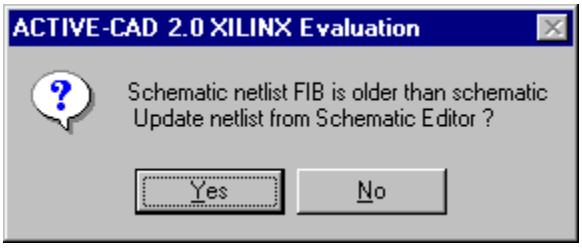
Timing Simulation Tutorial

The timing simulation is based on the FIB sample design provided with ACTIVE-CAD. The design generates the Fibonacci number sequence, where each new number is a sum of two previous numbers.

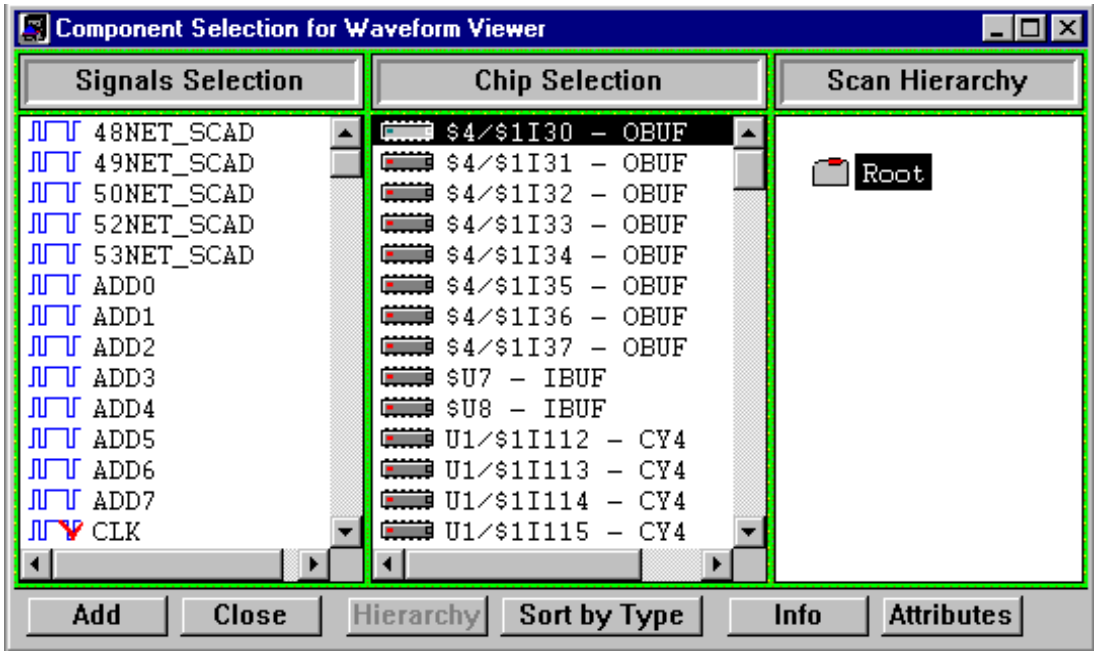
The design is implemented with Unified library macros. The routed files for timing simulation are provided in the sample design.

Starting Timing Simulation

1. Open FIB Project
2. Click on SIM Timing Button
3. At the Prompt for updating a netlist answer No.



4. The simulator window starts. (Ignore the message about Error reading formula file).
5. Select the Add Signals option from the Signal menu



Select the following signal names:

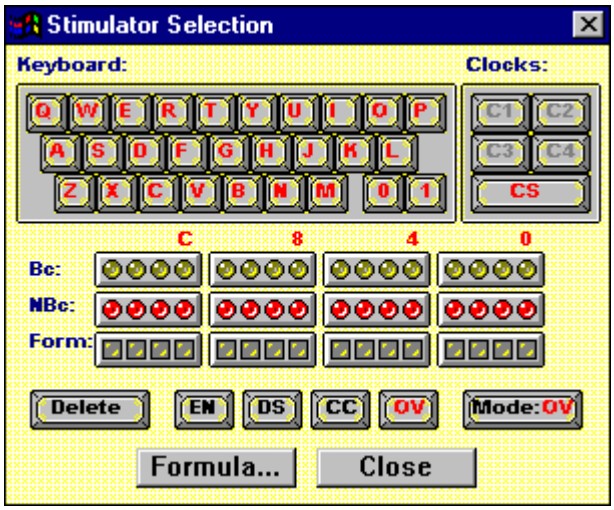
- CLK
- ENABLE
- FIBOUT0 - FIBOUT8

- RESET

The signals should be added to the Waveform Viewer window.

Defining Stimulators

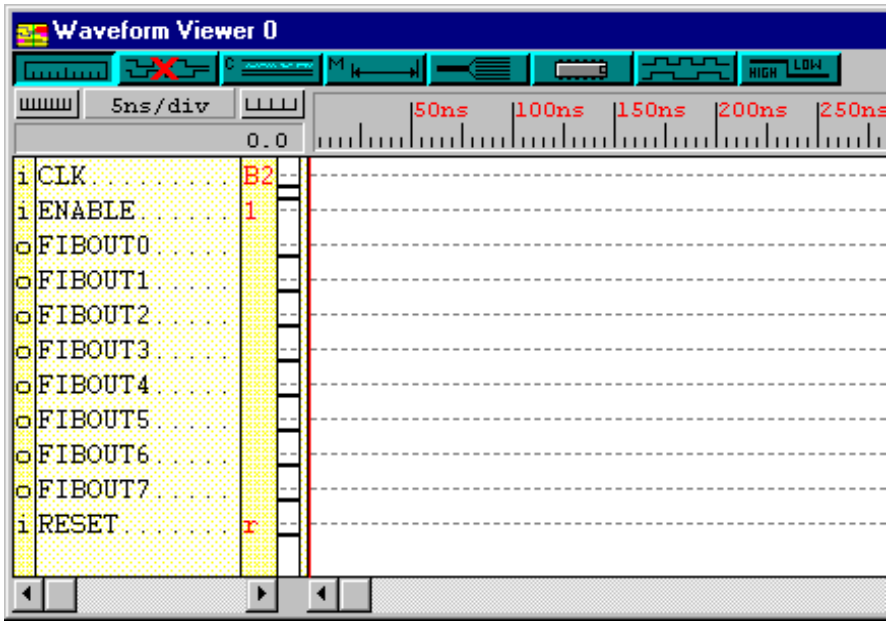
Select the Add Stimulators option from the Stimulator menu



Add these stimulators:

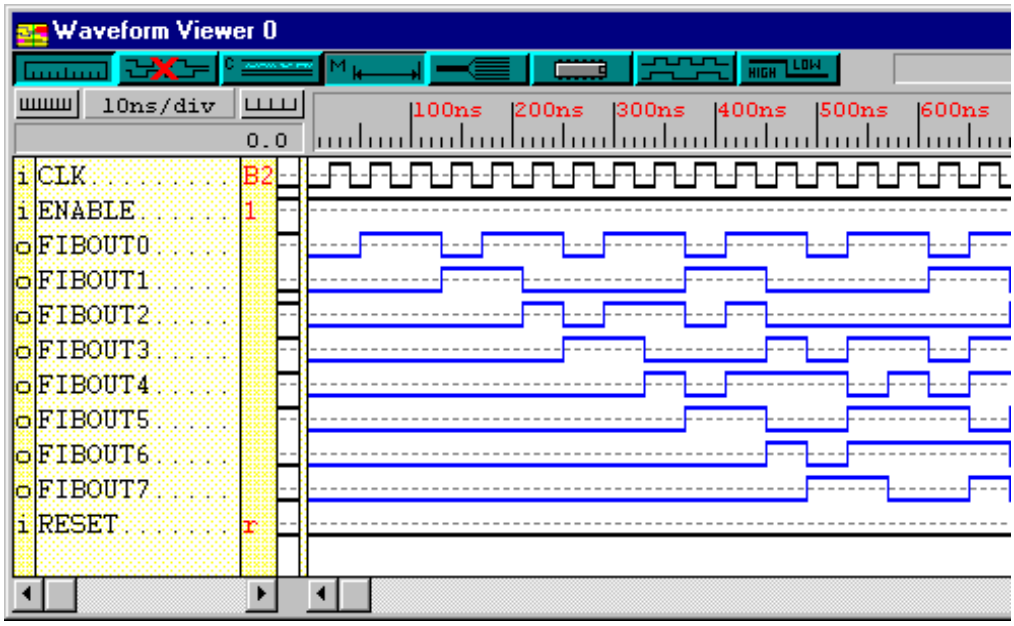
- **CLK = B2** (this will generate a clock with 40ns period)
- **ENABLE = 1**
- **RESET = r** (this keyboard key assignment will allow to toggle the signal with a keyboard key)

To add a stimulator, select the signal in thewaveform viewer and then click on the desired icon in the Stimulator Selection window.



Running Simulation

1. Close the Stimulator Selection window
2. Make sure that the Simulator toolbox shows Mode TM (Timing mode).
3. Toggle the R key to set RESET to Low state.
4. Press the Step button in the Simulator toolbox several times to generate the simulation data

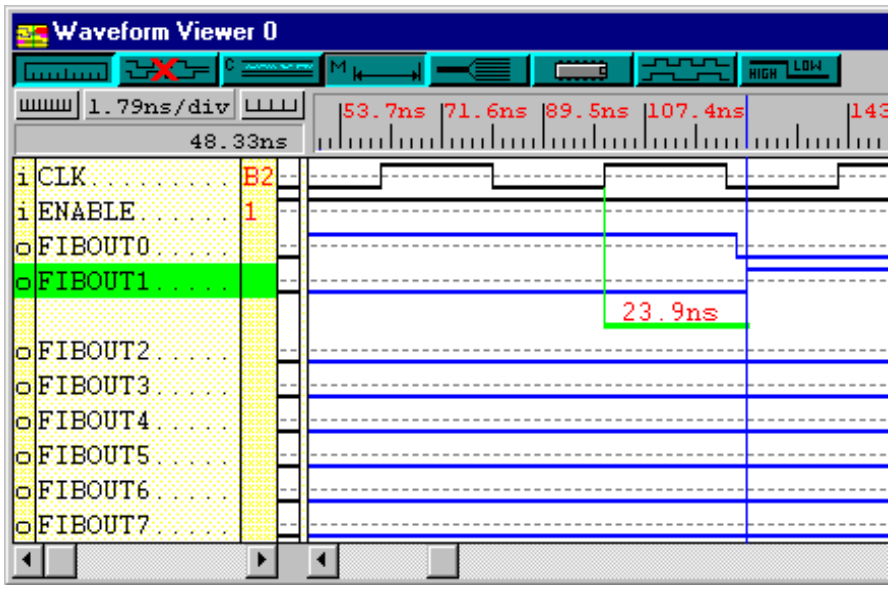


Note that you do not have to generate the high RESET signal, because the design is being reset automatically using the Global Reset in the simulator.

Measuring delays on the waveforms

This step will show you how to precisely measure the delays between transitions in the Waveform Viewer:

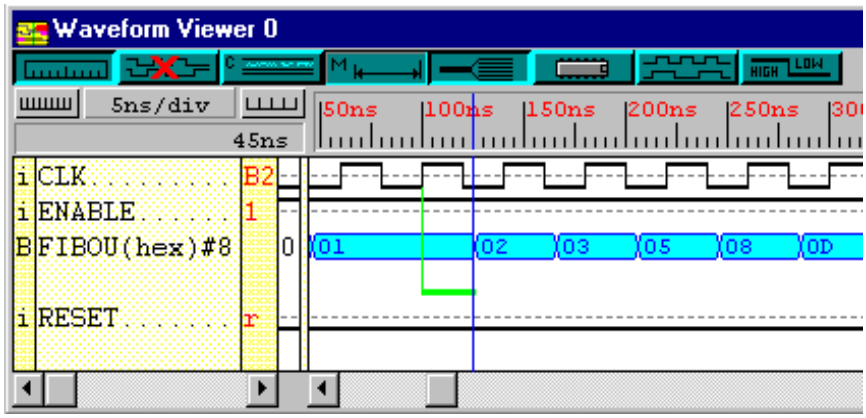
1. Zoom in the Waveform by dragging the line from 50 to 200ns on the Waveform ruler. As you drag the mouse, a blue line is being drawn to show the zoom area. Release the mouse button to expand the view.
2. Select the Measure On option from the Edit/Measurements menu
3. With the arrow in the cursor, click on the raising clock transition at 100ns
4. With the second arrow cursor click on the FIBOUT1 output transition at approximately 120ns
5. The Delay measurement will be displayed on the diagram. It should read 23.9ns.



Defining buses

To verify that the correctFibbonacci sequence is generated, the outputs will be displayed in numerical bus values, rather than separate waveforms.

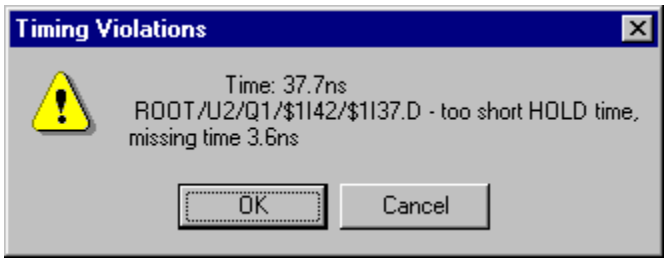
1. Select the signal FIBOUT0 and then with the Shift key depressed select the FIBOUT7 signal
2. The entire range of FIBOUT signals should be highlighted in blue
3. Select Create option from the Signal/Bus menu
4. Click on the Bus button in the Waveform Viewer toolbar to toggle the numerical display of the bus



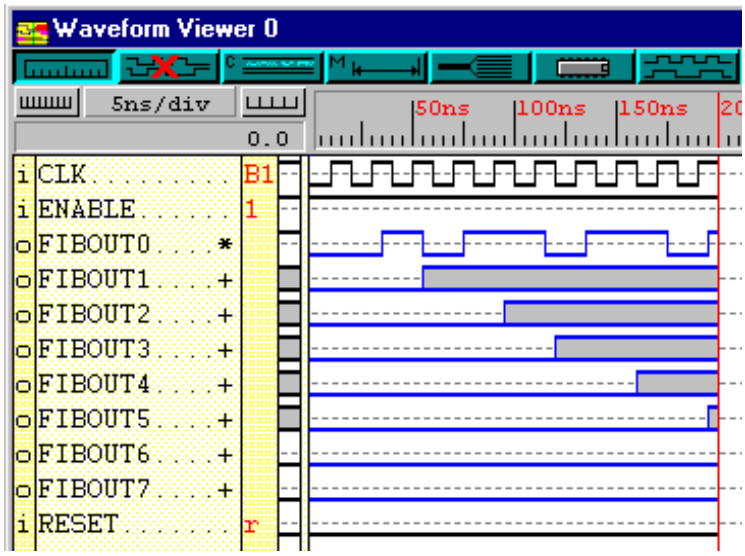
Delete Waveforms and define faster clock

To observe the timing violations, a faster clock signal will be defined

1. Using Stimulator Selection window select the B1 clock instead of B2
2. Press the Power On button in the Simulator toolbox
3. Select All Waveforms option from the Signal/Delete menu
4. Start the simulation again by pressing the Step button
5. The timing violation message is displayed on the screen



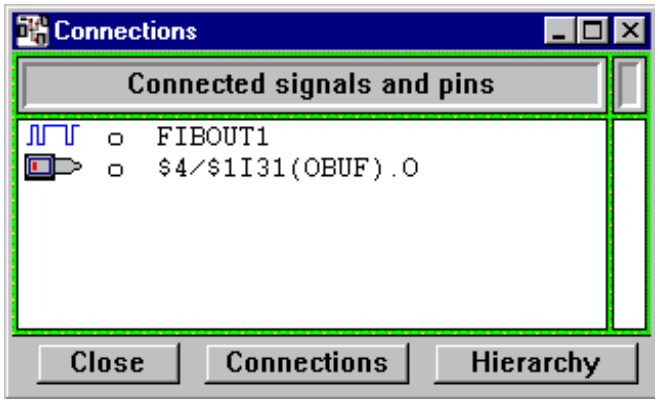
6. Select Cancel and simulate a few more steps
7. Notice that the FIBOUT outputs display the unknown states.



Trace Timing Violations

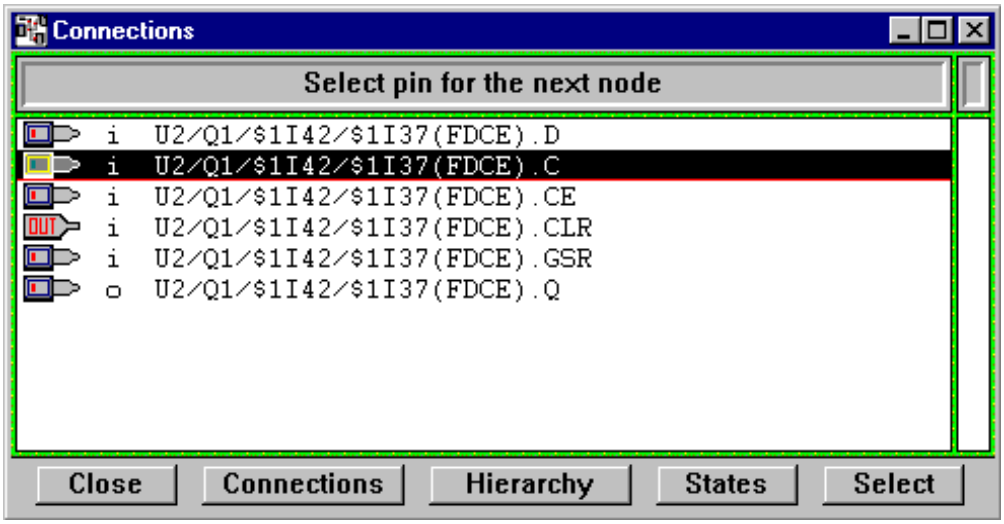
To trace the source of the timing violation, a Connection window will be used. It allows to trace the netlist connections without having to view the schematic. It is especially useful when timing problems are reported in synthesized modules that were created from VHDL or ABEL.

1. Select the FIBOUT1 signal in the Waveform Viewer
2. Select the Connections option
3. The window lists the OBUF output pin connected to the FIBOUT1 signal

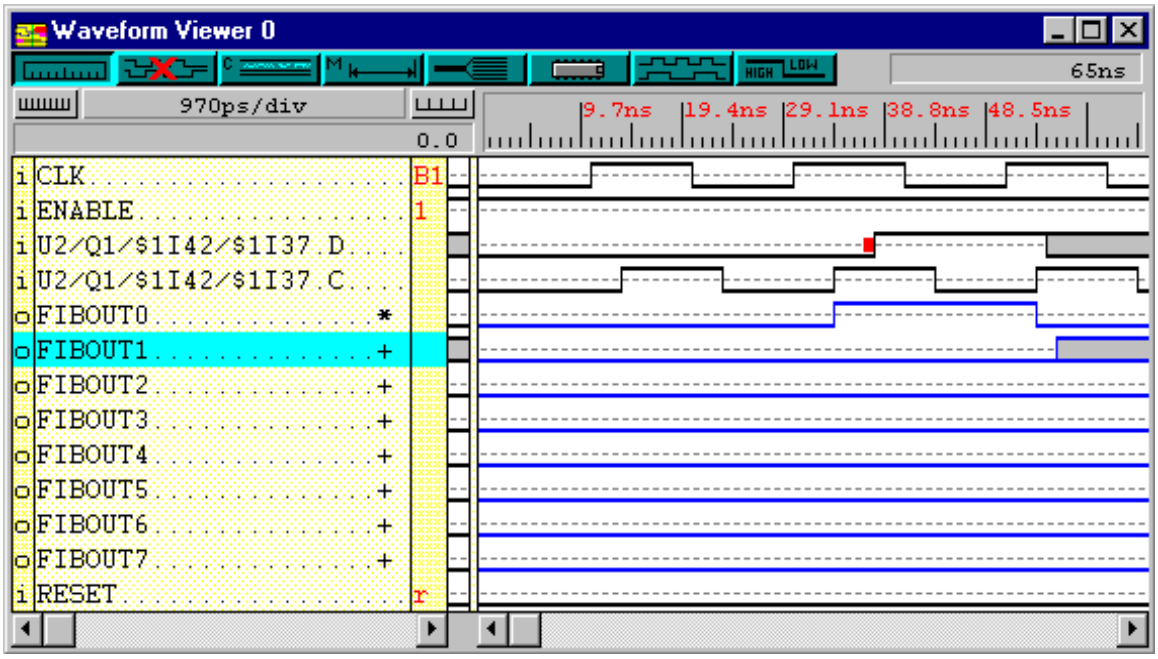


4. Double click on the O pin. This displays all pins of the OBUF.

5. Double click on the I pin to trace the connection to the input of the OBUF
6. This displays several input pins and one output pins. The source of errors is always generated by output pins
7. Double click on the Q output pin of the FDCE flip-flop



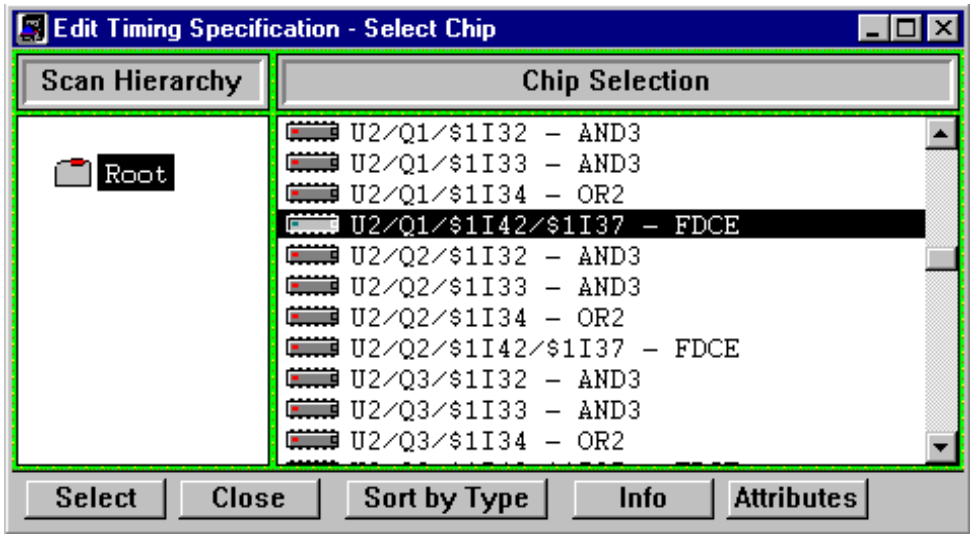
8. To trace the input signals of the suspected flip-flop, highlight the C clock input and press the Select button to add the signal into the Waveform Viewer
9. Then, highlight the D input and press the Select button again.
10. Press the Power On button in the Simulator toolbox and resimulate the design until the timing violation is reported.
11. Notice that the red error marker is displayed on the D input of the flip-flop



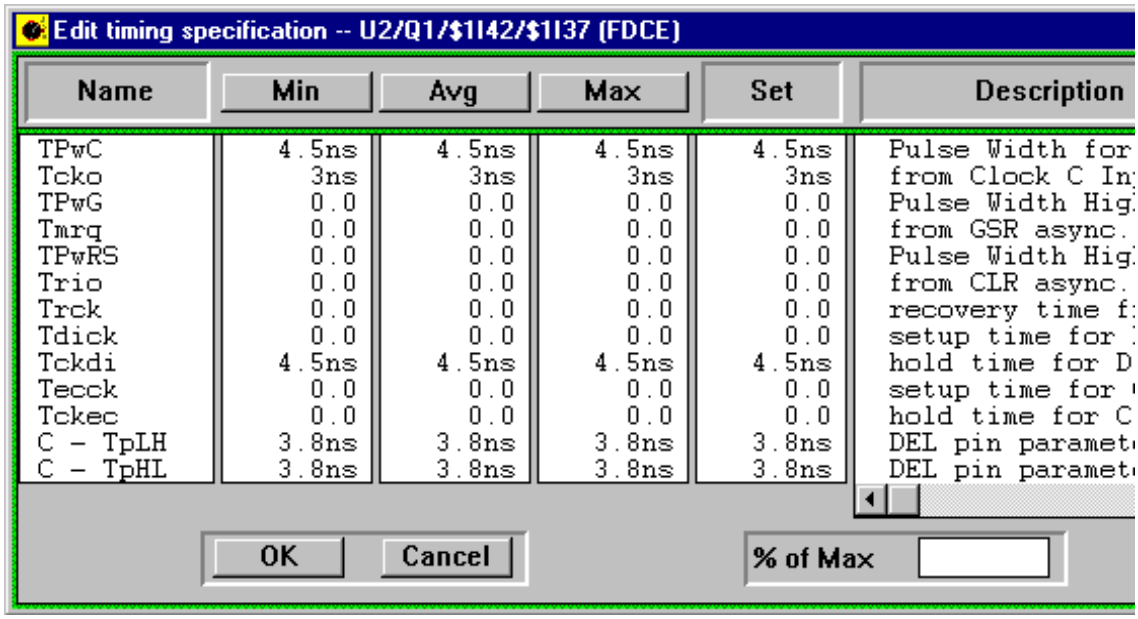
Review Timing Delays table

1. To review the timing data for the flip-flop that caused timing violation select the Edit Timing Specification option in the Patching menu

2. In the Chip selection list, double-click on the U2/Q1/$1I42/$1I37 - FDCE flip-flop entry



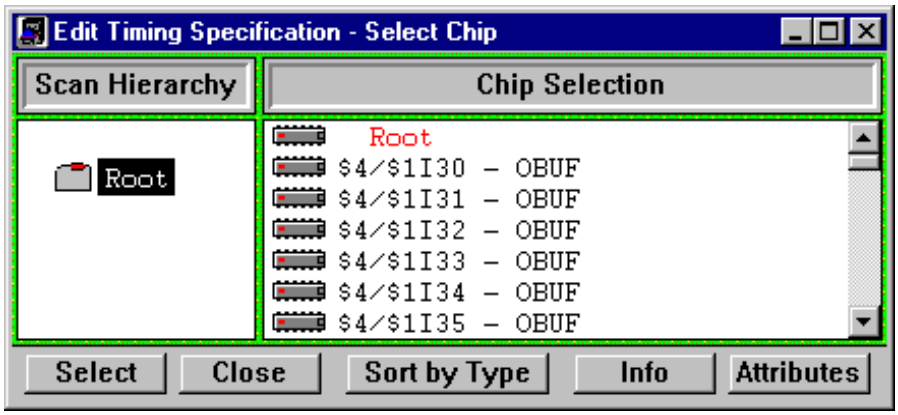
3. In the Edit Timing Specification window notice that there is a 4.5ns Hold time requirement for the D input.



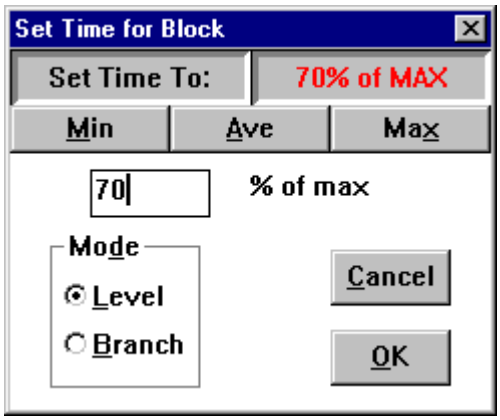
Scale device timing

To find out if a faster device selection would help with the timing problem, the simulator provides the delay scaling capabilities. If a faster device has delays of 70% of the current device, you can scale the entire FPGA timing by 70% and resimulate the design to see if the timing violations will go away.

1. Select the Edit Timing Specification option in the Patching menu
2. Double click on the first entry - **Root**



3. In the Set Time for Block window enter 70% of Max and press OK
4. This will recalculate the entire timing data of the design



5. Resimulate the design once more and notice that the timing violations are no longer reported.

End