Timing Simulation Tutorial

The timing simulation is based on the FIB sample design provided with ACTIVE-CAD. The design generates the Fibonacci number sequence, where each new number is a sum of two previous numbers.

The design is implemented with Unified library macros. The routed files for timing simulation are provided in the sample design.

Starting Timing Simulation

- 1. Open FIB Project
- 2. Click on SIM Timing Button
- 3. At the Prompt for updating a netlist answer No.



- 4. The simulator window starts. (Ignore the message about Error reading formula file).
- 5. Select the Add Signals option from the Signal menu

Component Selection for Waveform Viewer				
Signals Selection	Chip Selection	Scan Hierarchy		
N ✓ 48NET_SCAD ▲ N ✓ 49NET_SCAD ■ N ✓ 50NET_SCAD ■ N ✓ 52NET_SCAD ■ N ✓ S3NET_SCAD ■ N ✓ ADD0 ■ ■ N ✓ ADD1 ■ ■ N ✓ ADD2 ■ ■ ■ N ✓ ADD3 ■ ■ ■ ■ N ✓ ADD5 ■ ■ ■ ■ N ✓ ADD7 ■ ■ ■ ■	<pre>\$4/\$1130 - OBUF \$4/\$1131 - OBUF \$4/\$1132 - OBUF \$4/\$1133 - OBUF \$4/\$1134 - OBUF \$4/\$1135 - OBUF \$4/\$1136 - OBUF \$4/\$1137 - OBUF \$4/\$1137 - OBUF \$1/\$1137 - OBUF \$1/\$11112 - CY4 U1/\$11112 - CY4 U1/\$11113 - CY4 U1/\$11115 - CY4</pre>	n Root		
Add Close	lierarchy Sort by Type	Info Attributes		

Select the following signal names:

- CLK
- ENABLE
- FIBOUT0 FIBOUT8

• RESET

The signals should be added to the Waveform Viewer window.

Defining Stimulators

Select the Add Stimulators option from the Stimulator menu

🙀 Stimulator Selection 🛛 🗙
Keyboard: Clocks:
QWERTYUIOP CIC2
ASDFGHJKL C3 C4
C 8 4 0
Bc: 0000 0000 0000 0000
NBc: ଡଡଡଡ ଡଡଡଡ ଡଡଡଡ
Form: [0000] [0000] [0000]
Delete EN DS CC OV Mode:OV
Formula Close

Add these stimulators:

- **CLK = B2** (this will generate a clock with 40ns period)
- **ENABLE** = 1
- **RESET** = \mathbf{r} (this keyboard key assignment will allow to toggle the signal with a keyboard key)

To add a stimulator, select the signal in thewaveform viewer and then click on the desired icon in the Stimulator Selection window.

🚾 Waveform View	er O						
		≝ ^M ₩			170		.014
uuuu 5ns/div		· .	50ns	100ns	150ns	200ns	250ns
	0.0	huntu	uluulu	nluuluu	duului	<u>iliiiiliii</u>	duuli
i CLK	B2						
i ENABLE	1						
oFIBOUTO	<u></u>						
oFIBOUT1							
oFIBOUT2							
oFIBOUT3							
oFIBOUT4							
oFIBOUT5							
oFIBOUT6							
oFIBOUT7							
i RESET	r						
•	►	•					

Running Simulation

- 1. Close the Stimulator Selection window
- 2. Make sure that the Simulator toolbox shows Mode TM (Timing mode).
- 3. Toggle the R key to set RESET to Low state.
- 4. Press the Step button in the Simulator toolbox several times to generate the simulation data

🚾 Waveform Viewer O	
<u>مسسمار</u> ک کر ا	
10ns/div 1111	100ns 200ns 300ns 400ns 500ns 600ns
0.0	յուվուսիստիոսիստիոսիստիոսիստիոսիստիոսի
i CLK B2	<u>╶</u> ┎न _╋
i ENABLE 1	
oFIBOUTO	<u></u>
oFIBOUT1	
oFIBOUT2	
oFIBOUT3	<u></u> <mark></mark>
oFIBOUT4	
oFIBOUT5	
oFIBOUT6	
oFIBOUT7	
i RESET r	

Note that you do not have to generate the high RESET signal, because the design is being reset automatically using the Global Reset in the simulator.

Measuring delays on the waveforms

This step will show you how to precisely measure the delays between transitions in the Waveform Viewer:

- 1. Zoom in the Waveform by dragging the line from 50 to 200ns on the Waveform ruler. As you drag the mouse, a blue line is being drawn to show the zoom area. Release the mouse button to expand the view.
- 2. Select the Measure On option from the Edit/Measurements menu
- 3. With the arrow in the cursor, click on the raising clock transition at 100ns
- 4. With the second arrow cursor click on the FIBOUT1 output transition at approximately 120ns
- 5. The Delay measurement will be displayed on the diagram. It should read 23.9ns.

🎫 Waveform Viewer 0	
^و	
للللا 1.79ns/div	53.7ns 71.6ns 89.5ns 107.4ns 143
48.33ns	<u>իսիստիստիստիստիստիստիստիստիստիստիստիս</u>
iCLKB2	<u></u>
i ENABLE 1	
oFIBOUT0	
oFIBOUT1	
	23.9ns
oFIBOUT2	
oFIBOUT3	
oFIBOUT4	
oFIBOUTS	
oFIBOUT6	
oFIBOUT7	

Defining buses

To verify that the correctFibbonacci sequence is generated, the outputs will be displayed in numerical bus values, rather than separate waveforms.

- 1. Select the signal FIBOUT0 and then with the Shift key depressed select the FIBOUT7 signal
- 2. The entire range of FIBOUT signals should be highlighted in blue
- 3. Select Create option from the Signal/Bus menu
- 4. Click on the Bus button in the Waveform Viewer toolbar to toggle the numerical display of the bus

🎫 Waveform View	er O						
		≖ ^M k —	→ — (=		_ ~~		LOW
uuuu 5ns/div	ш	50ns	100ns	150ns	200ns	250n	.s 30
	45ns	յիստիս	որութող	luului	duulu	uluul	mulu
i CLK	B2_	<u> </u>					
i ENABLE	1	-					
BFIBOU(hex)#8	0	01	02	(03	(05	(08	(OD
i RESET	r -						
		-					
•		•					

Delete Waveforms and define faster clock

To observe the timing violations, a faster clock signal will be defined

- 1. Using Stimulator Selection window select the B1 clock instead of B2
- 2. Press the Power On button in the Simulator toolbox
- 3. Select All Waveforms option from the Signal/Delete menu
- 4. Start the simulation again by pressing the Step button
- 5. The timing violation message is displayed on the screen

Timing Violations			
	Time: 37.7ns ROOT/U2/Q1/\$1142/\$1137.D - too short HOLD time, missing time 3.6ns		
	Cancel		

- 6. Select Cancel and simulate a few more steps
- 7. Notice that the FIBOUT outputs display the unknown states.

🚾 Waveform Viewer O	
<u>ا سسما</u> ک ک ر	
لللل 5ns/div	50ns 100ns 150ns 20
0.0	
i CLK B1	╞╌┲╼╄╼┲╼╄╼┲╼╊╼┲╼┲╼┲╼┲╼┲╼┲╼┲╼┲
iENABLE 1	
oFIBOUTO*	<mark></mark>
oFIBOUT1+	
oFIBOUT2+	
oFIBOUT3+	
oFIBOUT4+	
oFIBOUT5+	-
oFIBOUT6+	
oFIBOUT7 +	
i RESET r	

Trace Timing Violations

To trace the source of the timing violation, a Connection window will be used. It allows to trace the netlist connections without having to view the schematic. It is especially useful when timing problems are reported in synthesized modules that were created from VHDL or ABEL.

- 1. Select the FIBOUT1 signal in the Waveform Viewer
- 2. Select the Connections option
- 3. The window lists the OBUF output pin connected to the FIBOUT1 signal

👪 Cor	nnectio	ns	_ 🗆 ×
	Co	nnected signals and	pins 🛛
	0 H 0 \$	TIBOUT1 94∕\$1I31(OBUF).0	
C	lose	Connections	Hierarchy

4. Double click on the O pin. This displays all pins of the OBUF.

- 5. Double click on the I pin to trace the connection to the input of the OBUF
- 6. This displays several input pins and one output pins. The source of errors is always generated by output pins
- 7. Double click on the Q output pin of the FDCE flip-flop

🌃 Conne	ctions	×
	Select pin for the next node	$\left[\right]$
	U2/Q1/\$1I42/\$1I37(FDCE).D U2/Q1/\$1I42/\$1I37(FDCE).C U2/Q1/\$1I42/\$1I37(FDCE).CE U2/Q1/\$1I42/\$1I37(FDCE).CLR U2/Q1/\$1I42/\$1I37(FDCE).GSR U2/Q1/\$1I42/\$1I37(FDCE).Q	
Clos	e Connections Hierarchy States Select	

- 8. To trace the input signals of the suspected flip-flop, highlight the C clock input and press the Select button to add the signal into the Waveform Viewer
- 9. Then, highlight the D input and press the Select button again.
- 10. Press the Power On button in the Simulator toolbox and esimulate the design until the timing violation is reported.
- 11. Notice that the red error marker is displayed on the D input of the flip-flop

💒 Waveform Viewer 0		
<u>□□□□□□</u> <u><u>-</u><u>-</u><u>-</u><u>-</u><u>-</u><u>-</u><u>-</u><u>-</u><u>-</u><u>-</u><u>-</u><u>-</u><u>-</u></u>		HIGH LOW 65ns
970ps/div	9.7ns 19.4n 0.0	ns 29.1ns 38.8ns 48.5ns
i CLK i ENABLE 1 U2/Q1/\$1I42/\$1I37.D i U2/Q1/\$1I42/\$1I37.C. o FIBOUT0 o FIBOUT1 o FIBOUT2 o FIBOUT3 o FIBOUT4 o FIBOUT5 o FIBOUT6 o FIBOUT7 i RESET ◀	B1	

Review Timing Delays table

1. To review the timing data for the flip-flop that caused timing violation select the Edit Timing Specification option in the Patching menu

2. In the Chip selection list, double-click on the U2/Q1/\$1I42/\$1I37 - FDCE flip-flop entry

📕 Edit Timing Specification - Select Chip 📃 💶 🗙				
Scan Hierarchy	Chip Selection			
noot	<pre> U2/Q1/\$1I32 - AND3 U2/Q1/\$1I33 - AND3 U2/Q1/\$1I34 - OR2 U2/Q1/\$1I34 - OR2 U2/Q2/\$1I32 - AND3 U2/Q2/\$1I33 - AND3 U2/Q2/\$1I34 - OR2 U2/Q2/\$1I42/\$1I37 - FDCE U2/Q2/\$1I42/\$1I37 - FDCE U2/Q3/\$1I32 - AND3 U2/Q3/\$1I32 - AND3 U2/Q3/\$1I33 - AND3 U2/Q3/\$1I33 - AND3 U2/Q3/\$1I33 - AND3 </pre>			
Select Clos	e Sort by Type Info Attributes			

3. In the Edit Timing Specification window notice that there is a 4.5ns Hold time requirement for the D input.

Edit timing specification U2/Q1/\$1142/\$1137 (FDCE)									
Name	Min	A∨g	Max	Set	Description				
TPwC Tcko TPwG Tmrq TPwRS Trio Trck Tdick Tckdi Tckdi Tcckdi C - TpLH C - TpHL	4.5ns 3ns 0.0 0.0 0.0 0.0 0.0 4.5ns 0.0 0.0 3.8ns 3.8ns 3.8ns	4.5ns 3ns 0.0 0.0 0.0 0.0 0.0 4.5ns 0.0 0.0 3.8ns 3.8ns 3.8ns	4.5ns 3ns 0.0 0.0 0.0 0.0 0.0 4.5ns 0.0 0.0 3.8ns 3.8ns	4.5ns 3ns 0.0 0.0 0.0 0.0 0.0 4.5ns 0.0 0.0 3.8ns 3.8ns 3.8ns	Pulse Width for from Clock C In Pulse Width Hig from GSR async. Pulse Width Hig from CLR async. recovery time for setup time for D setup time for D hold time for C DEL pin parameto DEL pin parameto				

Scale device timing

To find out if a faster device selection would help with the timing problem, the simulator provides the delay scaling capabilities. If a faster device has delays of 70% of the current device, you can scale there FPGA timing by 70% and resimulate the design to see if the timing violations will go away.

- 1. Select the Edit Timing Specification option in the Patching menu
- 2. Double click on the first entry **-Root**

📕 Edit Timing Specification - Select Chip					
Scan Hierarchy	Chip Selection				
noot	Root \$4/\$1I30 - OBUF \$4/\$1I31 - OBUF \$4/\$1I32 - OBUF \$4/\$1I33 - OBUF \$4/\$1I33 - OBUF \$4/\$1I34 - OBUF \$4/\$1I35 - OBUF	•			
Select Clo	se Sort by Type Info	Attributes			

- In the Set Time for Block window enter 70% oMax and press OK
 This will recalculate the entire timing data of the design

Set Time for Block						
Set Time	70% of MAX					
<u>M</u> in	<u>A</u> v	/e	Ma <u>×</u>			
70		% of max				
-Mo <u>d</u> e			<u>C</u> ancel			
C <u>B</u> ranc	h	<u>0</u> K				

5. Resimulate the design once more and notice that the timing violations are no longer reported.

End