XILINX®

ONLINE

DESIGN MANAGER FLOW ENGINE

REFERENCE/USER GUIDE

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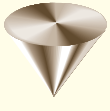

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Chapter 1

Introduction

This chapter briefly describes the Design Manager and Flow Engine. It describes their function, place in the design flow, major features, inputs and outputs, and the architectures with which they work. It also outlines the basic procedure for using these tools. Since the Design Manager and Flow Engine are very closely integrated, this manual covers the Design Manager and Flow Engine as a single software application. This chapter describes the following topics:

- Overview
- Design Flow
- Inputs and Outputs
- Architectures
- Design Manager Fundamentals
- Flow Engine Fundamentals
- Tutorial
- Online Help

Overview

The Design Manager is the top level software module in the Xilinx Development System which is a tool suite for implementing a design into a Xilinx XC2000, XC3000, XC3000A, XC4000, XC5200, or XC7000 device. The Design Manager provides access to all the tools you need to read and translate a design file from a design entry tool and implement it in a Xilinx device.

The Design Manager does the following:

- Reads and automatically translates xnf, .1 (Viewlogic), .sch (OrCAD), and .pld design files.
- Implements your design into a Xilinx device(s).
- Exports timing data to simulation tools
- Generates analysis reports
- Programs the FPGA or ELPD

The Design Manager manages your Xilinx designs. The Flow Engine implements your designs. It is tightly coupled with the Design Manager, sharing many of the same menus and dialog boxes.

Design Flow

You can use a variety of schematic, behavioral, and VHDL tools for design entry. The supported schematic entry tools are Viewlogic and OrCAD. The supported behavioral entry tools are Xilinx ABEL and PLUSASM. The supported VHDL entry tools is Viewlogic Synthesis.

After design entry, the Design Manager processes your design in the following basic steps:

1. *Translation* of your design file into Xilinx's internal XFF file format.
2. *Implementation* of your design for a specific target device.
3. *Export* of your design for timing simulation and programming.
4. *Report Generation* showing the status of your design.
5. *Timing Analysis* for design verification.

Figure 1-1 illustrates the processing steps and the flow of files in and out of the Design Manager.

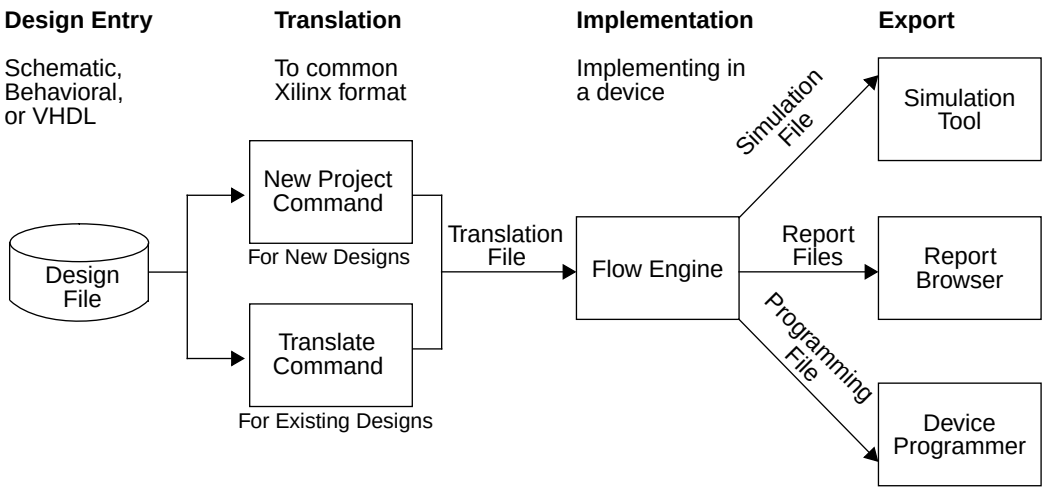


Figure 1-1 Design Manager Design Flow

Inputs and Outputs

The Design Manager accepts the following file types as inputs:

.1	Viewlogic schematic and wir
.sch	OrCAD schematic
.xnf	Xilinx hierarchical netlist
.pld	Xilinx (XC7000 only)

The Design Manager/Flow Engine outputs report, simulation, and programming files.

Architectures

You can use the Design Manager with Xilinx XC2000, XC3000/A, XC3100/A, XC4000/A/H/E, XC5200, and XC7000 devices.

Design Manager Fundamentals

The Design Manager window is shown in Figure 1-2.

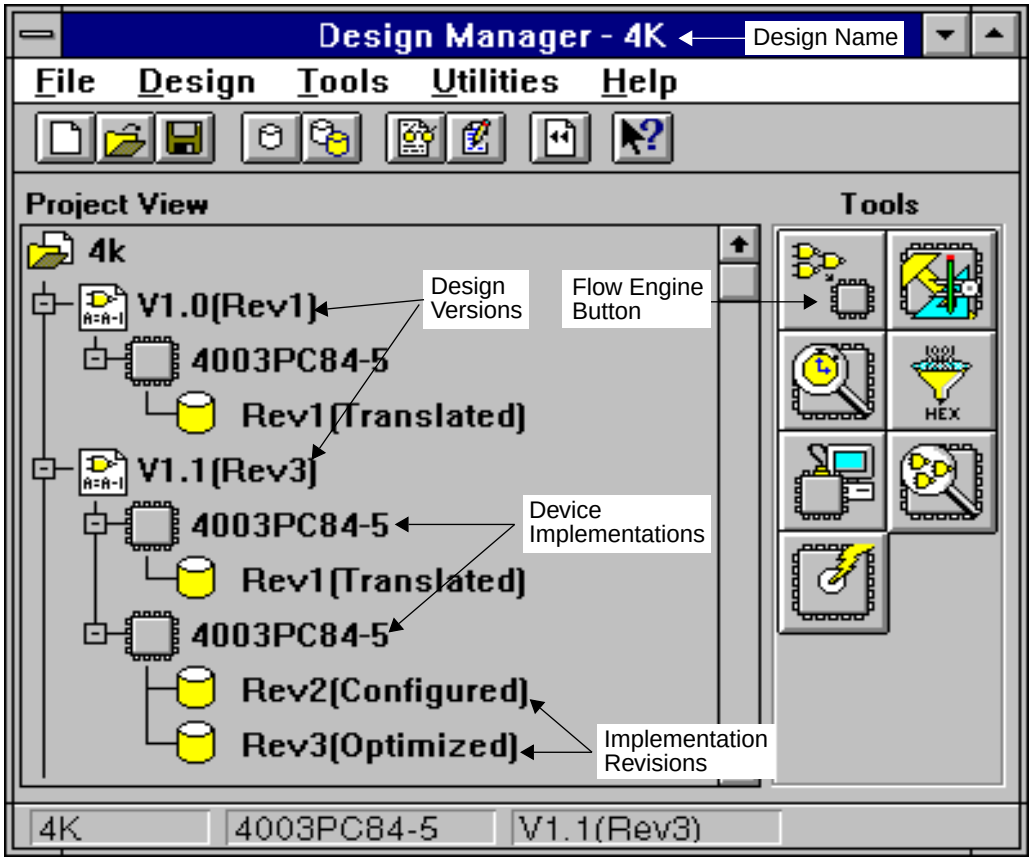


Figure 1-2 Design Manager Main Window

Design Manager Capabilities

You can use the Design Manager to perform the following functions:

- Read-in and automatically translate a design
- Organize and manage your design data
- Select a target device
- Manage data for and access to the following tools in the Xilinx Design Manager system. The tools differ for FPGA and EPLD.
  - FPGA (XC2000, XC3000, XC4000, XC5200)

    Flow Engine

    Timing Analyzer

    Floorplanner (XC3000A, XC4000, and XC5200 only)

    Hardware Debugger

    PROM File Formatter

    PROM Programmer

    Design Editor

    Report Browser
  - EPLD (XC7000)

    Flow Engine

    Timing Analyzer

    Partitioner

    Report Browser
- Implement the design
- Analyze the design
- Generate timing simulation data for external simulation tools
- Program a device

Design Management Functions

The Design Manager address the following design management functions.

Managing Projects

The Design Manager window displays all Xilinx data related to a single project. You can work with multiple projects (designs) but only one is displayed at a time. The hierarchical structure shows you the relationships of the data elements to each other. A project includes all design versions, device implementations, and implementation revisions that are created as you develop your design.

Managing Design Versions

You create your design using third party front-end tools such as schematic editors, behavioral equation editors, and VHDL. The design files are translated into the Design Manager and a version is created for the Design Manager project. Each time you change the logic of your design, you must translate it again and the Design Manager creates a new design version in the Project View. This allows you to try modified versions of your design and easily keep track of them. Each new file you translate becomes a new design version and is assigned a version number by the Design Manager. You can choose any one of the available versions for processing and for each version you may choose multiple target device implementations and different processing strategies. Old design versions can be deleted as desired.

Managing Device Implementations

You can target your design into any number of different devices within the same device family. This allows you to try your design in different devices in order to determine the most suitable fit. For example, if the results for a particular device prove to be too large or too slow for your needs, you can select a new target device in the same device family which is smaller or faster. You can delete old target device attempts which are no longer useful. You can implement your design into any number of different target devices; each is called an implementation.

Managing Implementation Revisions

After you create a design version by inputting a design file, and you choose a target device, you can try different implementation strategies on that design. This allows you to vary how your design is implemented in order to achieve your design objectives. For example, you can maximize speed and density in your design by controlling the implementation process. The data associated with each of these implementation strategies is called an implementation revision. Each implementation revision contains the output files and reports that are created based on a specific set of implementation strategies. You can delete implementation revisions that are no longer useful.

Design Management Basic Procedure

The typical procedure for managing a design is as follows:

1. Create your design using a third-party front-end tool such as those available from Viewlogic and OrCAD.
2. Output your design as a .1, .sch, or .xnf file.

   The Design Manager can read Viewlogic (.1) and OrCad (.sch) files directly. When you use other third-party tools, you need to write out hierarchical .xnf files for the Design Manager to read.
3. Open an existing project file; or create a new project file in which to import your logic design.
4. Translate your logic design. Your design file is converted into the Xilinx internal data base format (.xff).
5. If you desire, choose a different target device (or devices) in which to implement your design. The initial target device is specified in the input design or when you create a new project.
6. Select an option template to control your design process flow. You can use the default template, an existing template, or you can define a new template.
7. Process your design and:
   - Create timing simulation files (optional).
   - Create a device programming file (optional)

8. Review your design reports to verify that your design fits within the target device and that your timing requirements are met.
9. If your design requirements are not met you can do the following and process your design again:
   - Change your logic design.
   - Choose a different target device, package, or speed grade.
   - Define a different set of implementation options (option templates).

Flow Engine Fundamentals

The Flow Engine window is shown in Figure 1-3.

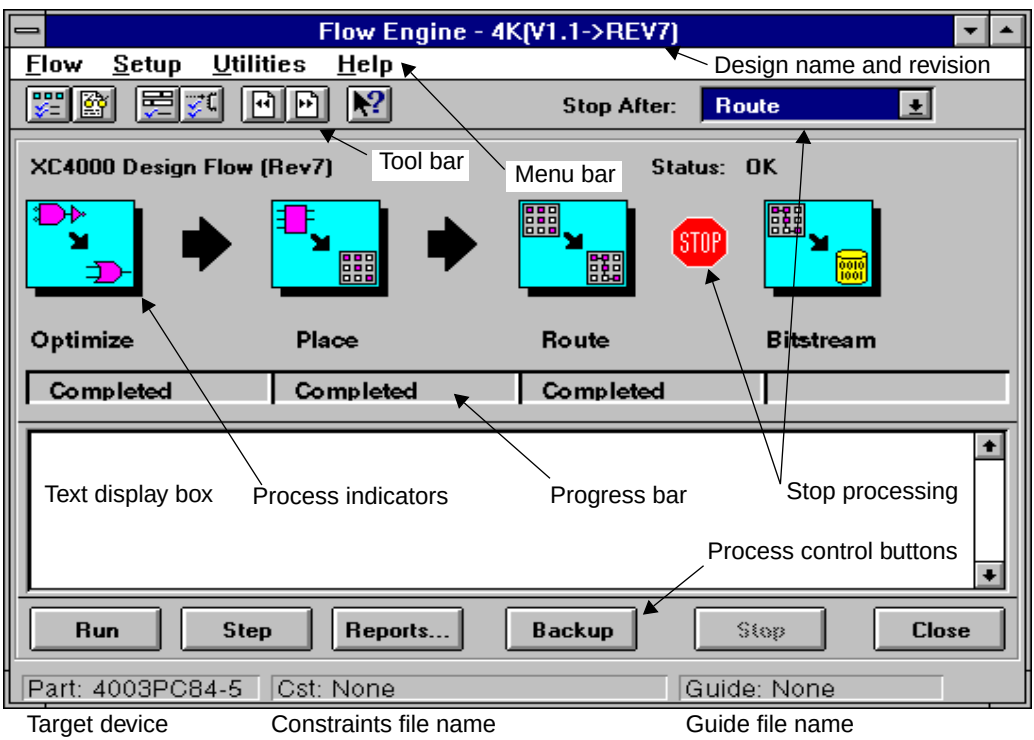


Figure 1-3 Flow Engine Window

Function

The Flow Engine allows you to easily manage the process flow of your design. You start the Flow Engine by selecting Flow Engine from the Design Manager Tools menu or by clicking the Flow Engine button (see Figure 1-4) in the Design Manager's toolbox.

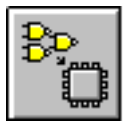


Figure 1-4 Flow Engine button

The Process Indicators (see Figure 1-3) show you the various software functions that are available for processing your design. You control how far to process your design by using the Stop After pull down dialog box. For example if you want to optimize, place, and route your design, but not create a timing simulation file or device programming file, select Stop After Place and Route. You will see a stop sign indicator verifying where the process will stop.

The Progress Bar shows you the status of each processing step and the arrows between each step turn black after the previous step is completed.

Controlling The Process Flow

The Flow Engine allows you to interact with the process flow in several ways. For example if you are new to Xilinx software or just want to run a quick "sanity check" on your design, you can simply click Run and the Flow Engine processes your design. However, if you are an experienced user and want to fine tune your design to get the best possible speed or density, you can control each function in the process. These controls are located under the Setup menu.

Using a Constraints File

You can create timing specifications which control the implementation of your design. These Timespecs may be described in a constraints file (*design_name*.cst) or in the design source such as the schematic. Additionally, if using an FPGA, you can include placement constraints in your constraints file. If you want to use a

constraints file to control the implementation of your design you can specify this file in the Flow Engine. The implementation software then tries to implement your design to meet the specified requirements.

Using a Guide File

Guide File usage differs for FPGA and EPLD devices.

FPGA — A guide file allows you to specify a previous revision of the design which has been implemented. The software attempts to use the implemented revision as a guide on how to place logic and route signals for the current revision of the design.

EPLD — Each time you implement your design, a guide file is created (*design_name*.gyd) which contains your pinout information. If you want to keep the same pinouts, you can re-use this file in subsequent iterations of your design. If you specify a valid guide file name in the Flow Engine window, the pinouts from that file will be used when the design is processed.

Tutorial

Online tutorials demonstrating the Design Manager's and Flow Engine's major functions are also available. To invoke the tutorial, select Tutorial from the Design Manager's or Flow Engine's Help menu.

Online Help

The Design Manager and Flow Engine have both context-sensitive help and a Help menu. See "Obtaining Online Help" on page 2-3 for information on accessing online help.

Getting Started

This chapter leads you through the basic operation of the Design Manager and Flow Engine. It covers the following topics:

- Preparing the Input Design File
- Starting the Design Manager
- Obtaining Online Help
- Creating a New Project
- Implementing the Design
- Viewing Reports

Preparing the Input Design File

Create the input design in your design entry tool and save it in one of the following formats that the Design Manager accepts as input:

.1	Viewlogic schematic and wir
.sch	OrCAD schematic
.xnf	Xilinx hierarchical netlist
.pld	Xilinx (XC7000 only)

Starting the Design Manager

1. Open the Windows Program Manager window.
2. Open the Xilinx Program Group window.
3. Double click the Design Manager icon (see Figure 2-1).

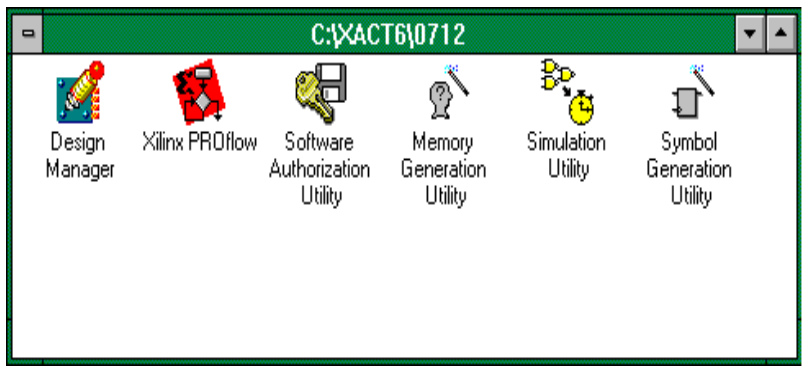


Figure 2-1 Design Manager Icon

The Design Manager window opens. Before you create a project, the window appears as shown in Figure 2-2. After you create a project, this window is configured for the device family that you specified in the input design.

Figure 2-2 The Design Manager Window with No Design

Obtaining Online Help

The Design Manager and Flow Engine have context-sensitive help and a Help menu. You can obtain help on commands and procedures through the Help menus or by selecting the Help toolbar button. In addition, the dialog boxes associated with many commands have a Help button that you can click on to obtain context-sensitive help.

Help Menu

Use the following Help menu commands to get help:

- The Contents command opens Help and lists the online help topics available for the Design Manager. From the Contents page, you can jump to command information or step-by-step instructions for using the Design Manager. Once you open help,

you can click the Contents button (first button on the left) in the Help window whenever you want to return to the Help contents.

- The Search for Help On command opens a dialog box in which you can search for a specific topic.
- The Tutorial command activates an interactive tutorial demonstrating some of the Design Manager procedures.

Toolbar Help Button

You can obtain context-sensitive help from the toolbar as follows:

1. Click on the Help button in the toolbar (see Figure 2-3).

Figure 2-3 Help Button

   The cursor changes to a question mark.

2. Click once with the left mouse button on the menu item or toolbar icon for which you want help.

   The Design Manager displays help for the selected command or option.

Note: Pressing the shift-F1 key combination is the same as selecting the Help toolbar button.

Help Button in Dialog Boxes

Many of the dialog boxes in the Design Manager have a Help button that you can click to obtain help on that dialog box.

Creating a New Project

After opening the Design Manager for the first time, you must create a new project for your design before you can use the Design Manger. The following procedure explains how to create a new project by importing and translating a design. This description of creating a new project applies to FPGA devices. See "Creating a New Project" on page 3-2 for a more complete description for creating a new project that also covers some extra features that apply only to the XC7000 family.

1. Select New Project from the File menu.

   The New Project dialog box appears as shown in Figure 2-4.

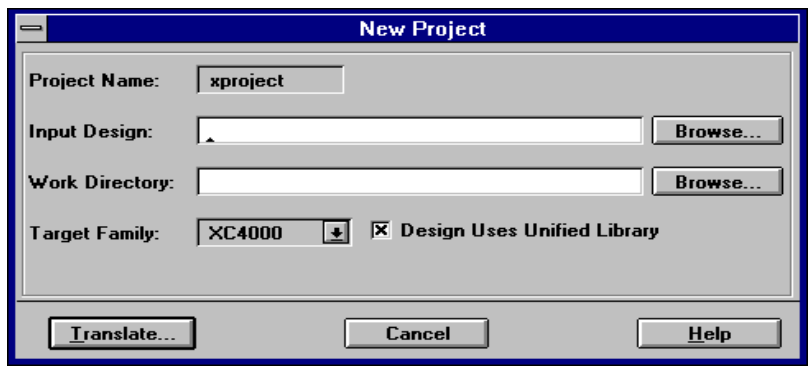


Figure 2-4 New Project Dialog Box (FPGA)

2. Type a project name in the Project Name box.

   The Design Manager creates a project directory with this name and locates it in the directory that you specify in the Work Directory box. The Design Manager uses the project directory to store all the data files for the project. The default name, xproject, is entered in the Project Name field when you open the New Project dialog box. The project name can consist of only alphanumeric characters and may not exceed eight characters in length.

Note: The project name must specify a directory which does not already exist.

3. Select the appropriate Target Family in the New Project dialog box (see Figure 2-4).

4. Enable the Design Uses Unified Library check box if your design uses the library elements from XACT 5.0 or later. Otherwise disable this check box. (This step does not apply to XC7000 and XC5200.)
5. Specify a design file to open using one of the following methods:
   - In the Input Design box, type the name of a design file to open.
   - If you don't know the file name click the Input Design Browse button. The Open dialog box appears in which you can select a design file to open (see Figure 2-5).

   You can open the following file types:

.1	Viewlogic schematic and wir
.sch	OrCAD schematic
.xnf	Xilinx hierarchical netlist
.pld	Xilinx (XC7000 only)

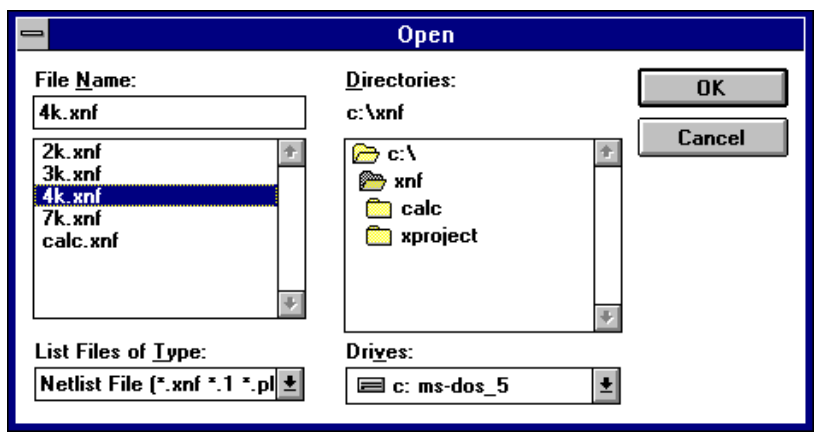


Figure 2-5 Open Dialog Box

6. In the New Project dialog box, type a directory name in the Work Directory box or click the Work Directory Browse button to open a directory selection dialog box in which you can specify a work directory. The work directory that you specify in this step will contain the new project directory that you specified in the Project Name box.

7. Click the Translate button to start the translate process and to close the New Project window.

   The Translate Options dialog box appears as shown in Figure 2-6. For more information on this dialog box, see "Translate Options Dialog Box Options" on page 4-49.

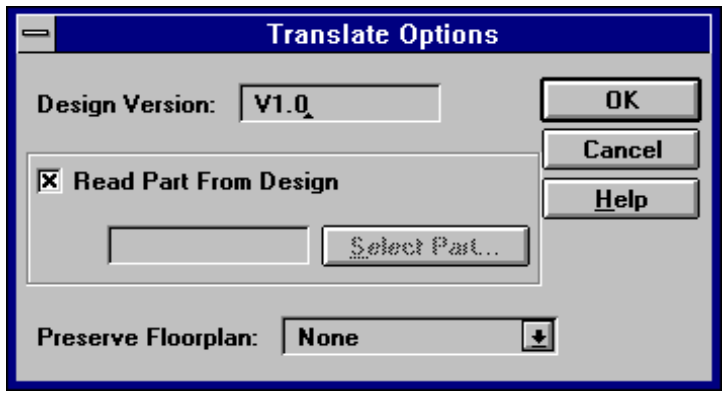


Figure 2-6 Translate Options Dialog Box

8. If you did not specify the device type in the design file using the PART attribute, deselect the Read Part From Design check box in the Translate Options dialog box, click on the Select Part button, and specify a part in the Part Selector dialog box that opens (see Figure 3-10).

   A translation dialog box appears, which translates the design into the internal Xilinx netlist format. When these translations are complete, a message box appears telling you that the translation completed successfully.

   If there are translation errors, a message box appears stating that translation failed. Click on the Review Log button to review the errors.

9. Select the OK button.

   After your design has loaded, the Design Manager window appears as shown in Figure 2-7.

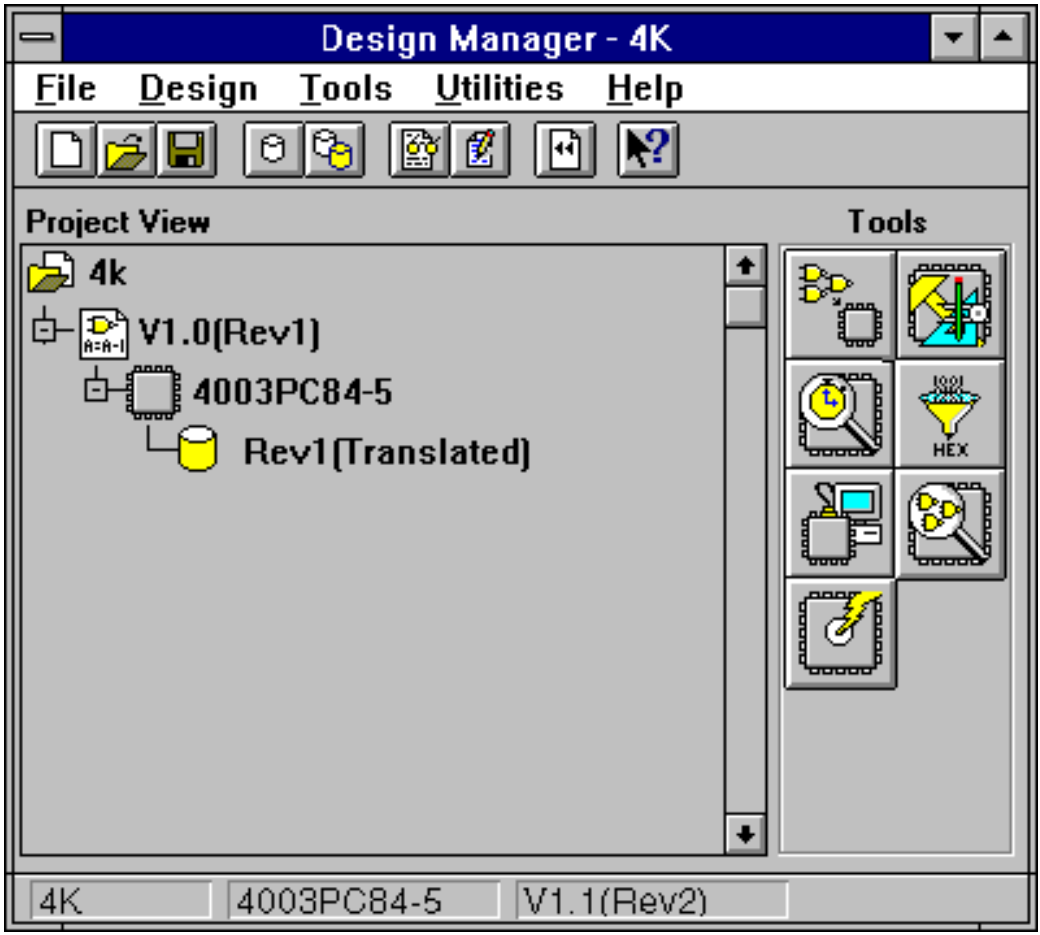


Figure 2-7 The Design Manager Window with a Design Loaded

Implementing the Design

The following procedure describes how to implement a design. There are two versions of the Flow Engine, read-only and configurable. This section uses the read-only Flow Engine.

1. Double click the desired Revision in the Project View (in the Design Manager Main Window). If you have just opened a new project, the implementation revision should look like Figure 2-8.

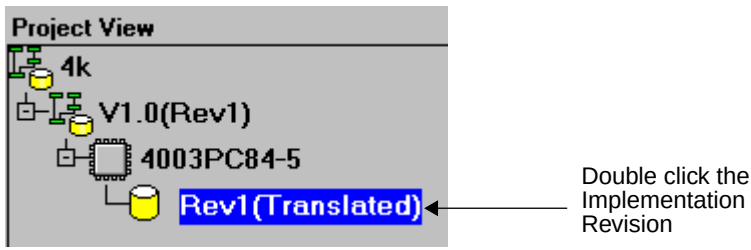


Figure 2-8 Starting the Flow Engine

Note: Instead of double clicking on the revision icon, you can select the revision icon and then select Implement from the Design menu.

2. The Design Implementation Options dialog box appears as shown in Figure 2-9.

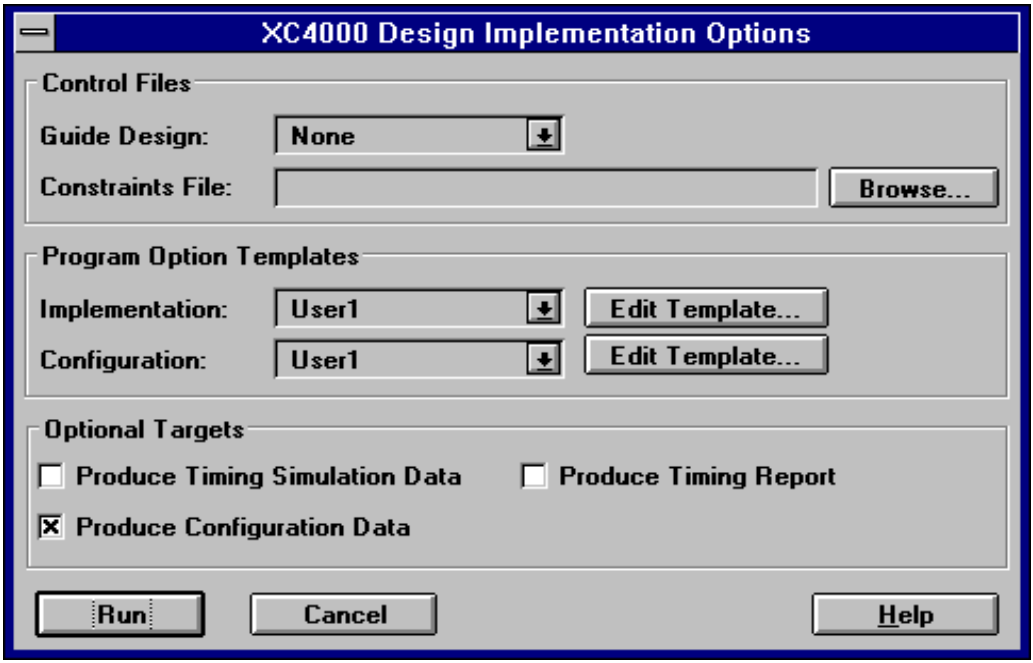


Figure 2-9 Design Implementation Options Dialog Box

3. Enable the Produce Timing Report, Produce Timing Simulation Data, and Produce Configuration Data options.
4. Click the Run button to implement the design.

   The Flow Engine window appears as in Figure 2-10. When processing is complete, the Flow Engine window closes. You can now view the reports as described in the next section.

   At this point you can also perform timing simulation, and program the device. Timing simulation is described in the Interface User Guide for your system. Device programming is described in the *Hardware & Peripherals User Guide*.

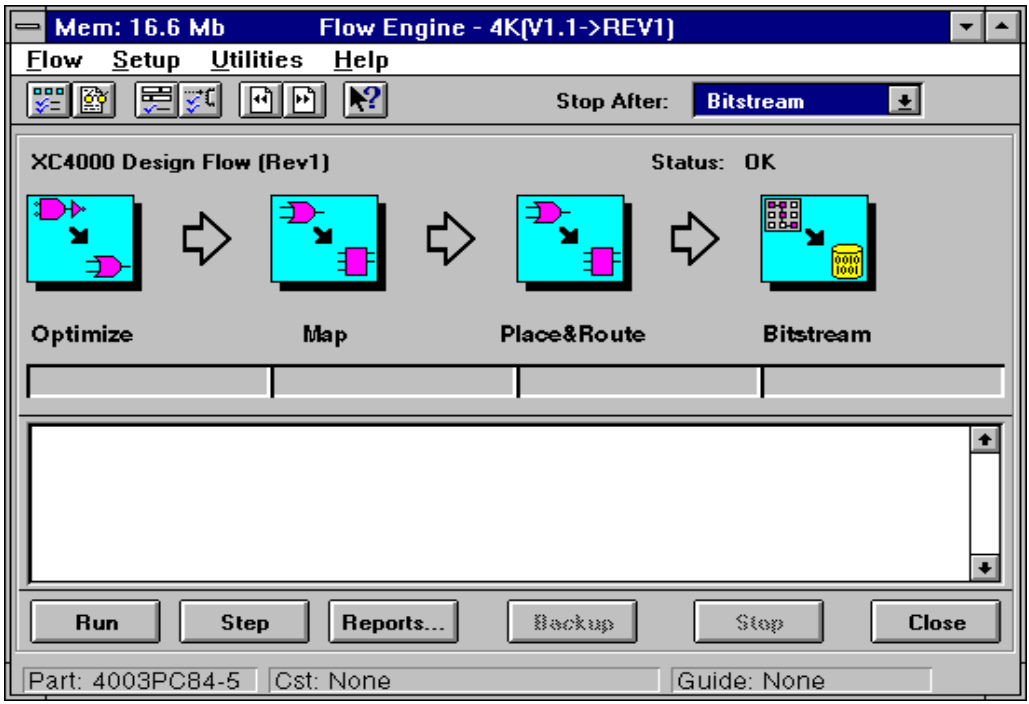


Figure 2-10 Flow Engine Window (Read-Only)

Viewing Reports

The Report Browser opens automatically when you select the Implement command. (To open the report browser at another time, select Report Browser from the Utilities menu.) The Report Browser window appears as shown in Figure 2-11.

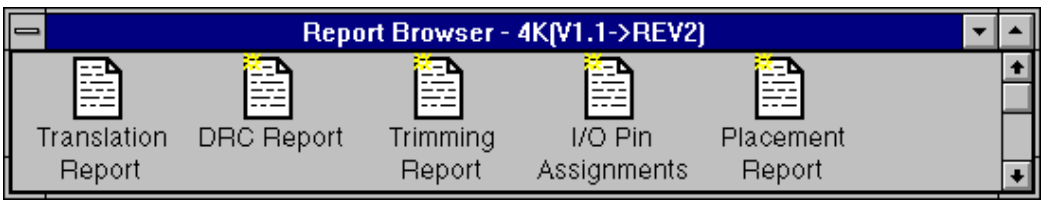


Figure 2-11 Report Browser

Double click on the Translation Report icon. The report appears in its own window, as shown in Figure 2-12. As the Flow Engine executes various steps, corresponding reports become available in the Report Browser.

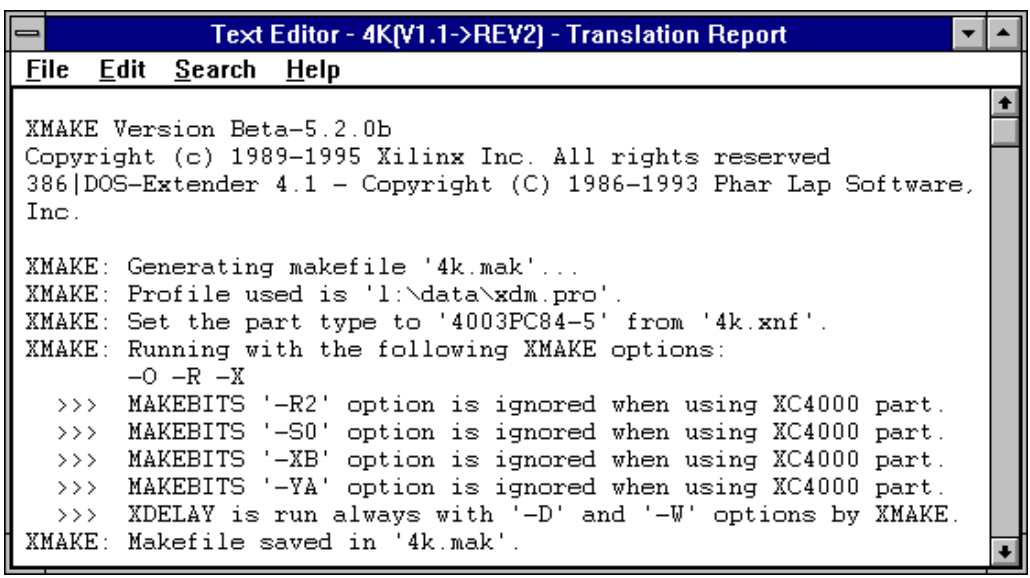


Figure 2-12 Translation Report

You can save the report to an ASCII file using the Save As command in the File menu, print the report using Print command in the File menu, or close the report window using Exit command in the File menu. Select these commands from the Text Editor window, not the main Design Manager window.

Chapter 3

Using the Design Manager

This chapter shows you how to perform common design tasks in the Design Manager and Flow Engine. It describes the following procedures:

- Creating a New Project
- Creating a New Design Version
- Deleting Items from the Project View
- Targeting a New Device
- Creating a New Implementation Revision
- Specifying Implementation Options
- Creating a New Template
- Setting Custom Template Options
- Constraining a Design
- Guiding a Design
- Configuring the Flow
- Setting a Run Target
- Producing Timing Simulation Data
- Viewing Reports
- Using the Floorplanner
- Using the Partitioner

Creating a New Project

A project includes all design versions, device implementations, implementation revisions, reports, and any other Xilinx data created as you work with a design. The Design Manager graphically displays information about these items in the Project View. When you create a new project, you specify a design to open, a device to target, and a directory for the project.

The Design Manager, translates the design into a Xilinx file format and sets up the appropriate files in the project directory. The Design Manager does not copy input schematic files since it works with the translated Xilinx netlist. You can create as many projects as you wish, but you can only work with one at a time.

To Create a New Project

1. Select New Project from the File menu.

   The New Project dialog box appears as shown in Figure 3-1 for FPGA devices and in Figure 3-2 for XC7000 EPLD devices.

2. Type a project name in the Project Name box.

   The Design Manager creates a project directory with this name and locates it in the directory that you specify in the Work Directory box. The Design Manager uses the project directory to store all the data files for the project. The project name must specify a directory which does not already exist. The project name can consist of only alphanumeric characters and may not exceed eight characters in length.

3. Select the appropriate Target Family in the New Project dialog box (see Figure 3-1 and Figure 3-2).

4. If you are using an XC7000 family device, select either the Single Chip Design or Multi Chip Design check box (see Figure 3-2).

5. Enable the Design Uses Unified Library check box if your design uses the library elements from XACT 5.0 or later. Otherwise disable this check box. (This step does not apply to XC7000 and XC5200.)

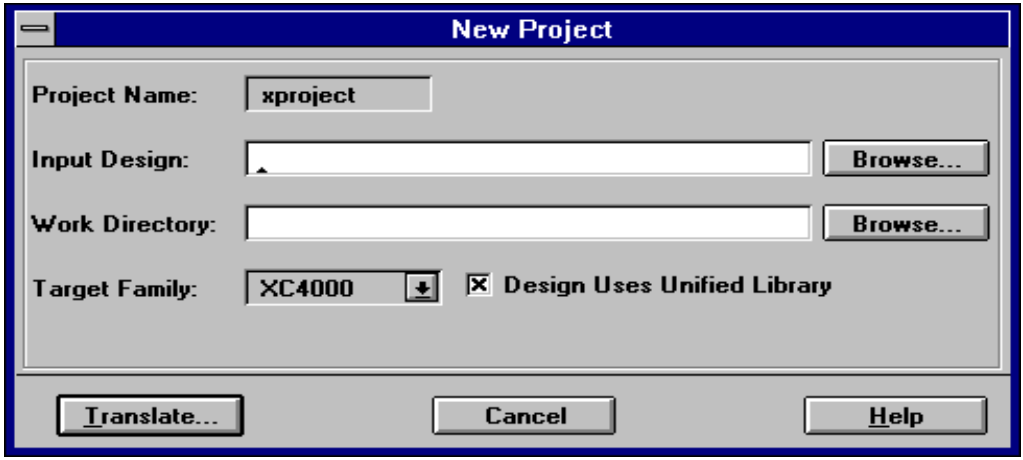


Figure 3-1 New Project Dialog Box (FPGA)

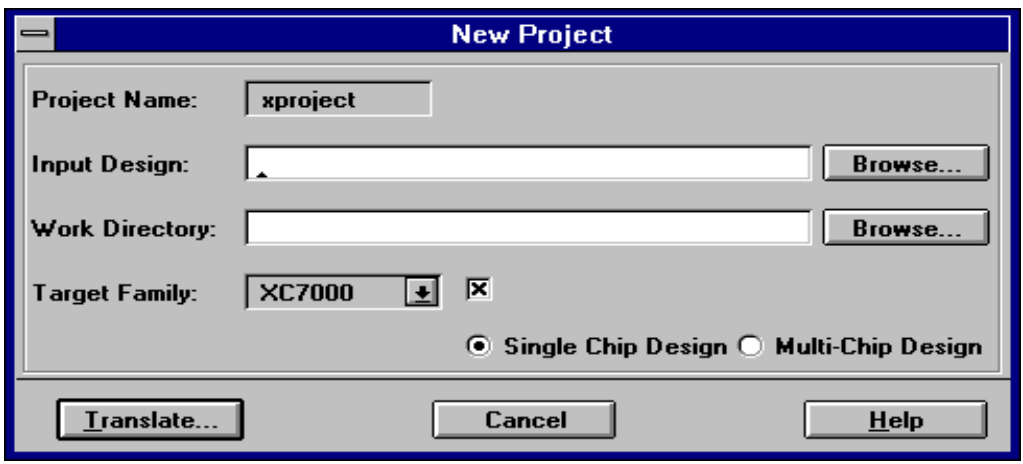


Figure 3-2 New Project Dialog Box (EPLD Devices)

6. Specify a design file to open using one of the following methods:
   - In the Input Design box, type the name of a design file to open.
   - If you don't know the file name, click the Input Design Browse button. A file selection dialog box opens in which you can select a design file to open (see Figure 3-3).

   You can open the following file types:

.1	Viewlogic schematic and wir
.sch	OrCAD schematic
.xnf	Xilinx hierarchical netlist
.pld	Xilinx (XC7000 only)

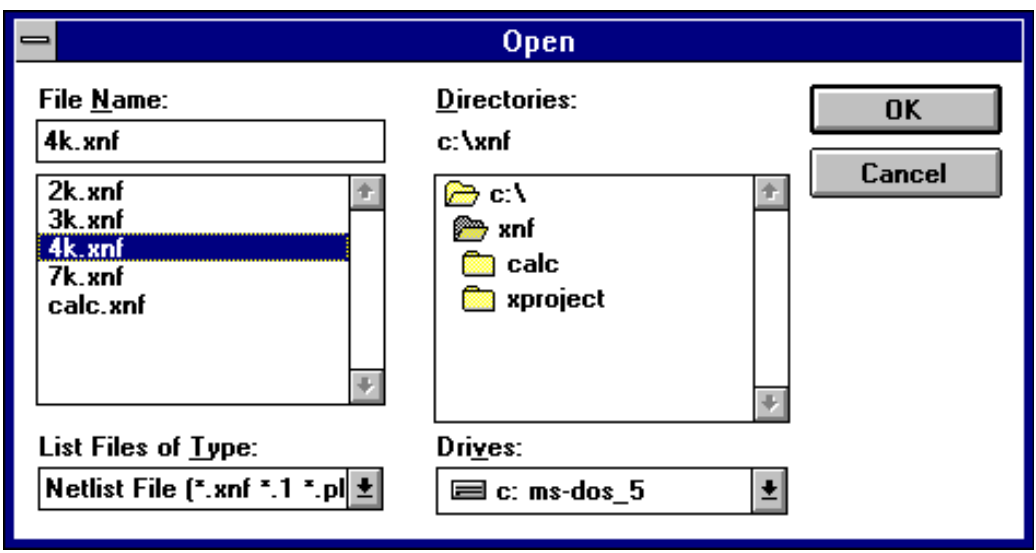


Figure 3-3 Open Dialog Box

7. In the New Project dialog box, type a directory name in the Work Directory box or click the Work Directory Browse button to open a directory selection dialog box in which you can specify a work directory. The work directory that you specify in this step will contain the new project directory that you specified in the Project Name box.

8. Click the Translate button to start the translation process and to close the New Project window.

   The Translate Options dialog box appears as shown in Figure 3-4. For more information on this dialog box, see "Translate Options Dialog Box Options" on page 4-49.

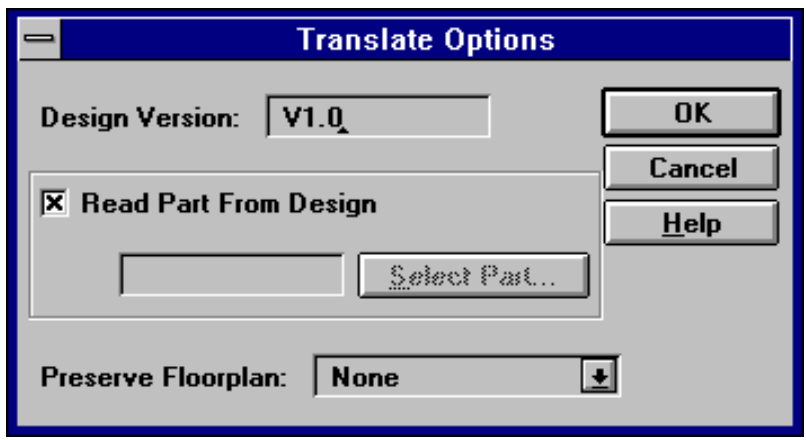


Figure 3-4 Translate Options Dialog Box

9. If you did not specify the device type in the design file using the PART attribute, deselect the Read Part From Design check box in the Translate Options dialog box, click on the Select Part button, and specify a part in the Part Selector dialog box that opens (see Figure 3-10).

   A translation dialog box appears, and the Design Manager translates the design file into an XFF file. When these translations are complete, a message box appears telling you that the translation completed successfully.

10. Select the OK button.

    After your design loads, the Design Manager window appears as shown in Figure 3-5. If you are using a Multi Chip EPLD Device, the Design Manager window appears as shown in Figure 3-6.

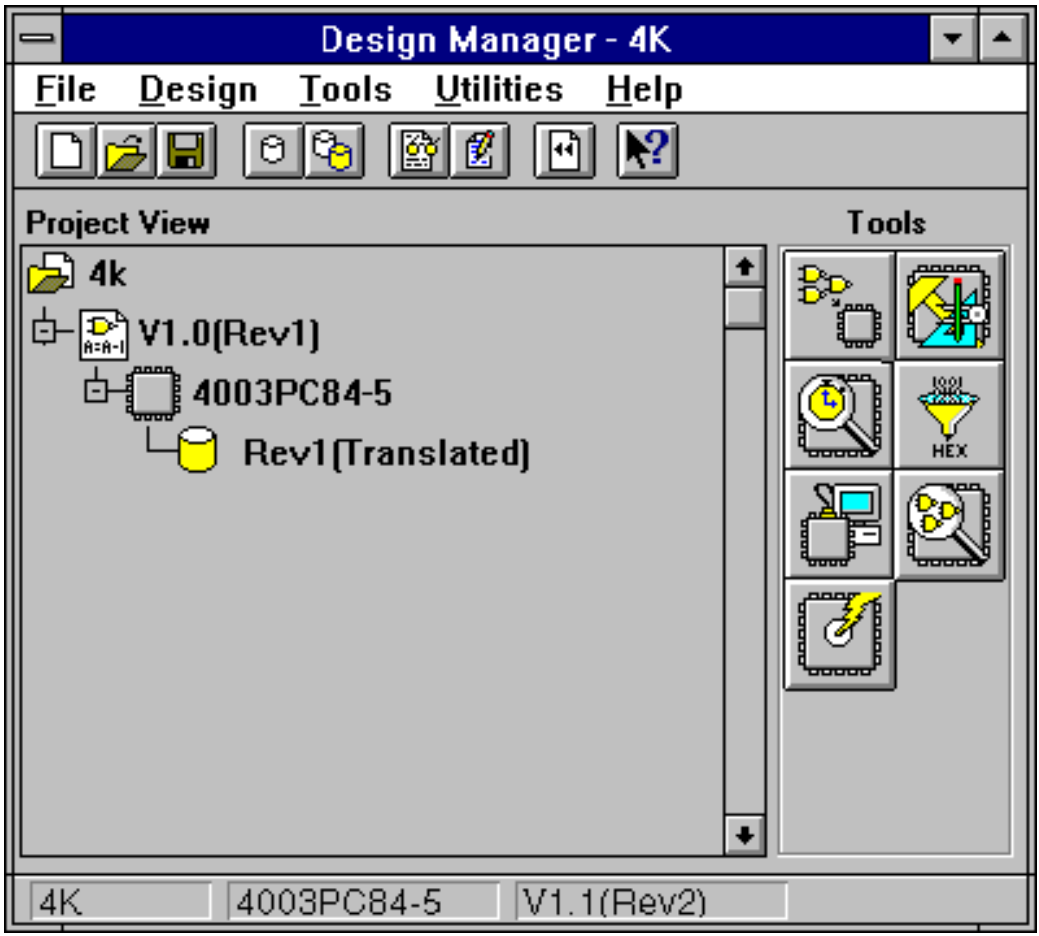


Figure 3-5 The Design Manager Window with a Design Loaded

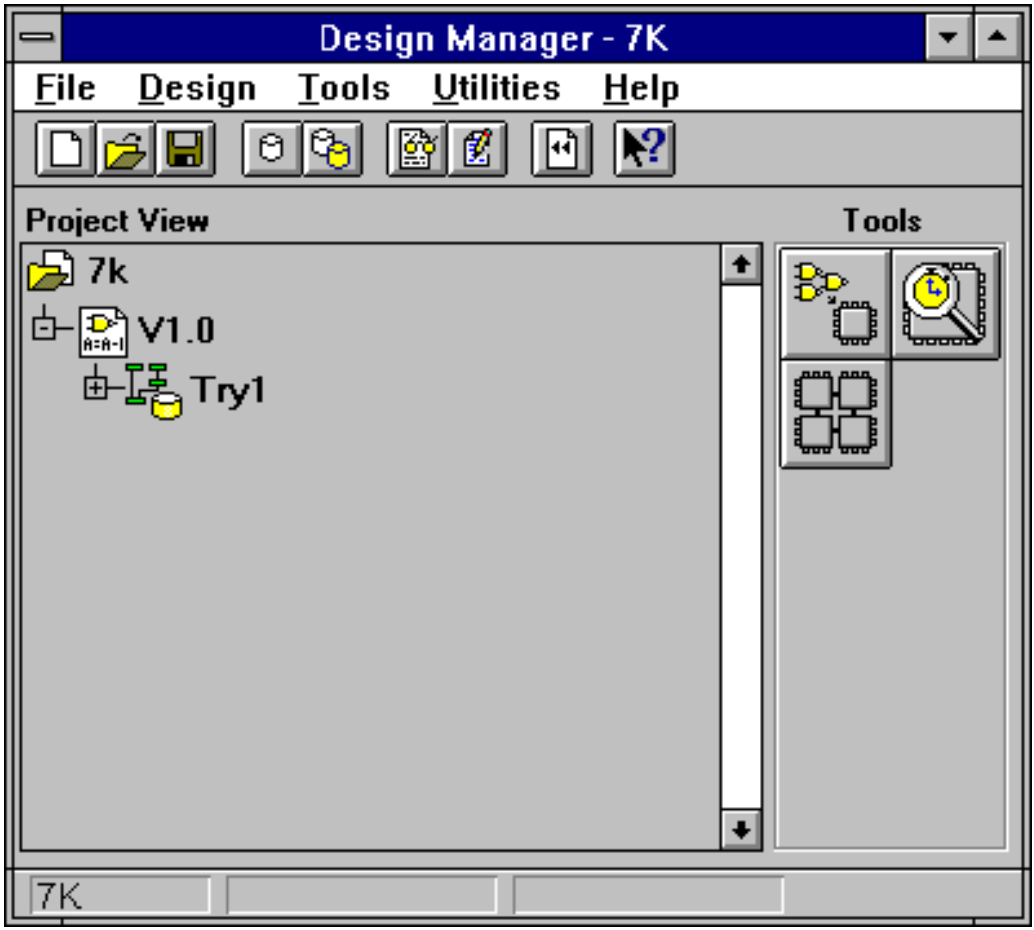


Figure 3-6 Design Manager Window with a Multi-Chip EPLD Design Loaded

Creating a New Design Version

While working on a project, you may need to modify the initial input design and bring these changes into an existing project in the Design Manager. You can do this with the Translate command in the Design menu. The Design Manager reads the modified input design file, translates it into a Xilinx netlist, and creates a new design version in the Project View. The Design Manager automatically assigns a name for the Design Version, but you can enter a different name in the Translate Options dialog box.

To Create a New Design Version

1. Choose Translate from the Design Manager's Design menu.

   The Translate Options dialog box appears as shown in Figure 3-7. For more information on this dialog box, see "Translate Options Dialog Box Options" on page 4-49.

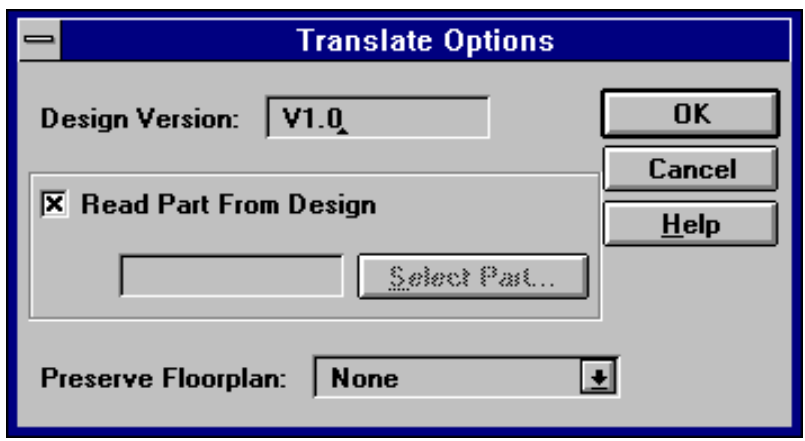


Figure 3-7 Translate Options Dialog Box

2. Type a name in the Design Version box if you want a name other than the default name in this box.
3. Specify the part type by doing one of the following:
   - Enable the Read Part From Design check box to use the part type specified in the design.

- To specify a part without regard to what is specified in the design, disable the Read Part From Design check box and specify a part using the Select Part button in the Translate Options dialog box. This opens the Part Selector window shown in Figure 3-8.

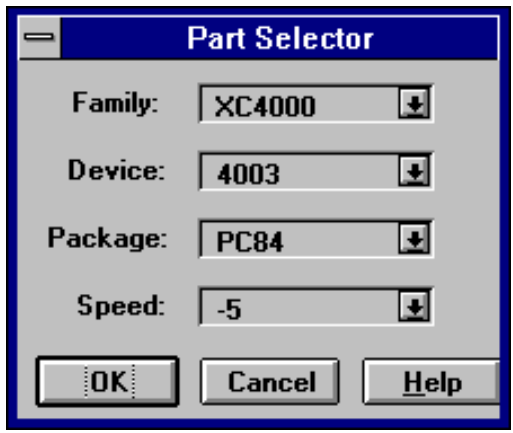


Figure 3-8 Part Selector

4. Click the OK button in the Translate Options dialog box.

   The Translate window appears and displays messages as the Design Manager translates the design. At the end of the translation, a dialog box (see Figure 3-9) appears saying that the translate process completed successfully.

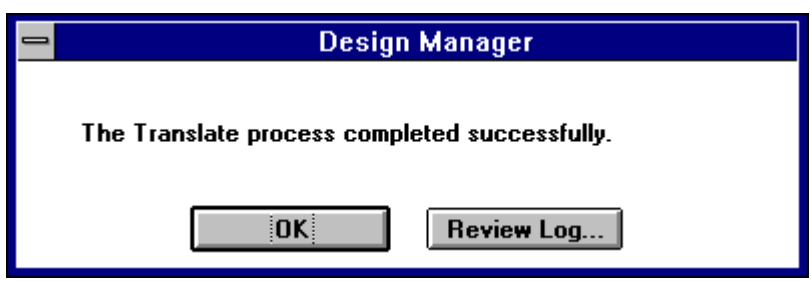


Figure 3-9 Translation Dialog Box

5. In this dialog box, click Review Log to view the log in the Text Editor or click OK to exit the dialog box.

The Design Manager creates a new version icon in the Project View.

Deleting Items from the Project View

Use the Delete command to delete a version, device, or revision from the project view.

Warning: When deleting an item from the Project View, the Design Manager immediately deletes the item and all accompanying data, and removes its icon from the Project View. Data which is deleted can not be recovered.

To Delete an Item from the Project View

1. Use the left mouse button to select a version, device, or revision icon in the Project View that you wish to delete.
2. Do one of the following:
   - Choose Delete from the Design Manager's Design menu.
   - Click the right mouse button in the Project View and select Delete from the popup menu.
   - Press the Delete Key on your keyboard.

   The Design Manager deletes the selected item and all accompanying data, and removes its icon from the Project View.

Targeting a New Device

You can target your design into any number of different devices within a target family; each is called an implementation. This allows you to try your design in different devices in order to determine the most suitable fit. For example, if a particular device proves to be too large or too slow for your needs, you can select a new target device which is smaller or faster. You can delete old target device attempts which are no longer useful.

To create a new device implementation in the Design Manager, use the New Device command in the Design menu.

You may only target a new device which is within the same family specified at the time of project creation. Only the options that are compatible with the original input design file are displayed in the Part Selector dialog box. For example, if your input design specifies a XC4000, you can only specify an XC4000, XC4000A, XC4000D, XC4000E, or XC4000H family.

To target a new device in a different family, you must make the appropriate changes to the input design file and create a new project.

To Target a New Device

1. In the Project View, click on the design version icon for which you want to target a new device.
2. Choose New Device from the Design Manager's Design menu.

   The Part Selector dialog box opens as shown in Figure 3-10.

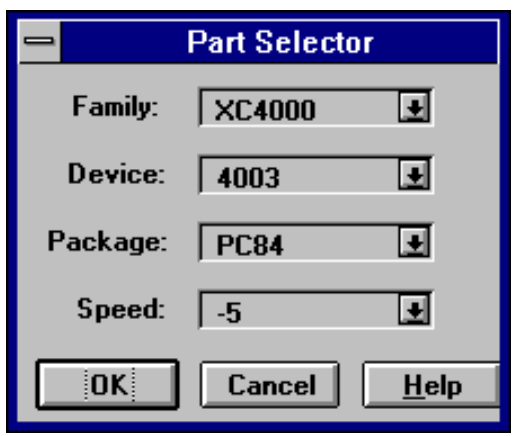


Figure 3-10 Part Selector

3. Specify the desired settings in the Family, Device, Package, and Speed pulldown menus.
4. Click OK.

Creating a New Implementation Revision

After you create a design version by translating your design, and you choose a target device (or devices), you can try different implementation strategies on that design. This allows you to vary how your design is implemented in order to achieve your design objectives. For example, you can maximize speed and density for specific functions in your design by controlling the implementation process. Each of these implementation strategies is called an implementation revision. Each implementation revision contains the output files and reports that are created based on a specific set of implementation strategies. You can delete implementation revisions that are no longer useful.

When you create a project, a revision icon is placed in the Project View with the status indicated as translated. As you process the implementation, its status (i.e. routed or placed) is indicated next to its icon in the Project View.

You use the New Revision command in the Design menu to create a new revision. This creates a revision that contains just the translated netlist and the status is "translated."

To Create a New Implementation Revision

1. In the Design Manager Project View, select the device implementation under the design version that you wish to work with.
2. Do one of the following:
   - Choose New Revision from the Design Manager's Design menu.
   - Click the right mouse button in the Project View and select New Revision from the popup menu.

   The Design Manager creates a new revision and displays its icon in the Project View.

Specifying Implementation Options

You can specify options that control how the Flow Engine implements a design and configures a device, and whether it generates reports, timing data, and configuration data. The available options depend on the target device family.

There are two types of option templates, implementation and configuration. The Implementation Template controls how the Flow Engine places, routes, and optimizes a design. The Configuration Template sets options which define the initial configuration sequence of a device, the start-up conditions, and readback capabilities.

You can create and edit option templates with the Template Manager command in the Utilities menu. You can also modify existing templates in the Design Implementation Options dialog box and in the Flow Engine.

To Specify Implementation Options

1. Open the Design Implementation Options dialog box (see Figure 3-11) using one of the following methods:
   - From the Design Manager's Design menu, choose Implement.
   - From the Flow Engine's Setup menu, choose Options.
   - In the Project View, select a design revision, press the right mouse button, and select Implement from the popup menu.
   - In the Project View, double click on the design revision icon.

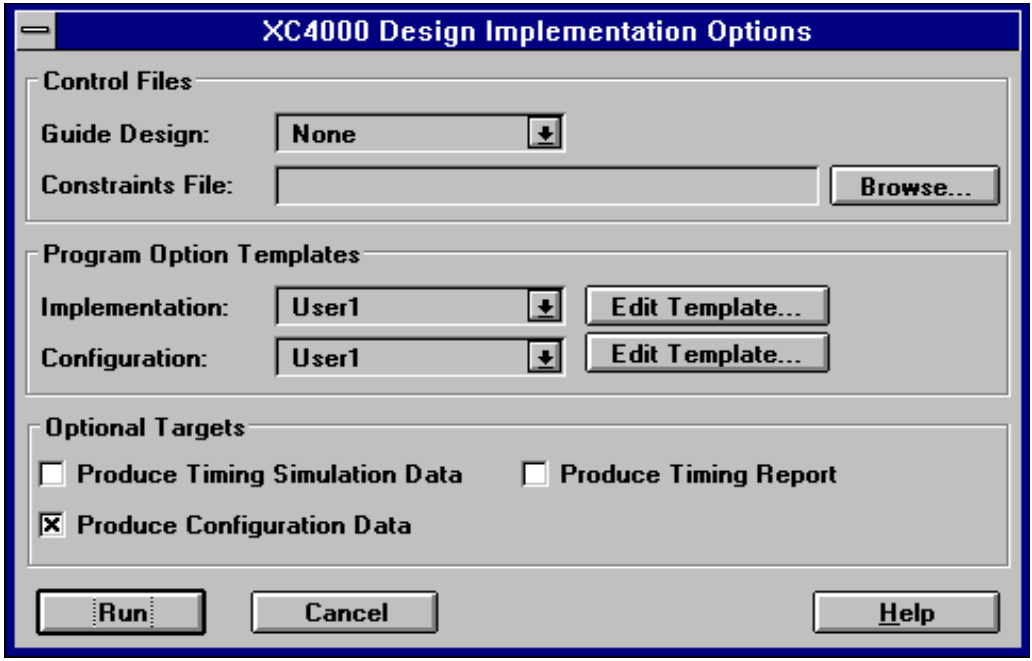


Figure 3-11 Design Implementation Options Dialog Box

2. Make the desired settings in the Design Implementation Options dialog box. Select Implementation Edit Template or Configuration Edit Template to set the options in the option templates.

   There are many options in the Design Implementation Options dialog box. For a complete explanation of what these options do and how to set them, see "Implementation Options" on page 5-1.

3. Exit the Design Implementation Options dialog box by doing one of the following:

   - If you opened the Design Implementation Options dialog box from the Design Manager, click Run to exit the dialog box and start a compile in the Flow Engine.
   - If you opened the Design Implementation Options dialog box from the Flow Engine, click OK to exit the dialog box.
   - Click Cancel to exit the Design Implementation Options dialog box without making any changes.

Creating a New Template

An option template is a set of option settings. Templates provide a convenient way to have several sets of option settings that you can select from when you implement a design. For example, you can have a template for quick place and route and another one for maximum effort place and route.

You can create additional templates with the Template Manager utility.

There are two types of option templates. They are implementation templates and configuration templates. You can create these templates as described below.

To Create a New Template

1. In the Design Manager or Flow Engine, select Template Manager from the Utilities menu.

   The Template Manager dialog box opens as shown in Figure 3-12.

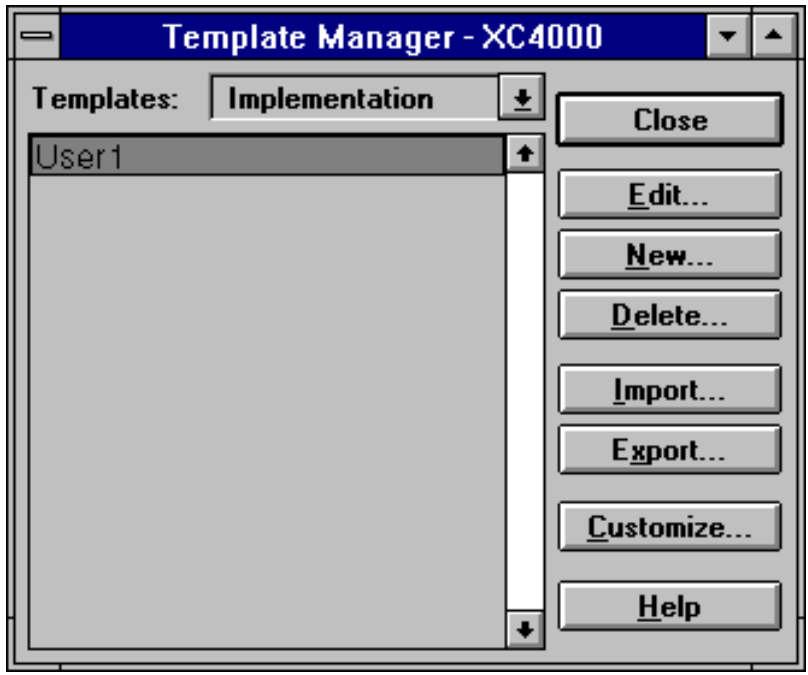


Figure 3-12 Template Manager

2. Specify the type of template you wish to create by selecting either Implementation or Configuration from the Template popup menu in the Template Manager dialog box.
3. Click the New button.

   The Name dialog box opens as shown in Figure 3-13.

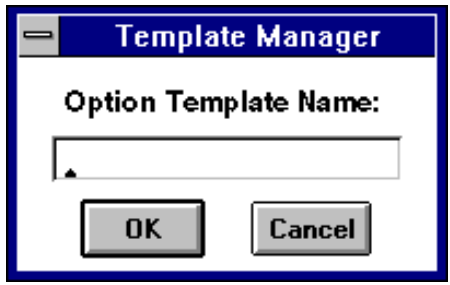


Figure 3-13 New Template Dialog Box

4. Type a name for the new template.
5. Click OK.

   The name of the new template is added to the Option Templates list in the Template Manager dialog box. At this point you can exit the Template Manager. But since you have just created a new template you probably want to edit the options.
6. In the Template list in the Template Manager dialog box, click on the name of the new template.
7. Click the Edit button.

   The Implementation Template dialog box or Configuration Template dialog box opens depending on which type of template you are working with.
8. Specify the desired settings. The available settings depend on the device family and the template type.

   See Chapter 5, “Implementation Options” for information on how to set the options in the Implementation Template and Configuration Template dialog boxes.
9. When you are finished, click OK.

   The Design Manager saves the options settings and closes the Template dialog box.
10. Click the Close button to exit the Template Manager.

Setting Custom Template Options

The options available in the Option templates permit you to set the most commonly used options. However, you may wish to set more advanced options. This capability is provided in the Template Manager.

For example, you can instruct the Design Manager to use PPR options that are not provided in the standard Design Manager template options.

For Implementation Templates, you can enter options for XNFPREP, XBLOX, XNFMAP (XC2000, XC3000, XC3000A), APR (XC2000, XC3000), and PPR (XC3000A, XC4000, XC5200). For Configuration Templates, you can enter options for MAKEBITS.

To Set Custom Template Options

1. Choose Template Manager from the Utility menu in either the Design Manager or Flow Engine.

   The Template Manager dialog box opens (see Figure 3-12).

2. Specify the type of template you want to work with by selecting either Implementation or Configuration from the Template popup menu in the Template Manager dialog box.

3. Select a template from the template list box in the Template Manager dialog box (see Figure 3-12).

4. Click on Customize.

The Custom Template Dialog box appears as shown in Figure 3-14.

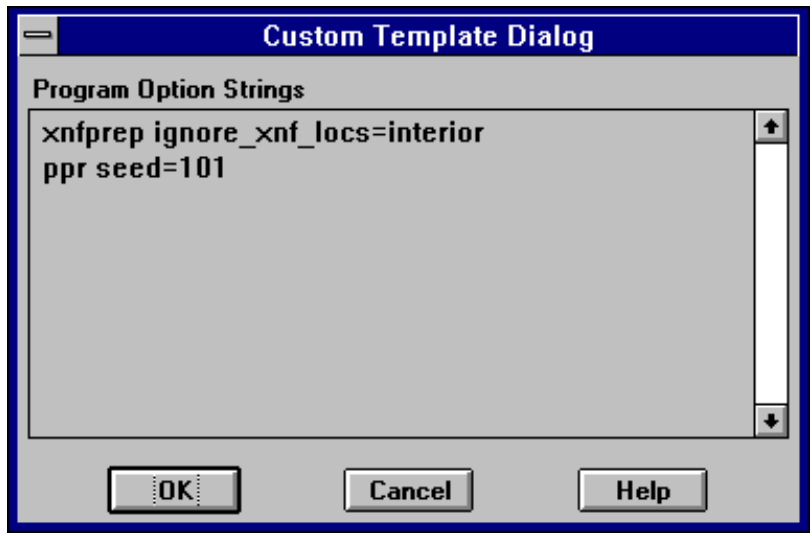


Figure 3-14 Custom Template Dialog Box

5. Type the program name in the Custom Template dialog box (see Figure 3-14) followed by the option and appropriate strings.

   You can enter any number of programs and options in this box. Start each line with the program name followed by the options for that program on the same line.

Warning: It is possible to enter options in the Custom Template dialog box that can conflict with normal Flow Engine options. It is beyond the scope of this manual to explain all the possible conflicts.

6. Click OK in the Custom Template dialog box.
7. Click Close in the Template Manager dialog box.

   When you implement the design, the Flow Engine uses the normal options as well as the custom options that are specified in the custom template.

Constraining a Design

You can use a constraints file (*design_name*.cst) to control the implementation of your design. The constraints file can contain information on where to place I/O pins and blocks of logic, and timing requirements for the design.

If you want to use a constraints file to control the implementation of your design, you can specify this file in the Design Implementation Options dialog box. The Flow Engine tries to implement your design to meet the specified timing requirements and other constraints.

To Specify a Constraints File

1. Open the Design Implementation Options dialog box using one of the following methods. See "Design Implementation Options Dialog Box" on page 5-1 for information on using this dialog box.
   - From the Design Manager Design menu, choose Implement.
   - From the Flow Engine Setup menu, choose Options.
   - In the Design Manager Project View, select a revision, press the right mouse button, and select Implement from the popup menu
2. In the Design Implementation Options dialog box, type the path to a constraints file or click the Constraints File Browse button to open a file selection dialog box in which to specify a constraints file.
3. Click OK.

   When you implement the design, the Flow Engine uses the specified file to constrain the implementation.

Guiding a Design

You can specify a previously placed and/or routed design revision to use as a guide for implementation. The software attempts to use the implemented revision as a guide for how to place logic and route signals for the current revision of the design. You can specify a Guide design in the Design Implementation Options dialog box which is described in the section "Design Implementation Options Dialog Box" on page 5-1.

For EPLD devices, a guide design has a different function. Each time you implement your design, a guide file is created (*design_name*.gyd) which contains your pinout information. You can re-use this file in subsequent iterations of your design if you want to keep the same pinouts. If you specify a valid guide file name in the Flow Engine window, the pinouts from that file will be used when the design is processed.

In some cases, you may want to use a guide file that was not generated from within the Design Manager. This is possible using the Advanced command in the Flow Engine's Setup menu. See "Advanced Command (Setup Menu)" on page 4-6 for more details on using an externally generated guide file.

To Specify a Guide Design

1. Open the Design Implementation Options dialog box using one of the following methods (see "Design Implementation Options Dialog Box" on page 5-1):
   - From the Design Manager Design menu, choose Implement.
   - From the Flow Engine Setup menu, choose Options.
   - In the Design Manager Project View, select a revision, press the right mouse button, and select Implement from the popup menu
2. Select a design in the Guide Design pulldown menu, which contains all the revisions available for you to use.
3. Click OK.

   When you implement the design, the Flow Engine uses the specified revision to guide the implementation.

Configuring the Flow

Use the Advanced command in the Flow Engine Setup menu to configure the implementation flow as well as certain aspects of the Flow Engine interface as follows:

- Use flashing icons to indicate that a process step is being processed. A trade-off of this feature is that flashing icons slow down the implementation process.

- Use separate steps for place and route or combine them into one place/route step. For the XC4000, you can have a separate map step (if floorplanning is desired) or have the mapping done in the place/route step(s). For the XC2000 and XC3000, the map step is always done separately.
- Specify guide files.
- Update the Design Manager and Flow Engine as to which implementation state was last completed. In normal Flow Engine use, you do not use this setting to change the implementation state. This setting is typically used if some processing on the design was performed outside of the Design Manager or Flow Engine framework. For example, if the design was routed using the Design Editor, the Implementation State should be set to Routed to inform the Design Manager and Flow Engine that this state is completed. You can also use this feature when you have used the Flow Engine's Backup button by mistake and want to reset the implementation state to its original state.

To Configure the Flow

1. Choose Advanced from Flow Engine Setup menu.

   The Flow Configuration dialog box opens (see Figure 3-15).

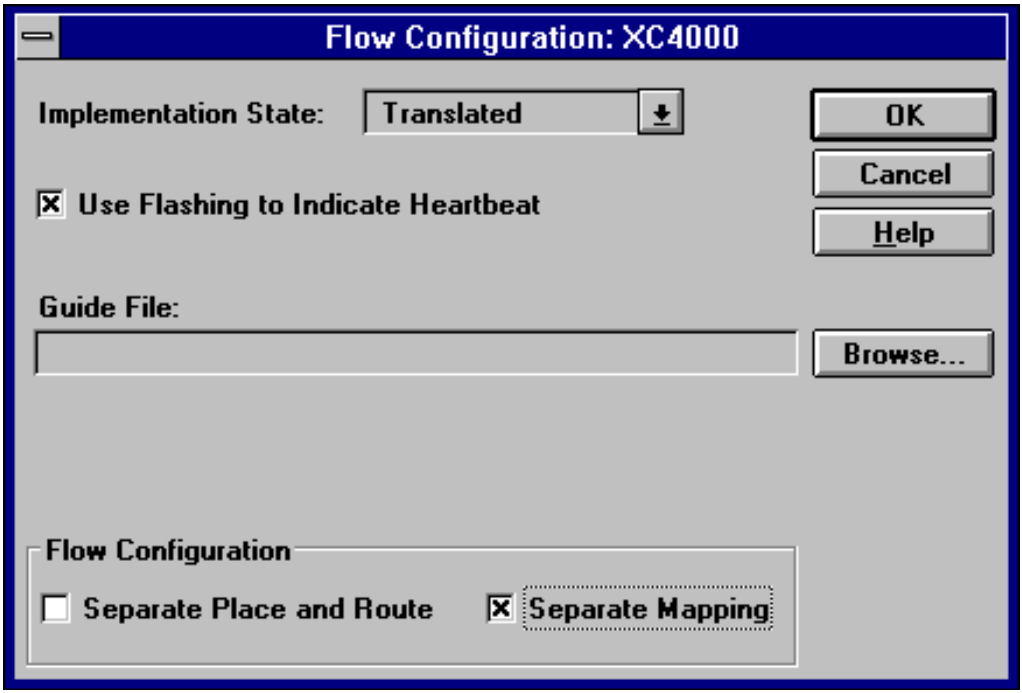


Figure 3-15 Flow Configuration Dialog Box

2. Specify the dialog box options. For a description of these options, see "Advanced Command (Setup Menu)" on page 4-6.
3. Click OK.

Setting a Run Target

The Flow Engine flow includes several process steps. You can specify that the flow stop at a certain point with the Stop After command. When specified, the Flow Engine does not process beyond that point. You do not need to set a run target for typical Flow Engine use. By default the Flow Engine processes all the steps.

To Set a Run Target

1. Select the desired Run target in the Stop After popup menu on the right side of the Flow Engine tool bar (see Figure 3-16).

This instructs the Flow Engine to stop processing after the specified point. The red stop sign visually indicates the Run target.

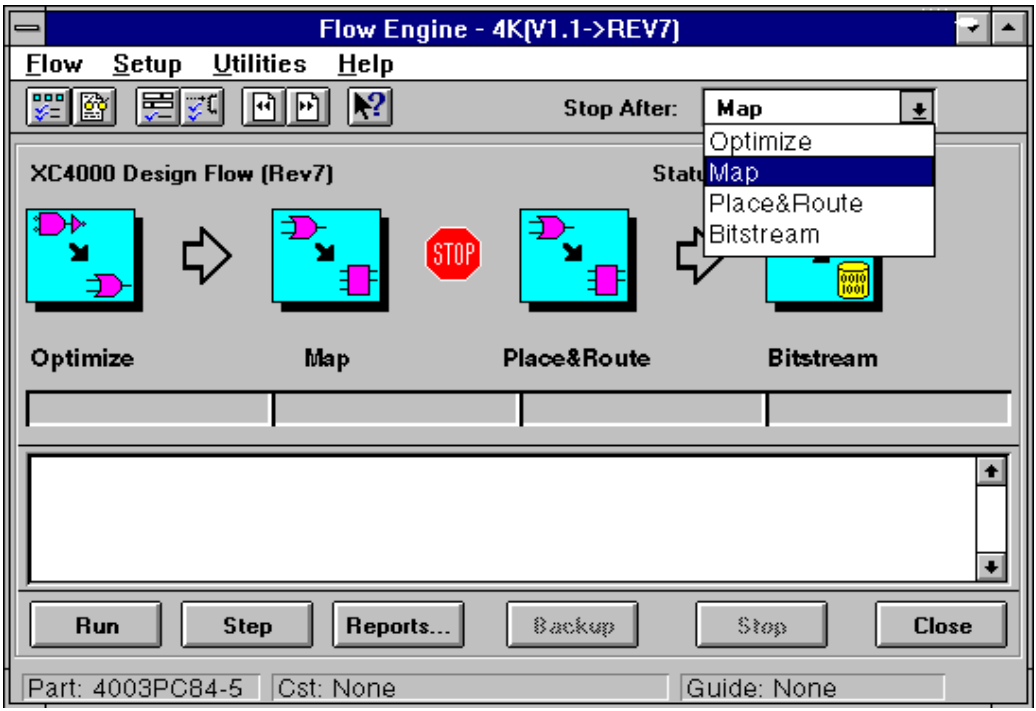


Figure 3-16 Flow Engine Window with a Run Target

Producing Timing Simulation Data

The Design Manager/Flow Engine can produce timing simulation data for use in a third party simulation tool.

To Produce Timing Simulation Data

1. Open the Design Implementation Options dialog box using one of the following methods (see "Design Implementation Options Dialog Box" on page 5-1):
   - From the Design Manager Design menu, choose Implement.
   - From the Flow Engine Setup menu, choose Options.

- In the Design Manager Project View, select a revision, press the right mouse button, and select Implement from the popup menu

2. In the Design Implementation Options dialog box, enable the Produce Timing Simulation Data check box.
3. Click OK.

   When you implement the design, the Flow Engine produces timing simulation data files. Each time the data is produced, it is automatically exported to your design directory. This usually means the same directory as your input design.

   You can now use these files to simulate the design with a supported third party simulation tool.

Viewing Reports

The Design Manager and Flow Engine generate various reports which you can view in the Report Browser.

To View Reports

1. Select the revision in the Design Manager Project View for which you wish to view reports.
2. To open the Report Browser, do one of the following:
   - Select Report Browser from the Utility menu in either the Design Manager or Flow Engine.
   - Click the Browse Reports button in either the Design Manager or Flow Engine toolbar.
   - Click the Reports control button at the bottom of the Flow Engine window.
   - Press the right mouse button in the Design Manager Project View window and select Reports from the popup menu.

   The Report Browser window opens and displays reports for the active revision (see Figure 3-17).

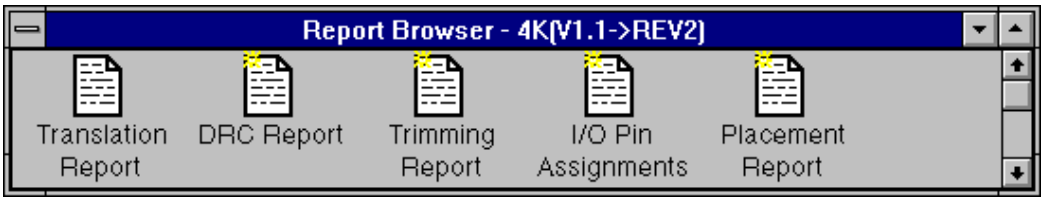


Figure 3-17 Report Browser Window

3. In the Report Browser window, double click on the report icon for the report you wish to view.

   Figure 3-18 shows the meaning of the icons in the Report Browser window. The report is displayed in the Text Editor (see Figure 3-19).

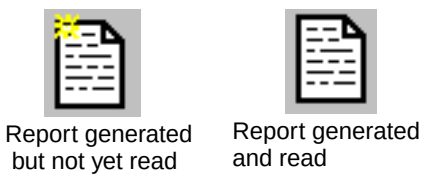


Figure 3-18 Key to Report Browser Icons

4. Use the Text Editor menu commands to work with the report information in the Text Editor (see "Text Editor Commands" on page 4-54).

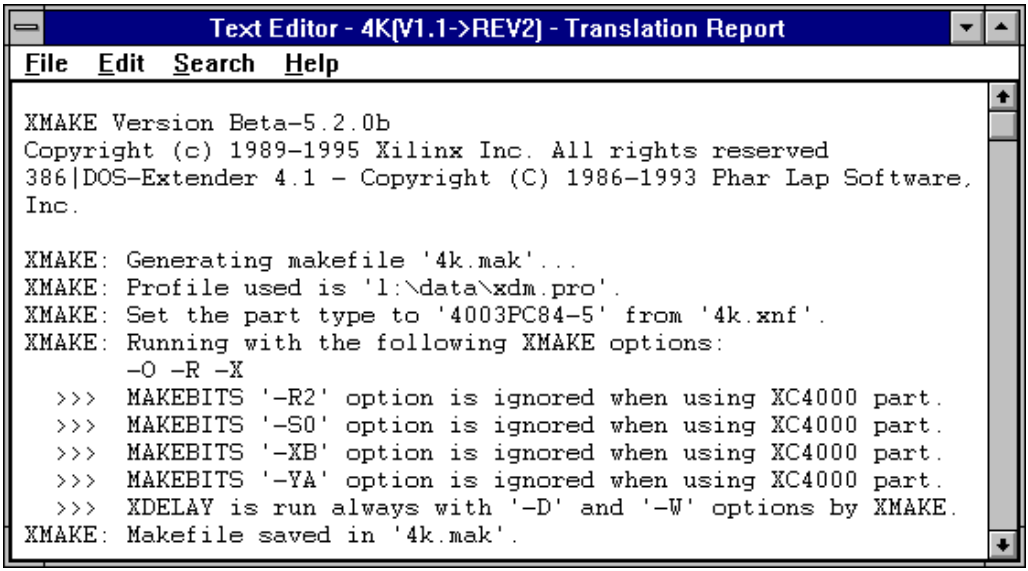


Figure 3-19 Text Editor Window

Using the Floorplanner

This section shows you how to run the Floorplanner from the Design Manager. The Floorplanner is only available for the XC3000A, XC4000, and XC5200 devices.

The Floorplanner requires a mapped design as input.This section covers how to create a mapped design after you have a project open in the Design Manager.

When you run the Floorplanner and save a constraints file and then want to implement the design in the Design Manager, you must specify the location of the CST file that you created in the Floorplanner.

This section covers the following steps:

1. Creating the map file
2. Running the Floorplanner
3. Specifying the CST file.

Creating a Map File

To use the Floorplanner, you must have a mapped design. If you try to open the Floorplanner without a mapped design, you will see the message in Figure 3-20.

Figure 3-20 Floorplanner Message

If you click OK, the Flow Engine automatically maps your design and then opens the Floorplanner. If you would like more control over this process, the following section describes how to map the design.

Mapping a Design

The following procedure describes how to map a design.

1. Select the desired Revision in the Project View (in the Design Manager Main Window) as shown in Figure 3-21.

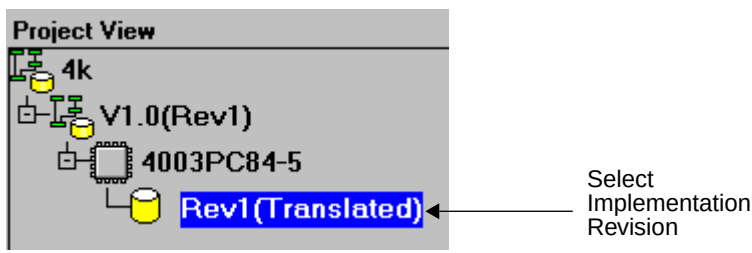


Figure 3-21 Selecting an Implementation Revision

2. Click on the Flow Engine button in the Design Manager's tool box (see Figure 3-22) to open the Flow Engine.

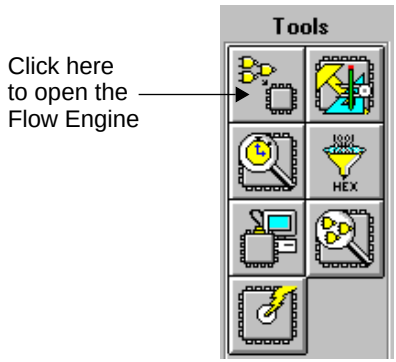


Figure 3-22 Opening the Flow Engine

The Flow Engine window opens (see Figure 3-23).

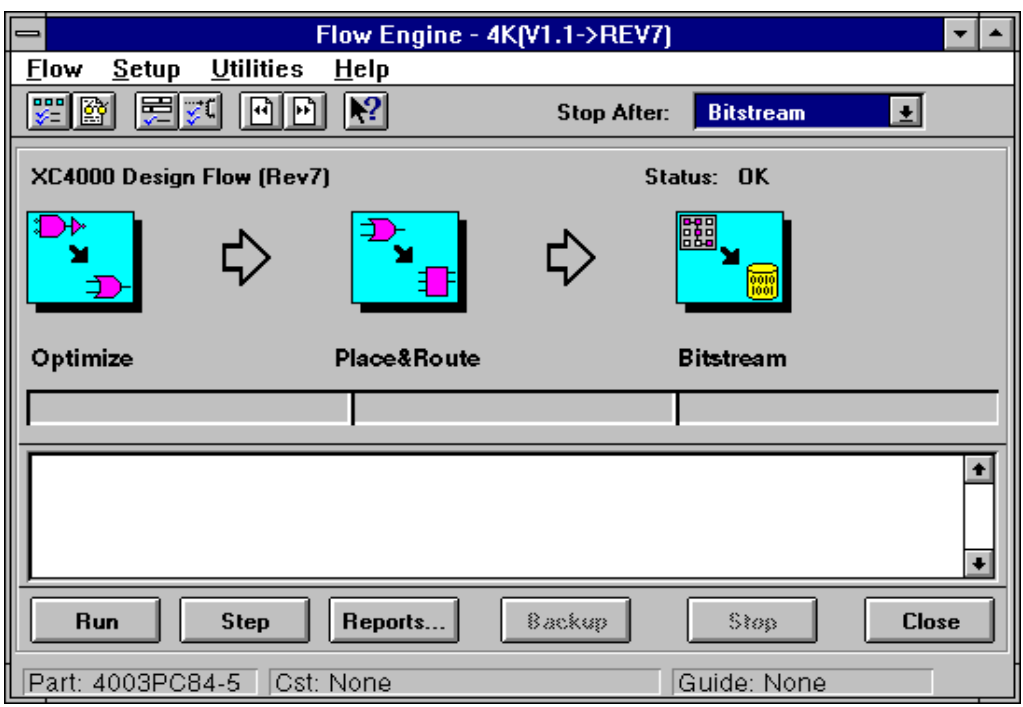


Figure 3-23 Flow Engine Window

3. If this is an XC4000 design, select Advanced from the Flow Engine's Setup menu and enable the Separate Mapping check box (see Figure 3-24).

   This causes the Flow Engine to separate the map step from the place and route step (see Figure 3-25).

4. Click OK to close the Flow Configuration dialog box.

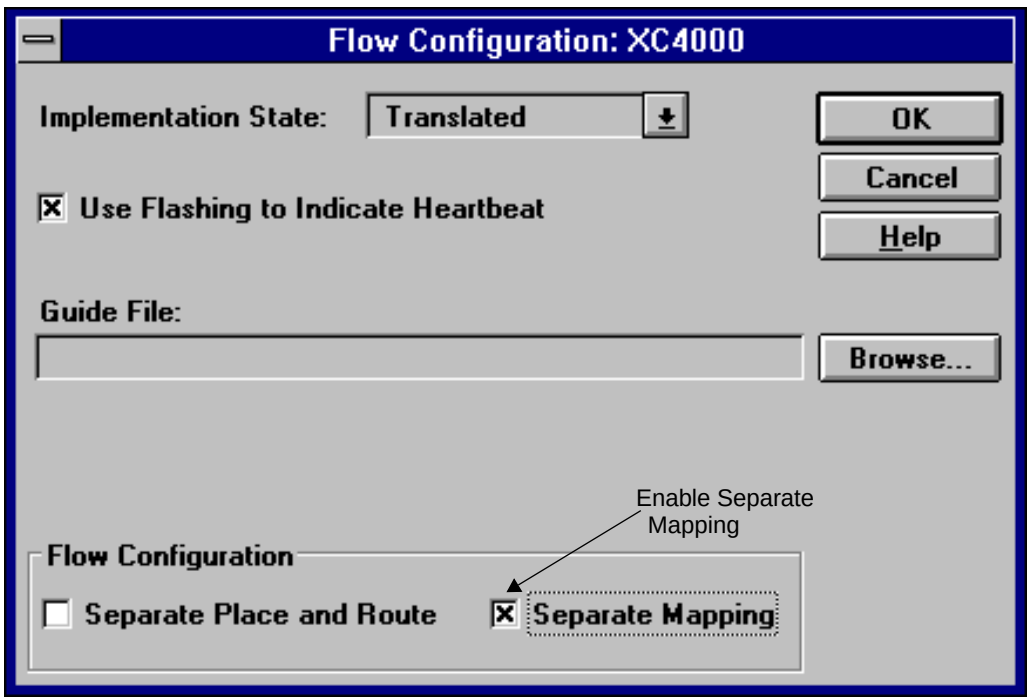


Figure 3-24 Flow Configuration Dialog Box

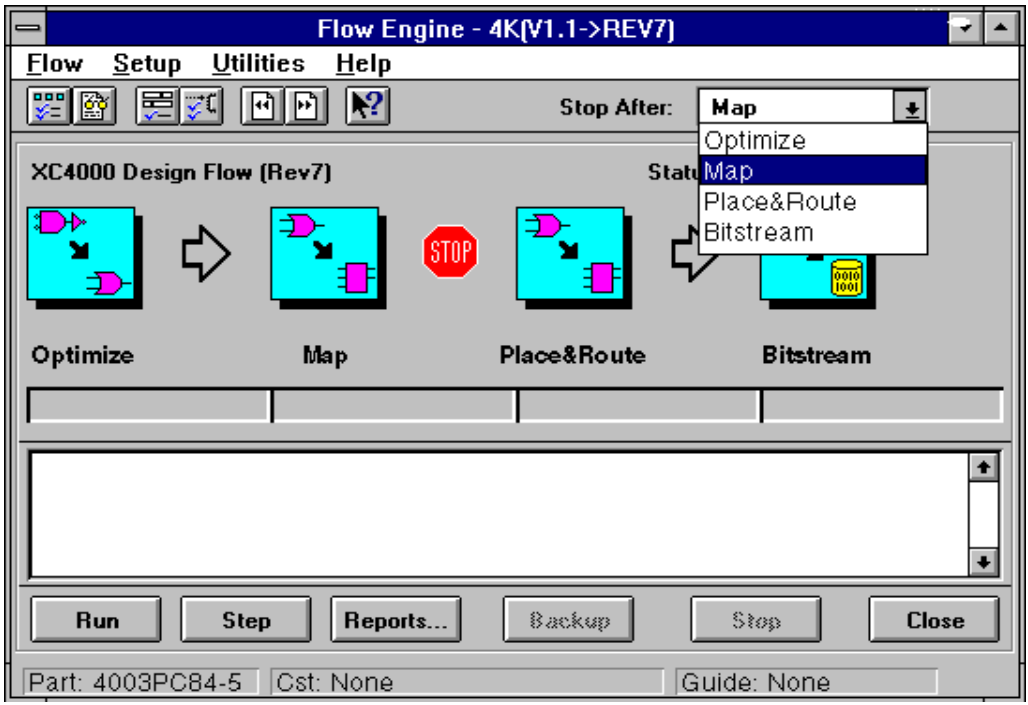


Figure 3-25 Flow Engine Window with Separate Optimize and Map Icons

5. Select Map in the Stop After popup menu on the right side of the Flow Engine tool bar. See Figure 3-25.

   This instructs the Flow Engine to stop processing after mapping.

6. Click the Flow Engine's Run button (lower left in Flow Engine Main Window).

   The Flow Engine optimizes and maps the design. At this point you have the necessary mapped design that is required in order to open the Floorplanner.

Running the Floorplanner

1. Start the Floorplanner by clicking on the Floorplanner icon in the Design Manager's Toolbox as shown in Figure 3-26.

   The Floorplanner window should open displaying your design.

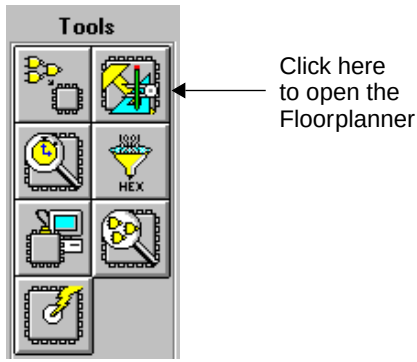


Figure 3-26 Toolbox

2. Floorplan the design.
3. Use the Write Constraints command in the Floorplanner's File menu to generate the .cst file for use with the Flow Engine.
4. Save the floorplan using the File Save command in the Floorplanner to preserve your floorplanning data.
5. Exit the Floorplanner to return to the Design Manager.

   For information on using the Floorplanner, refer to the *Floorplanner Reference/User Guide*.

Specifying the CST File

After working with a design in the Floorplanner, you will have created a constrains (CST) file. To use this CST file, you specify the file in the Constrains File box in the Design Implementation Options dialog box (see Figure 3-27).

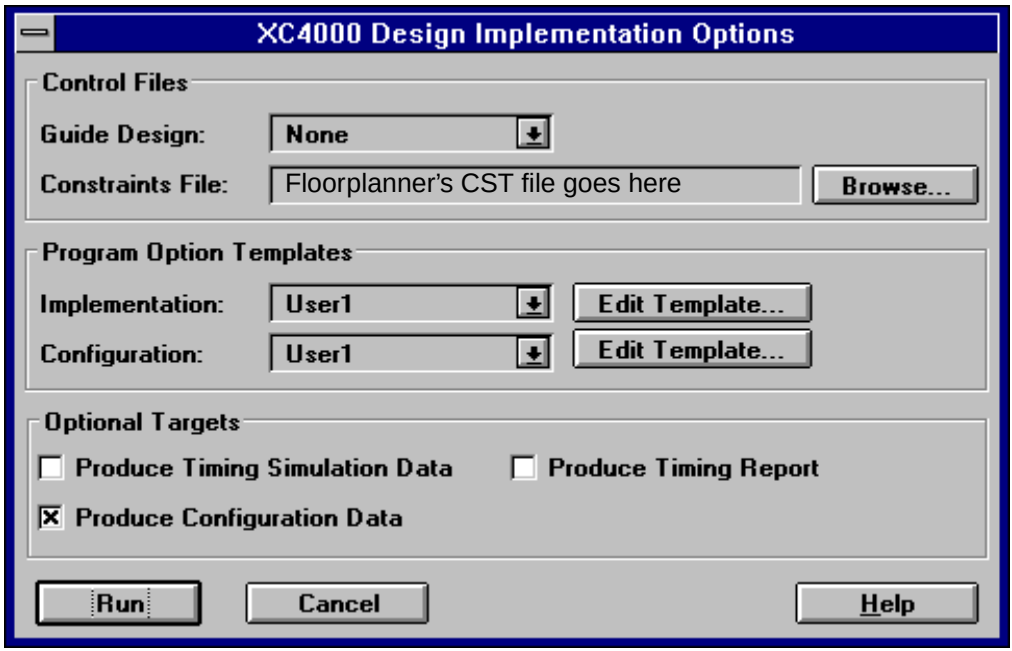


Figure 3-27 Specifying a Constraints File

Using the Partitioner

The Partitioner allows you to easily fit your design into multiple target EPLD devices. The Partitioner is only available for the XC7000.

To partition your design into two or more target devices, do the following:

1. Create a new project and select Multi-Chip Design.

   If you have a project that was originally intended for one target device, you can partition it into multiple devices by doing the following:

   a) Save the single-chip project.

   b) Open the project with the New Project command, as shown in Figure 3-28.

c) Select Multi-Chip Design.

d) Click Translate.

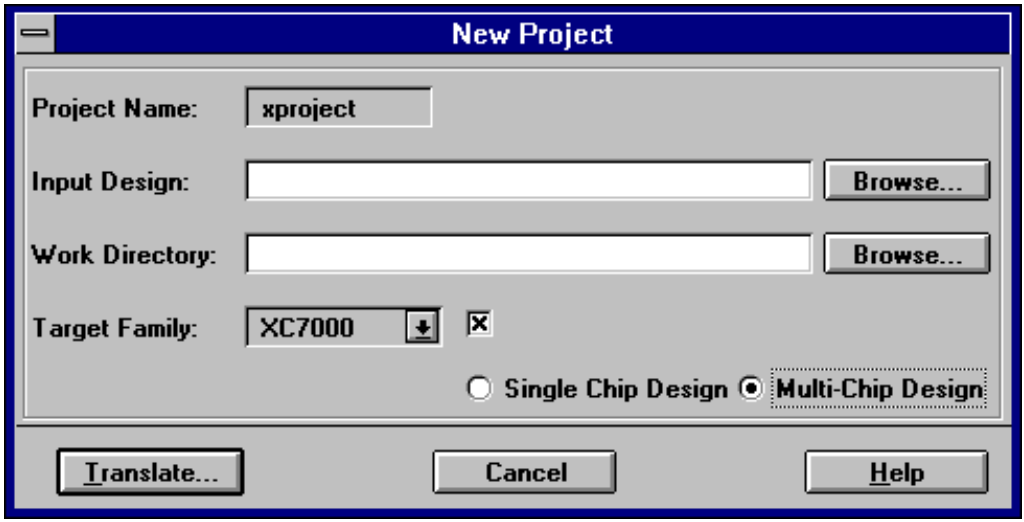


Figure 3-28 The New Project Window

2. Select the Multi-Chip Partitioner from the Design Manager Tools menu or by double clicking the Multi-Chip Partitioner button in the Design Manager Toolbox (see Figure 3-29).

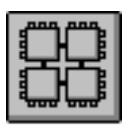


Figure 3-29 Multi-Chip Partitioner Button

The Multi-Chip Partitioner Window appears as shown in Figure 3-30.

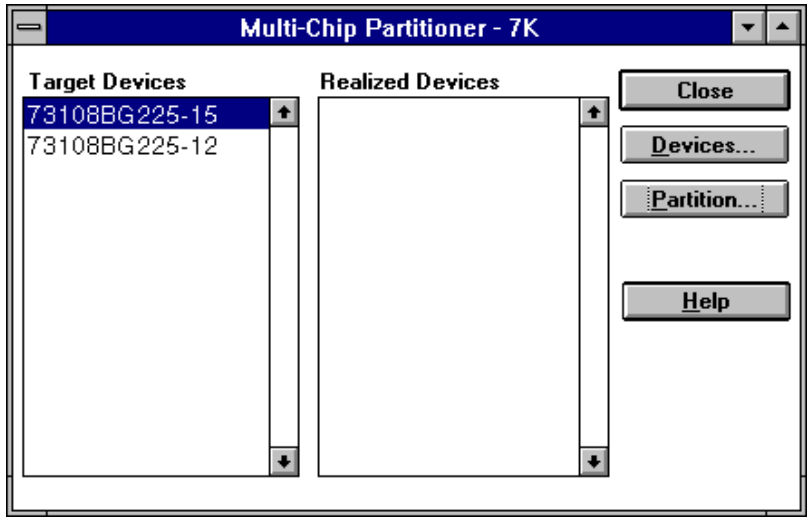


Figure 3-30 Multi-Chip Partitioner Window

3. From the Multi-Chip Partitioner Window, you can specify a range of possible target devices from which the Partitioner can choose the best ones to fit your design. After partitioning, you will see the target devices that were actually used by the fitter, displayed in the Realized Devices column.

4. After you have successfully partitioned your design into multiple devices, the Design Manager window shows each multi-chip implementation as “Try1”, “Try2”, and so on; single-chip designs show the specific device type instead.

   The Design manager window shown in Figure 3-31, shows a design with two different multi-chip implementations.

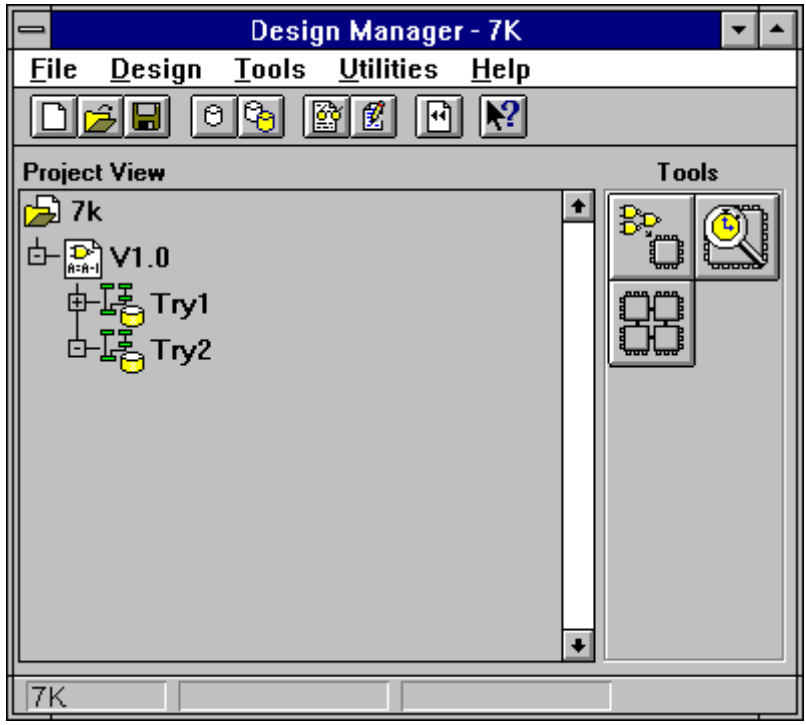


Figure 3-31 Two Multi-Chip Implementations

Note: Your design timing may be affected by multi-chip partitioning; your timing requirements, as defined by your Timespecs, cannot be guaranteed when your design is partitioned into multiple devices.

Chapter 4

Command Reference

This chapter describes the Design Manager and Flow Engine commands. It covers the following topics:

- Design Manager Menus
- Flow Engine Menus
- Design Manager/Flow Engine Command Reference
- Toolbars
- Toolbox
- Mouse Accelerator Buttons
- Text Editor Commands
- Standard Dialog Boxes
- Keyboard Shortcuts

Design Manager Menus

The following is a list of the Design Manager menus and menu commands.

File Menu

New Project

Open Project

Save Project

Close Project

Delete Project

Exit

Design Menu

Translate

Implement

Export

New Device

New Revision

Copy Revision

Browse Revision

Rename

Delete

Tools Menu

Flow Engine

Floorplanner

Timing Analyzer

PROM File Formatter

Hardware Debugger

Design Editor

PROM Programmer

Partitioner

Utilities Menu

Report Browser

Command History

Project Notes

Template Manager

Makebits Utility

Check Routed Design

Help Menu

Contents

Search for Help On

Tutorial

About Design Manager

Flow Engine Menus

The following is a list of the Flow Engine menus and menu commands.

Flow Menu

Run

Step

Backup

Stop

Close

Setup Menu

Options

Font

Advanced

Utilities Menu

Report Browser

Command History

Command Preview

Project Notes

Template Manager

Help Menu

Contents

Search for Help On

Tutorial

About Flow Engine

Design Manager/Flow Engine Command Reference

Since the Design Manager and Flow Engine share many of the same commands and dialog boxes, this section describes all the menu commands for both tools combined together and presented in alphabetical order.

About Design Manager Command (Help Menu)

Use this command to display the version number of your copy of the Design Manager and the copyright notice. A dialog box displays this information as shown in Figure 4-1.

Figure 4-1 About Design Manager Dialog Box

About Flow Engine Command (Help Menu)

Use this command to display the version number of your copy of the Flow Engine and the copyright notice. A dialog box displays this information as shown in Figure 4-2.

Figure 4-2 About Flow Engine Dialog Box

Advanced Command (Setup Menu)

Use this command to open the Flow Configuration dialog box (see Figure 4-3) and configure the Flow Engine.

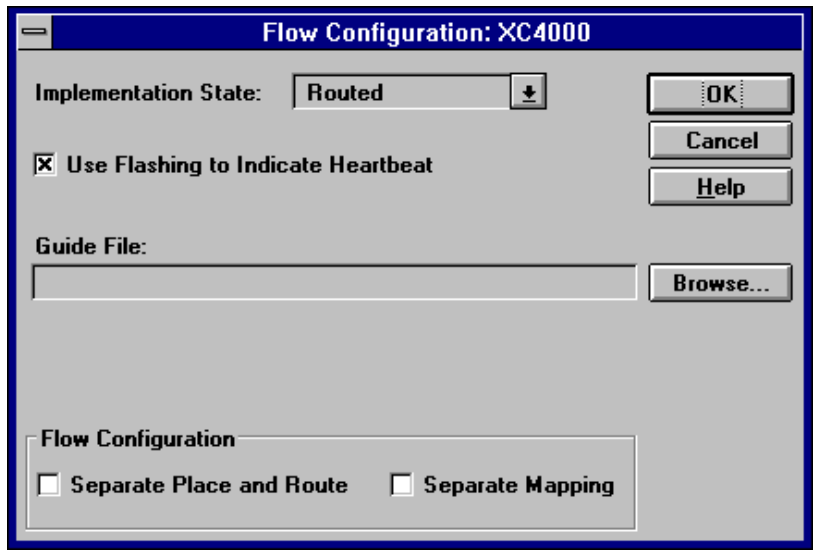


Figure 4-3 Flow Configuration Dialog Box

Flow Configuration Dialog Box Options

Implementation State

Most users will not need to modify this setting. Use this option to update the Flow Engine as to which implementation state was last completed. In normal Flow Engine use, do not use this setting to change the implementation state. This setting is typically used if some processing on the design was performed outside of the Design Manager or Flow Engine framework. For example, if the design was routed using the Design Editor, the Implementation State should be set to Routed to inform the Design Manager and Flow Engine that this implementation state is completed.

Use Flashing to Indicate Heartbeat

Enables flashing process icons to indicate processing activity in the Flow Engine. This option is useful for providing feedback that the Flow Engine is running. This option is off by default. Enabling this option may slow down the implementation process.

Guide File

Specify a guide file to use for implementation. Type the guide file name or press the browse button to open a file selection dialog box.

The function of a guide file differs for FPGA and EPLD designs. For FPGA designs, a guide file guides the place and route software in placing logic and routing signals. For EPLD designs, a guide file maintains the pin assignments from a previous iteration of the design.

A guide file is not the same as a guide design that you specify in the Implementation dialog box. In this context, a guide file is created by software other than the Design Manager such as by the Floorplanner or a previous version of the XACT software.

Separate Place and Route

Enable this option to have the Flow Engine perform logic placement and signal routing in two separate steps. Typically this option is disabled. It is useful for focusing special efforts on either placing or routing the design. This allows you to step only through the place step so that the design is placed, but not routed. Or, if the placement is satisfactory, you can make various attempts at routing without having to place the design each time.

This option does not apply to the XC7000.

Separate Mapping (XC4000 and XC5200 only)

Enable this option to have the Flow Engine separate the map step from place and route. This option is useful if you intend to floorplan the design. Before the Floorplanner can be used on a design, the design must be mapped. Enable this option to have the Flow Engine generate the required mapped design file for the Floorplanner.

Backup Command (Flow Menu)

Use this command to go back one step in the processing flow. You can use this command to backup and then re-run a step using different options. The data is not deleted until you overwrite it by re-running the step.

Browse Revision Command (Design Menu)

Use this command to work with the files in a design revision. It opens the Revision Browser dialog box in which you can edit, copy, move, rename, and delete data files for a design revision. The Revision Browser serves as a file manager.

Warning: Use caution when you change files with the Revision Browser since it is possible to interfere with the Design Manager's normal processing by changing files this way.

Select Browse Revision from the Design Menu to open the Revision Browser dialog box as shown in Figure 4-4.

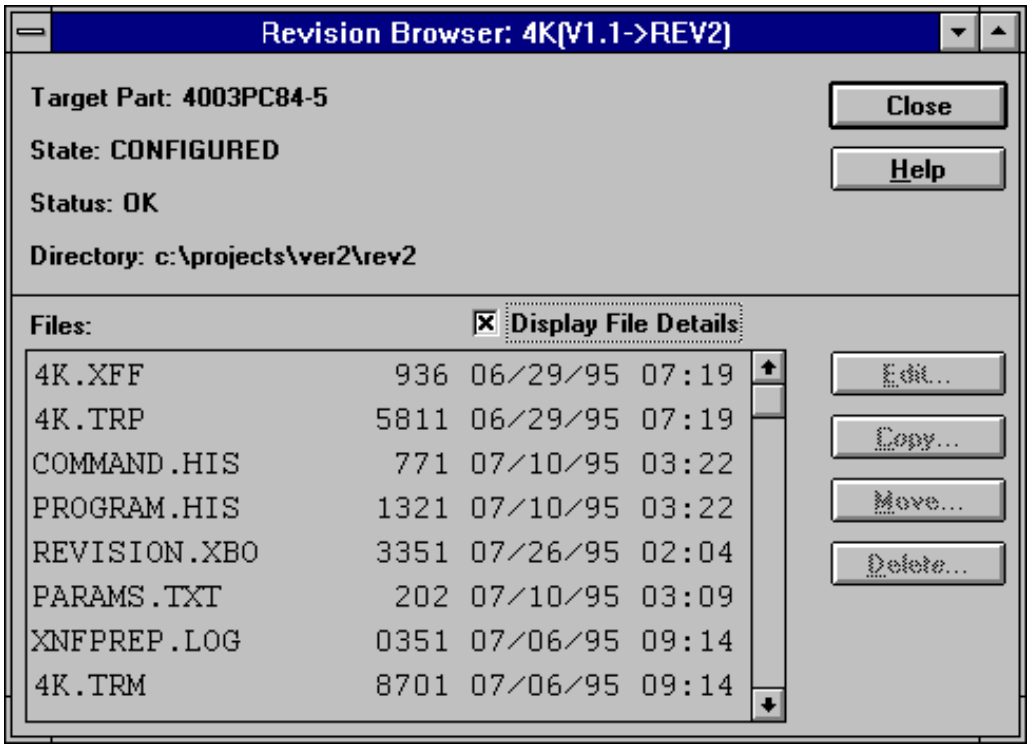


Figure 4-4 Revision Browser Dialog Box

Revision Browser Dialog Box Options

Target Part

The part type that you are targeting with this revision.

State

The current position completed in the process flow. The possible states are translated, optimized, mapped, placed, routed, fitted (XC7000 only), timed, configured, or programmed (XC7000 only).

Status

The status of the design processing up to the current state. The possible states in this field are:

OK

The software generated no errors or warnings

Warning

The software encountered a situation that may require your attention.

Error

The software encountered a processing error.

Directory

The full path to the current implementation revision.

Files

A list of files that the were generated while running the flow.

Display File Details

Enable this check box to display more file details such as file size, date, and time of creation.

Edit

Opens the selected file in a text editor when you click the Edit button. You can also open a file by double clicking on it's name in the Revision Browser dialog box.

Copy

Opens a file selection dialog box for you to specify where to save a copy of the selected file.

Move

Opens a file selection dialog box for you to specify where to move the selected file.

Delete

Deletes the selected file after confirmation.

Note: The Edit, Copy, Move, and Delete buttons are grayed out if no file is selected.

Check Routed Design Command (Utilities Menu)

Use this command to verify a design after it has been routed. It is only available after the design revision has been routed. This command runs the Design Rules Checker. It checks the routed design for proper routing of signals and correct configuration of logic blocks. This command is useful for determining unrouted signals in a design. The Design Rules Checker displays a message (see Figure 4-5) upon completion and if you click the Review Log button, the log report is displayed in a Text Editor window (see Figure 4-6).

Figure 4-5 Check Routed Design Message

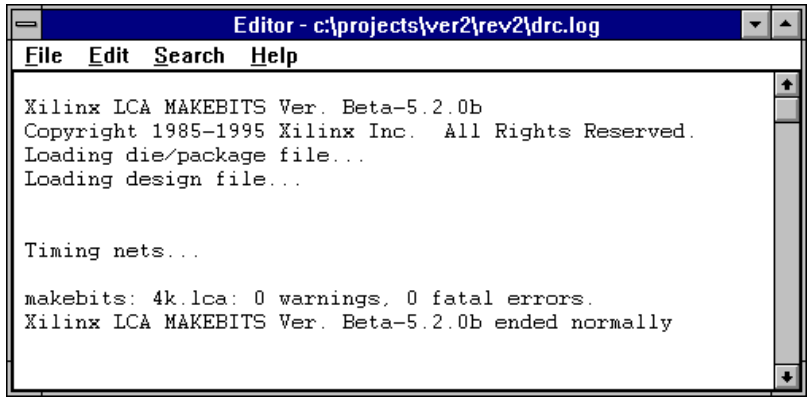


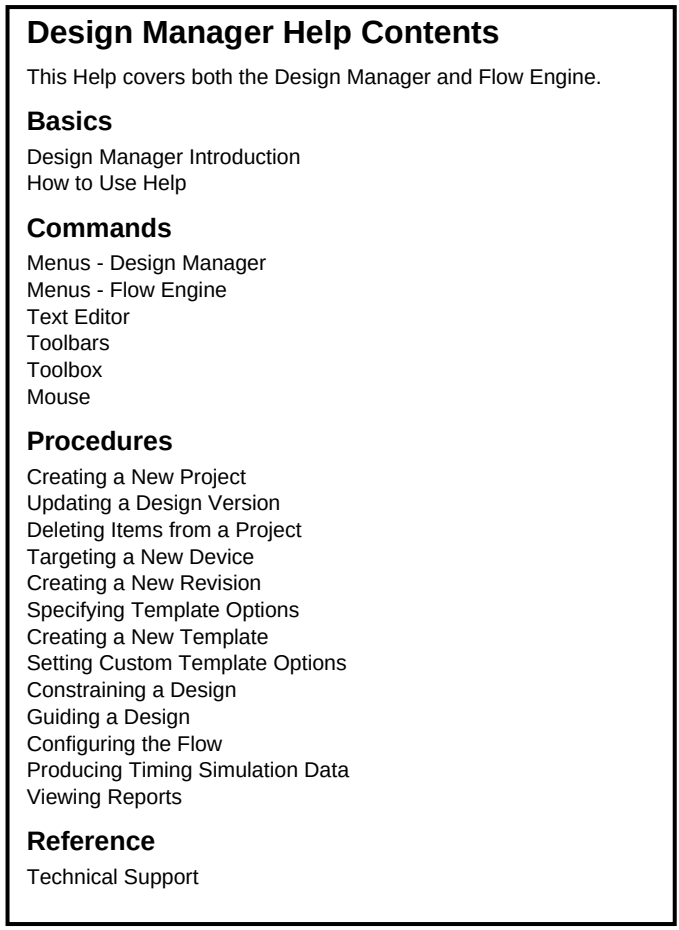
Figure 4-6 Check Routed Design Log

Contents Command (Help Menu)

Use this command to display the opening screen of Design Manager Help as shown in Figure 4-7. From the opening screen, you can jump to step-by-step instructions for using the Design Manager and Flow Engine and various types of reference information.

Once you open help, you can click the contents button in the Help window whenever you want to return to the opening screen of Help.

For more information about online help, see “Obtaining Online Help” on page 2-3.



Design Manager Help Contents

This Help covers both the Design Manager and Flow Engine.

Basics

Design Manager Introduction
How to Use Help

Commands

Menus - Design Manager
Menus - Flow Engine
Text Editor
Toolbars
Toolbox
Mouse

Procedures

Creating a New Project
Updating a Design Version
Deleting Items from a Project
Targeting a New Device
Creating a New Revision
Specifying Template Options
Creating a New Template
Setting Custom Template Options
Constraining a Design
Guiding a Design
Configuring the Flow
Producing Timing Simulation Data
Viewing Reports

Reference

Technical Support

Figure 4-7 Design Manager Help Contents

Close Command (Flow Menu)

Use this command to close the Flow Engine window. Use this command when you are finished compiling and no longer need the Flow Engine.

Close Project Command (File Menu)

Use this command to close the current project along with all of its associated Design Manager files.

Command History Command (Utilities Menu)

Use this command to display the commands that have already been run in the flow for the current implementation revision. This command is useful for reviewing the programs and options that were used while executing the flow. It opens the Command History dialog box (see Figure 4-9). There are two view modes which you select in the View Mode pulldown menu. The modes are:

Normal — Displays high level flow information about the executed commands.

Command Line — Displays more detail about the executed commands and command options.

Use the toolbar button shown in Figure 4-8 for quick access to this command.

Figure 4-8 Command History Button

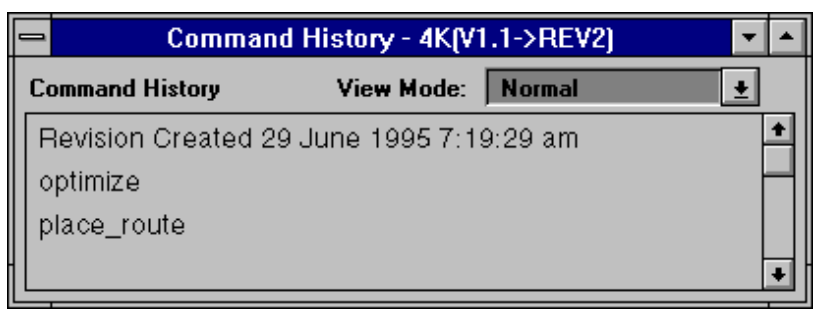


Figure 4-9 Command History Dialog Box

Command Preview Command (Utilities Menu)

Use this command to display the commands that remain to be run in the flow for the current implementation revision. This command is useful for determining which programs will be executed in the flow and whether the appropriate options have been set. It opens a Command Preview dialog box (see Figure 4-11).

Use the toolbar button shown in Figure 4-10 for quick access to this command.

Figure 4-10 Preview Commands Button

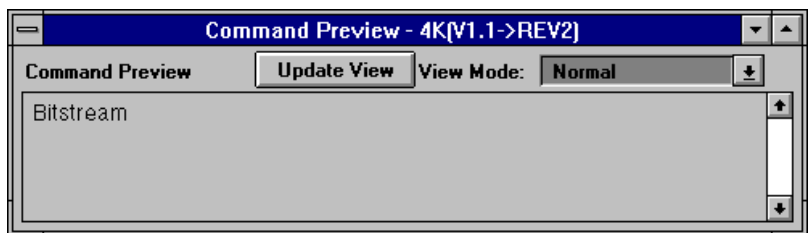


Figure 4-11 Command Preview Dialog Box

Command Preview Dialog Box Options

Command Preview Box

Displays the commands that the Flow Engine will execute.

Update View

Updates the command preview information to reflect any changes made in Flow Engine option settings since opening the Command Preview window.

View Mode

Normal

Displays high level flow information about the commands that will be executed.

Command Line

Displays more detailed information about the commands and command options that will be executed.

Copy Revision Command (Design Menu)

Use this command to make a copy of the currently selected implementation revision. This creates a new revision which contains the same data as the selected revision. The Design Manager displays a new revision icon in the Project View.

You can also access this command by pressing the right mouse button in the Project View and selecting Copy Revision in the popup menu.

Use the toolbar button shown in Figure 4-12 for quick access to this command.

Figure 4-12 Copy Revision Button

When you use the Copy Revision command, the Copy Revision dialog box (see Figure 4-13) opens in which you can type in a name for the revision copy.

Figure 4-13 Copy Revision Dialog Box

Delete Command (Design Menu)

Use this command to delete the currently selected design version, device, or implementation revision.

You can also delete items by selecting a design version, device or implementation revision icon and pressing the delete key or by pressing the right mouse button and selecting Delete in the popup menu.

Warning: When deleting an item from the Project View, the Design Manager immediately deletes the item and all accompanying data, and removes its icon from the Project View. Data which is deleted cannot be recovered.

Delete Project Command (File Menu)

Use this command to delete a project along with all its associated files in the project directory.

This command opens the Delete Project dialog box shown in Figure 4-14. You are presented with a list of projects from which you can select a project to delete.

To delete a project, select a project and click the delete button. You are prompted to confirm that you really want to delete the project.

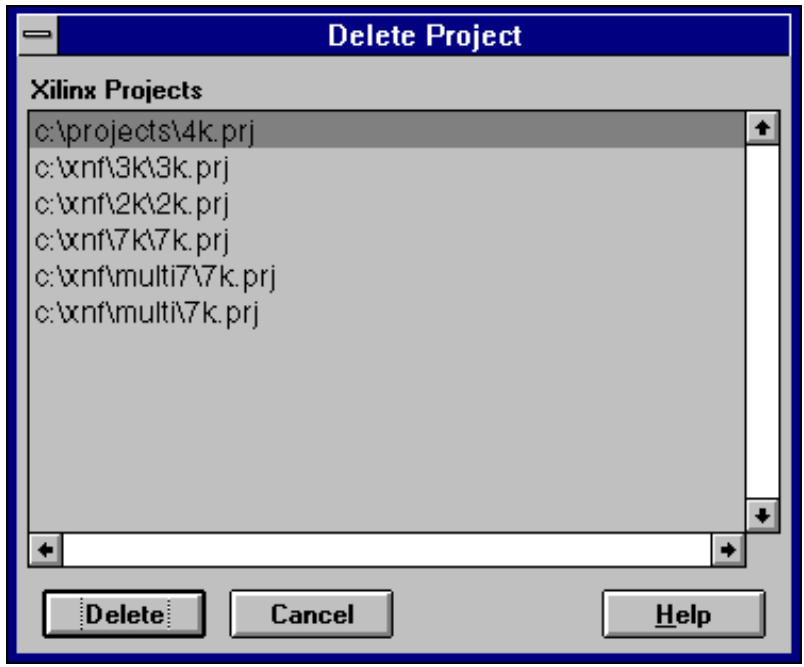


Figure 4-14 Delete Project Dialog Box

Design Editor Command (Tools Menu)

Use this command to launch the Xilinx Design Editor from the Design Manager. The Xilinx Design Editor is a graphical tool which allows you to view the die resources of a device. You can use the Xilinx Design Editor to edit design logic, logic placement, and signal routing. The Design Editor is not available for the XC7000. You can also use the Toolbox button shown in Figure 4-15 for quick access to this command.

Note: The Design Editor is a DOS application.

Figure 4-15 Design Editor Button

Exit Command (File Menu)

Use this command to close the current project and exit the Design Manager. You are prompted to confirm that you really want to quit.

Export Command (Design Menu)

Use this command to export your design data. It opens the Design Export dialog box shown in Figure 4-16. This command is useful for transferring design data created in the Design Manager to other environments.

Figure 4-16 Design Export Dialog Box

Design Export Dialog Box Options

Physical Design Data

Export physical design data (*design*.lca file for FPGA and *design*.gyd file for EPLD).

Timing Simulation Data

Export timing simulation data (*back_annotated*.xnf file).

Configuration Data

Export configuration data (*design*.bit or *design*.ll file for FPGA and *design*.prg file for EPLD).

Export to

Type the directory path and name in which to save the exported data.

Browse

Opens a file selection dialog box (see "File Selection Dialog Box" on page 4-63) in which you can specify a directory for the exported data.

Floorplanner Command (Tools Menu)

Use this command to launch the Floorplanner and work with the selected design revision.

The selected design revision must be mapped before starting the Floorplanner. If the design revision is not mapped, the Design Manager confirms that you want to map it, maps it, and starts the Floorplanner.

The Floorplanner is a graphical placement tool that gives you manual control over placing a design into a target FPGA die. It provides a graphical representation of the mapped design hierarchy and the resources available on the die. Use this tool to manually place critical logic on the die.

For more information on the Floorplanner, click on Help from within the Floorplanner.

You can also use the Toolbox button shown in Figure 4-17 for quick access to this command.

Figure 4-17 Floorplanner Button

Flow Engine Command (Tools Menu)

Use this command to launch the interactive Flow Engine. You can use the Flow Engine to compile a design. You can set compile and flow options from within the Flow Engine. You can also use the Toolbox button shown in Figure 4-18 for quick access to this command.

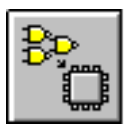


Figure 4-18 Flow Engine Button

Font Command (Setup Menu)

Use this command to specify the font type and font size for the text displayed in the Flow Engine message window. This command opens the Font dialog box shown in Figure 4-19 in which you can make these settings.

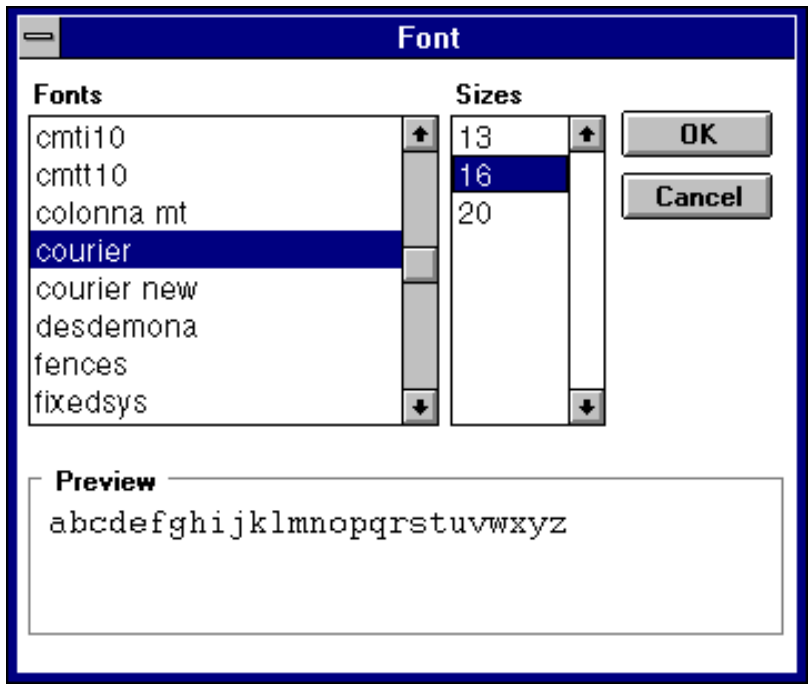


Figure 4-19 Font Dialog Box

Dialog Box Options

Font

Specifies the font type such as Courier or Helvetica.

Sizes

Specifies the font size in points.

Preview

Shows an example of text displayed with the font type and font size that you specify.

Hardware Debugger Command (Tools Menu)

Use this command to launch the Hardware Debugger.

Use the Hardware Debugger to download a design to a device, verify the downloaded configuration, and display the internal states of the programmed device.

You can also use the Toolbox button shown in Figure 4-20 for quick access to this command.

Figure 4-20 Hardware Debugger Button

For additional online help for the this tool, get Help from within the Hardware Debugger.

Implement Command (Design Menu)

Use this command to start the implementation process. This command opens the Design Implementation Options dialog box (see Figure 4-21). When you close the Design Implementation Options dialog box, a read-only version of the Flow Engine opens and begins to process the design (see Figure 4-22).

The Design Implementation Options dialog box contains many options which differ for each device family type. This dialog box and all its options are described in the chapter, “Implementation Options” on page 5-1.

You can also open the Design Implementation Options dialog box as follows:

- From the Flow Engine Setup menu, choose Options.
- In the Project View, press the right mouse button, and select Implement from the popup menu
- Double click on a revision in the Project View.

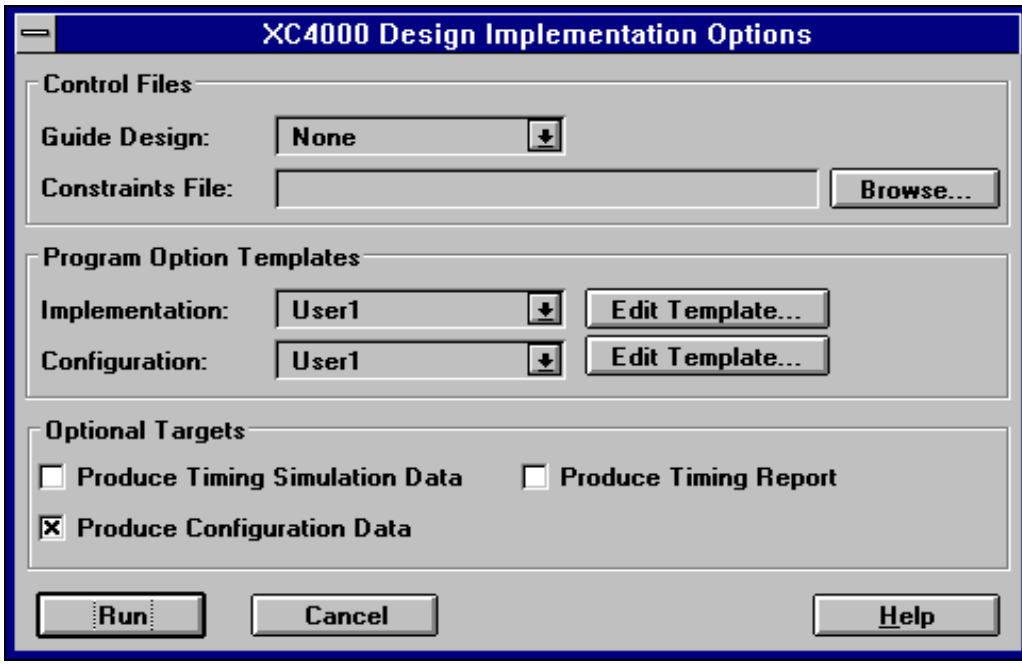


Figure 4-21 Design Implementation Options Dialog Box

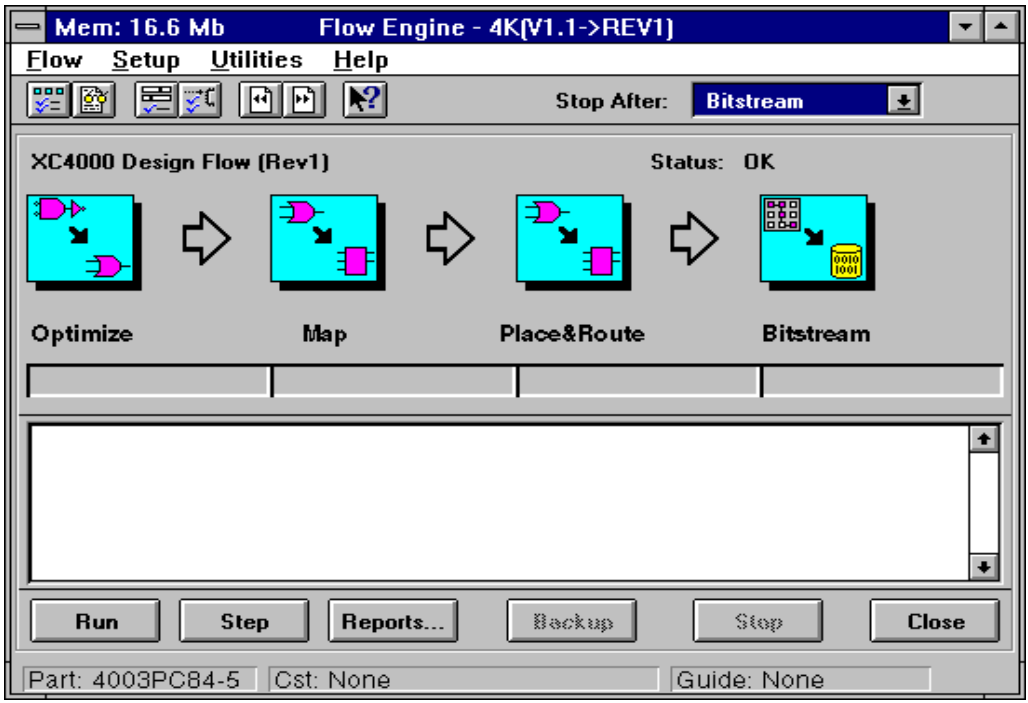


Figure 4-22 Flow Engine Window (Read-Only)

Makebits Utility Command (Utilities Menu)

Use this command to produce the configuration bitstream for a routed design. The configuration bitstream describes the internal functions and interconnections of an LCA device. The bitstream is downloaded to the FPGA to program it with the design. Although the Flow Engine can generate the bitstream, the Makebits Utility provides additional bitstream options which are not available in the Flow Engine.

Selecting Makebits Utility from the Utilities menu in either the Design Manager or Flow Engine opens the Makebits Utility dialog box as shown in Figure 4-23.

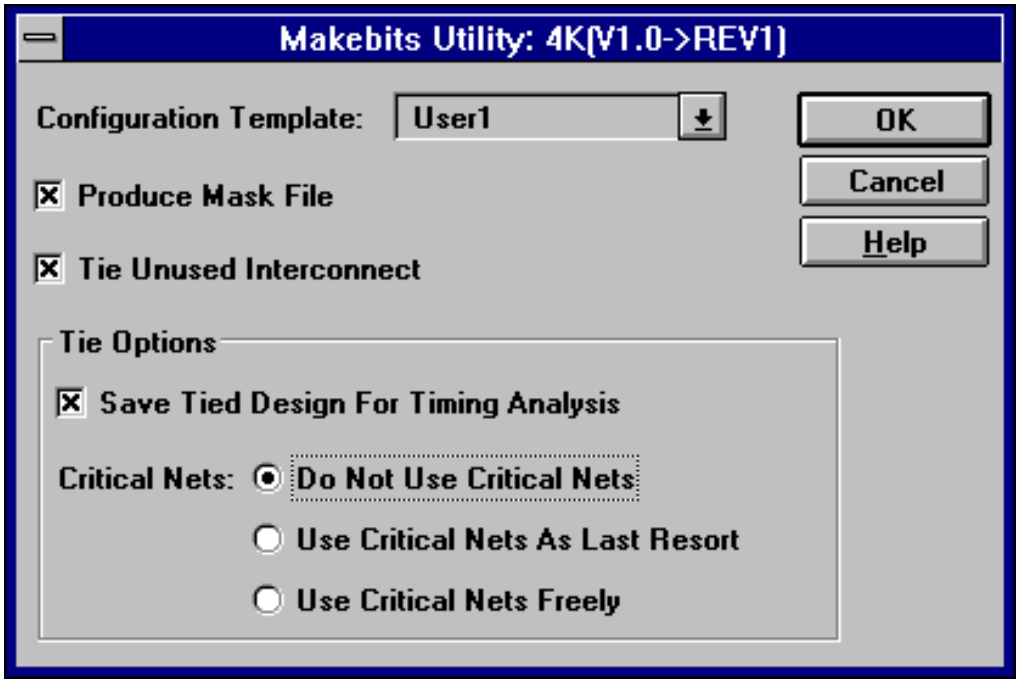


Figure 4-23 Makebits Utility Dialog Box

Makebits Utility Dialog Box Options

Configuration Template

The Configuration Template is used to select a template of option settings to use when creating the configuration bitstream for a design. The templates set various options for configuration, startup, and readback. To view the option settings for each template or to create a new template, use the Template Manager command in the Utilities menu.

Produce Mask File

Use this option to create a mask file (.MSK). The mask file is used during the verification of a bitstream readback from a configured FPGA. When the bitstream is readback from the FPGA, the state of certain bits will vary depending on the state of the design in the FPGA. The mask file indicates which bits in the readback bitstream can be safely ignored when compared against the configuration bitstream.

Tie Unused Interconnect

Use this option to create a configuration bitstream with all unused interconnects tied High or Low or to a defined signal. This process helps minimize internal noise and power consumption that can result from undefined levels on CMOS gate inputs. However, using this option can affect the timing of a routed design. Also, this process may fail to complete on some designs if the software is not able to tie all unused interconnects.

Save Tied Design for Timing Analysis

Use this option to save the results of a tied design for timing analysis. The tie process can affect the timing of a design. A simulation should be performed on the tied design to verify its timing. This option is only valid if the Tie Unused Interconnect option is selected.

Critical Nets

In your design entry tool, you can flag timing critical nets in your design as critical. The following options determine whether the Makebits Utility uses critical nets in the tie process. Refer to the appropriate Xilinx third party interface user guide for information on how to assign critical nets in a design.

Do Not Use Critical Nets

Use this option if nets marked as critical are not to be used during the tie process. This prevents the possibility of adding additional delays to critical nets during the tie process.

Use Critical Nets As Last Resort

Use this option if nets marked as critical can be used as a last resort to complete the tie process. Nets which are used in the tie process may incur additional delay.

Use Critical Nets Freely

Use this option if nets marked as critical can be used freely to complete the tie process. Setting this option allows the software to use all signals freely to complete the tie process. Nets which are used in the tie process may incur additional delay.

New Device Command (Design Menu)

Use this command to select a new device for implementation. The Design Manager opens the Part Selector dialog box. The Part Selector dialog boxes are shown in Figure 4-24 and Figure 4-25.

Only the options that are compatible with the original input design file are displayed in this dialog box. For example, if your design specified an XC3000, this dialog box gives you the option of selecting devices from the XC3000 family.

When working with EPLD XC7000 devices, the Part Selector has some additional functionality. You can specify All in the Device, Package, and Speed boxes and the allowed selections are displayed in the Filtered List box. You can select a specific device from the list. Or you can specify an All setting in one or more of the boxes and the Design Manager automatically selects the best device during implementation.

Part Selector Dialog Box Options

Family

Specifies the family type such as XC2000, XC3000, XC4000, XC5200, and XC7000.

Device

Specifies the device type. Only the devices that are in the family that you specify in the Family field are displayed in the Devices field.

Package

Specifies the package type such as PC84, PQ100, and BGA225.

Speed

Specifies the speed of the device.

Filtered List (EPLD only)

Displays a list of possible devices to choose from.

Final Selection (EPLD only)

The device that will be used for implementing the design.

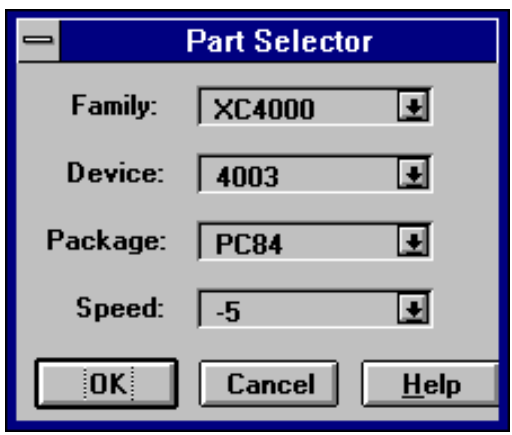


Figure 4-24 Part Selector Dialog Box (FPGA Devices)

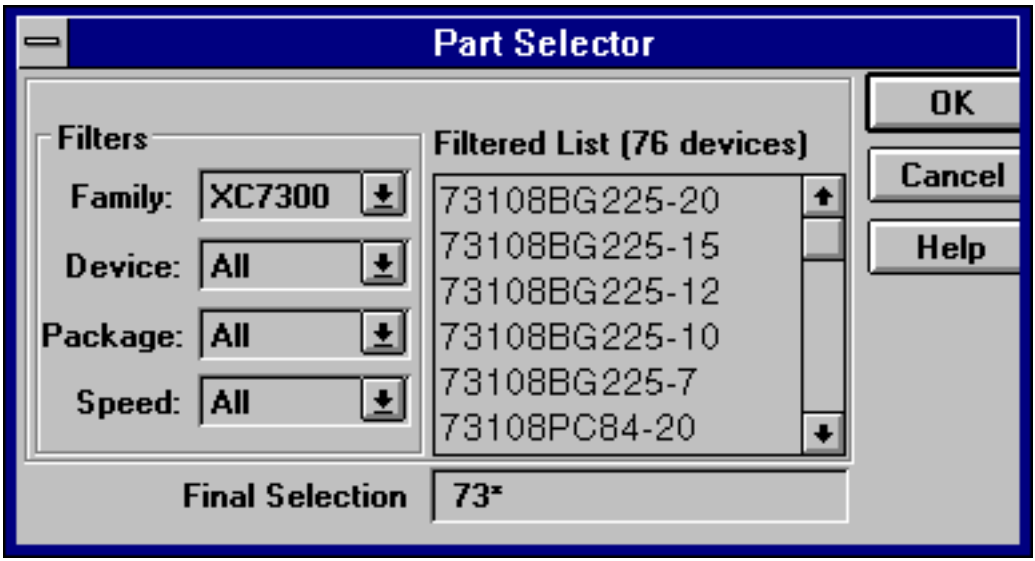


Figure 4-25 Part Selector Dialog Box (EPLD Devices)

For EPLD devices (XC7000), the automatic device selector uses the Filters list to automatically select a device in which to fit the design.

New Project Command (File Menu)

Use this command to create a new project and translate a design into the Design Manager. You can translate a file created by a design entry tool. This command opens the New Project dialog box (see Figure 4-27 and Figure 4-28) in which you can specify the conditions for creating your new project. When you select Translate in the New Project dialog box, the Design Manager translates the netlist.

To open an existing project, use the Open Project command.

Use the toolbar button shown in Figure 4-26 for quick access to the New Project command.

Figure 4-26 New Project Button

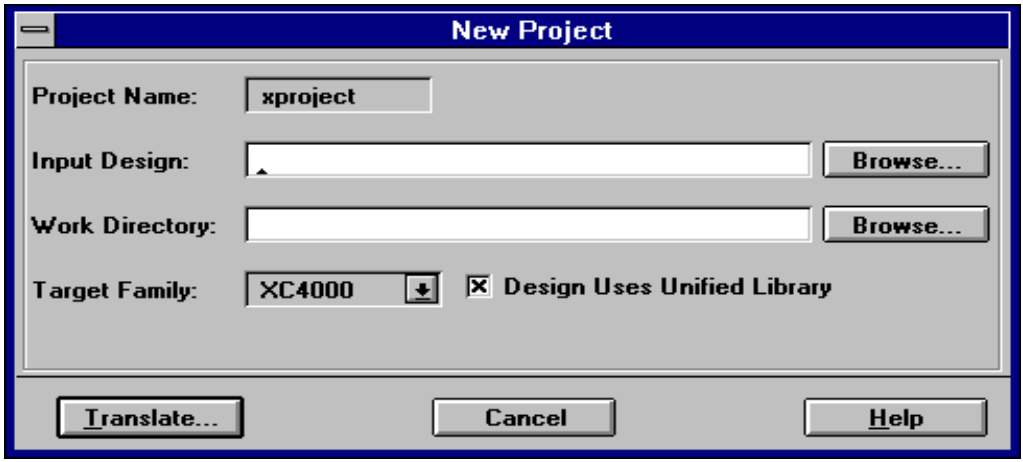


Figure 4-27 New Project Dialog Box (FPGA Devices)

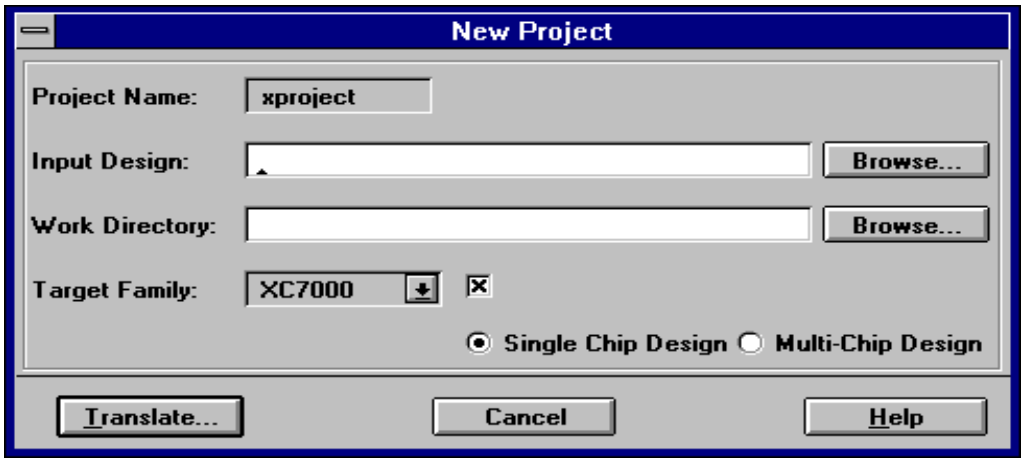


Figure 4-28 New Project Dialog Box (EPLD Devices)

New Project Dialog Box Options

Project Name

The Design Manager creates a project directory with this name and locates it in the work directory that you specify in the Work Directory box. The project name can consist of alphanumeric characters and may not exceed eight characters in length. The Design Manager uses the project directory to store all the data files for the project. The project name must specify a directory which does not already exist. The Design Manager creates the directory during project creation. The typical work directory is *design_directory*\xproject.

Input Design

Specifies the name of the design file you want to open. You may either type the name or click the browse button (to the right of this field) to open a file selection dialog box (see "File Selection Dialog Box" on page 4-63) in which you can select a design file to open. The Design Manager can accept the following input design file types:

.1	Viewlogic schematic and wir
.sch	OrCAD schematic
.xnf	Xilinx hierarchical netlist
.pld	Xilinx (XC7000 only)

Target Family

Specifies the target device family for the new project.

When you select the XC7000 family, the Target Family portion of the dialog box (see Figure 4-28) displays the Single-Chip Design or Multi-Chip Design radio buttons. These buttons are not applicable for the other device families and are not displayed. Select the appropriate option for your design. In the XC7000 single chip design mode, you can leave the device part number in the design, or you can use the device selector to choose a device for implementation.

Design Uses Unified Library

Check this box if the design uses the Xilinx libraries from version 5.0 or higher of the Xilinx XACT software.

Single Chip Design (XC7000 Only)

Enable this option if you do not wish to partition the design into multiple chips. If selected, the Partitioner tool is disabled and the design will be fitted into a single device.

Multi-Chip Design (XC7000 Only)

Enable this option if you plan to use the Partitioner tool and fit the design into more than one device. This allows you to partition the design into different combinations of multiple devices.

Work Directory

Specifies the name of the directory in which to put the new project directory. You may either type the name or click the browse button (to the right of this field) to open a directory selection dialog box (see "Directory Selection Dialog Box" on page 4-65) and specify a work directory.

Translate

Click this button to begin the translation. The design manager displays the Translate Options dialog box (see Figure 4-29). When you select the OK button in the Translate Options dialog box, the Design Manager reads your input design file, translates it into a Xilinx netlist, and creates the new project. For more information on the Translate Options dialog box, see "Translate Options Dialog Box Options" on page 4-49.

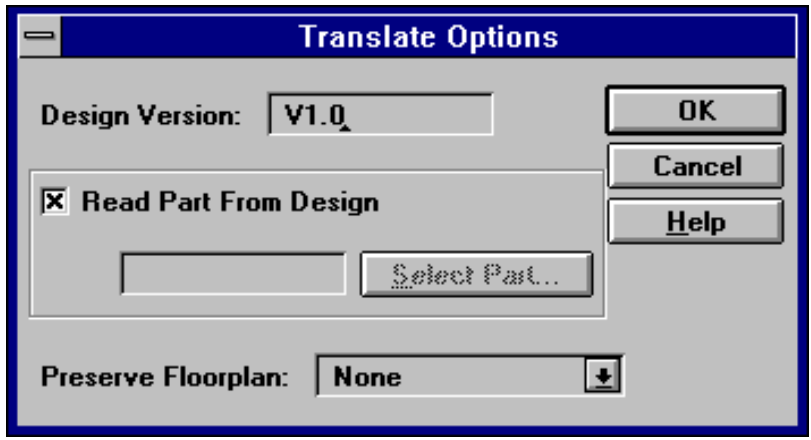


Figure 4-29 Translate Options Dialog Box

New Revision Command (Design Menu)

Use this command to create a new implementation revision. A new icon is displayed in the Project View. A new revision allows you to attempt a new implementation of the design using different compile options.

You can also access this command by pressing the right mouse button in the Project View and selecting New Revision in the popup menu.

Use the toolbar button shown in Figure 4-30 for quick access to this command.

Figure 4-30 New Revision Button

When you use the New Revision command, the Revision Name dialog box (see Figure 4-31) opens in which you can type a name for the new revision.

Figure 4-31 New Revision Dialog Box

Open Project Command (File Menu)

Use this command to open an existing project. The project consists of several files but is represented in the Xilinx Projects dialog box as a single file with the .prj extension. The Open Project command opens the Open Project dialog box (see Figure 4-33) in which you can select a project.

To create a new project, use the New Project command.

Use the toolbar button shown in Figure 4-32 for quick access to this command.

Figure 4-32 Open Project Button

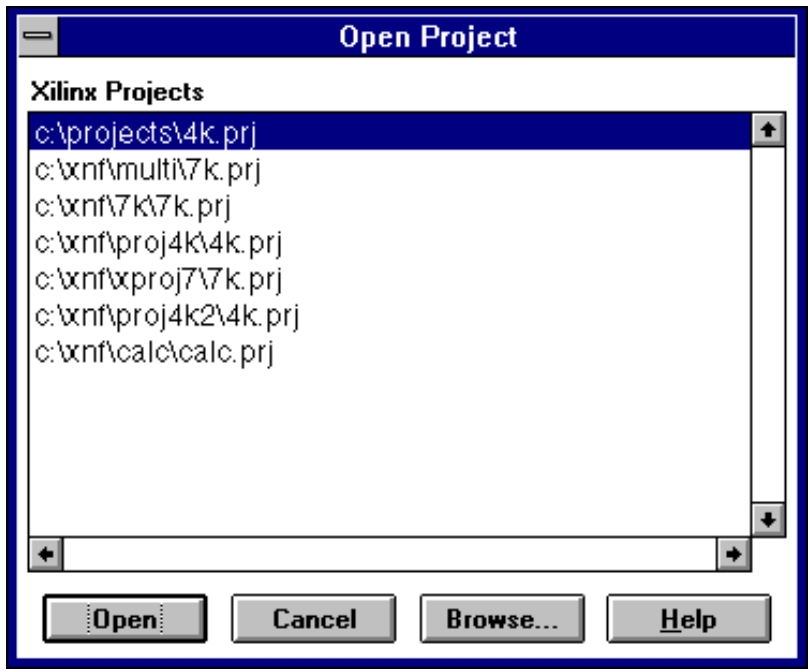


Figure 4-33 Open Project Dialog Box

Options Command (Setup Menu)

Use this command to specify the implementation settings and options for the Flow Engine to use for a particular implementation. This command opens the Design Implementation Options dialog box which is described on page 5-1.

Partitioner Command (Tools Menu)

Use this command to launch the Partitioner. The Partitioner is only available for XC7000 EPLD devices. It is a tool for partitioning a design into multiple chips.

You can also use the Toolbox button shown in Figure 4-34 for quick access to this command.

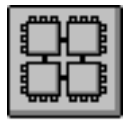


Figure 4-34 Partitioner Button

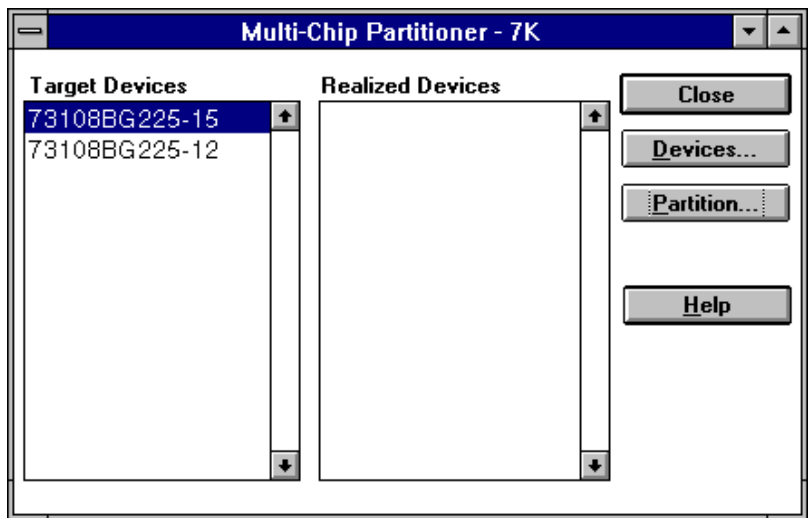


Figure 4-35 Multi-Chip Partition Dialog Box

Multi-Chip Partitioner Dialog Box Options

Devices

This button opens the Multiple Part selector dialog box (see Figure 4-36) in which you set the following options:

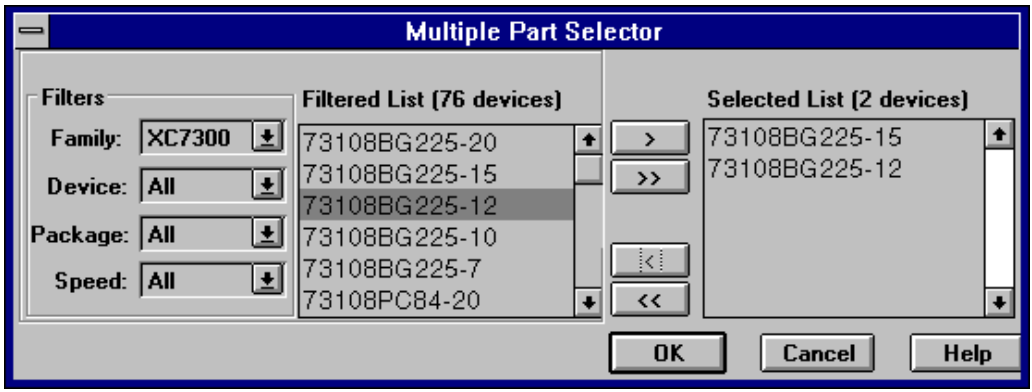


Figure 4-36 Multiple Part Selector Dialog Box

Family

Specifies the family type. You can select either the XC7200 or XC7300 family.

Device

Specifies the device type. Based on the selected family, the Device menu allows you to select from a list of available devices.

Package

Specifies the package type. Based on the selected device, the Package menu allows you to select from a list of available packages.

Speed

Specifies the speed of the device. Based on the selected device and package, the Speed menu allows you to select from a list of available speeds.

Filtered List

Lists the device types that match the criteria specified in the Family, Device, Package, and Speed boxes.

Selected List

Lists the device types that you want the design partitioned into. The partitioned design only uses devices in the Selected List.

> Button

Move selected item to Selected List.

>> Button

Move all items to Selected List

< Button

Remove the selected item from the Selected List.

<< Button

Remove all items from the Selected List

Partition

This button starts the partitioning process. The Partitioner partitions the design into multiple devices using the devices available in the Selected List. The Partition dialog box (see Figure 4-37) opens and displays processing messages.

Figure 4-37 Partition Dialog Box

Project Notes Command (Utilities Menu)

Use this command to open a Text Editor window in which to make notes for the current project.

Use the toolbar button shown in Figure 4-38 for quick access to this command.

Figure 4-38 Edit Project Notes Button

PROM File Formatter Command (Tools Menu)

Use this command to launch the PROM File Formatter.

Use the PROM File Formatter to format BIT files into a PROM file compatible with Xilinx and third party PROM programmers. You can also use it to concatenate multiple bitstreams into a single PROM file for daisy chain applications.

You can also use the Toolbox button shown in Figure 4-39 for quick access to this command.

Figure 4-39 PROM File Formatter Button

For additional online help for the this tool, get Help from within the PROM File Formatter.

PROM Programmer Command (Tools Menu)

Use this command to launch the PROM Programmer. The PROM Programmer is the software interface for controlling Xilinx device programmers.

You can also use the Toolbox button shown in Figure 4-40 for quick access to this command.

Figure 4-40 PROM Programmer Button

For additional online help for the this tool, get Help from within the PROM Programmer.

Rename Command (Design Menu)

Use this command to rename the currently selected item in the Project View. You are presented with a dialog box (see Figure 4-41) in which you can change the existing name of the selected item in the Project View.

Figure 4-41 Rename Dialog Box

Report Browser Command (Utilities Menu)

Use this command to view reports. You can also access this command by pressing the right mouse button in the Project View and selecting Reports in the popup menu. Or you can use the toolbar button shown in Figure 4-42 for quick access to this command.

Figure 4-42 Browse Reports Button

The Report Browser command opens the Report Browser window (see Figure 4-43) which contains icons that represent the reports that have been generated by the Design Manager and Flow Engine.

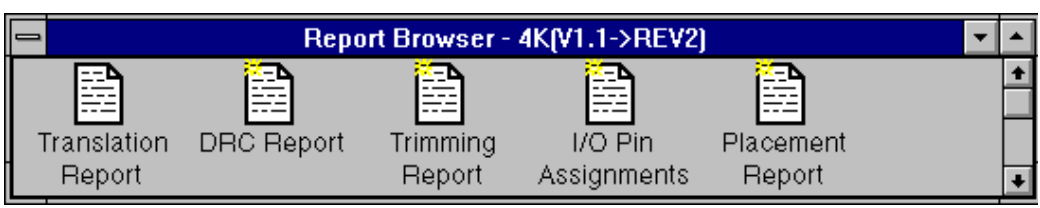


Figure 4-43 Report Browser Window

The icons change appearance to indicate whether or not you have read a report. Figure 4-44 explains the icons in the Report Browser.

Figure 4-44 Key to Report Icons

To read a report, double click the report icon and the report opens in the Text Editor as shown in Figure 4-45. The section, "Text Editor Commands" on page 4-54 describes the Text Editor menu commands.

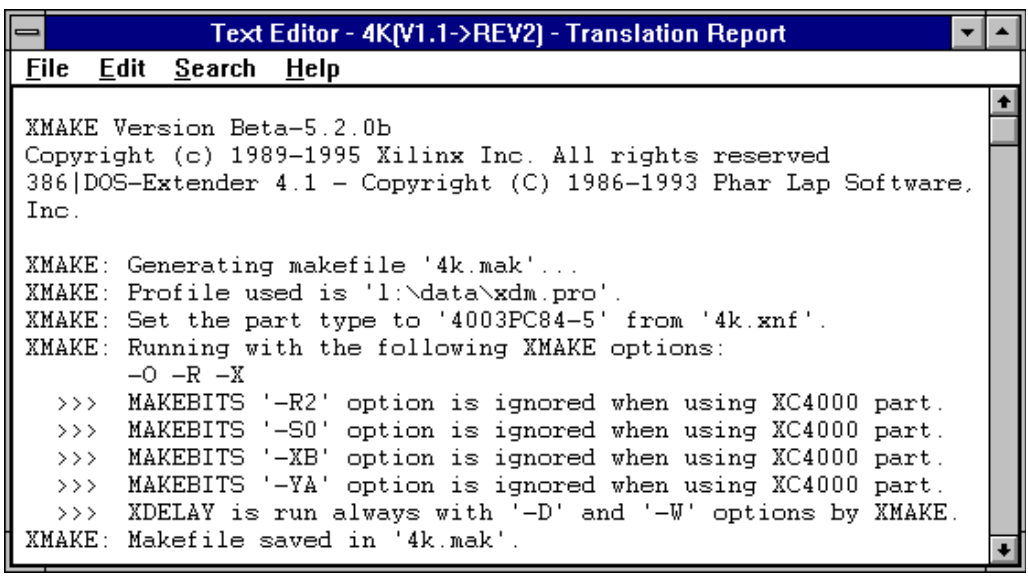


Figure 4-45 Text Editor Window

Run Command (Flow Menu)

Use this command to start the Flow Engine. The Flow Engine processes until it reaches a target or the end of the flow.

Save Project Command (File Menu)

Use this command to save the current project.

Use the toolbar button shown in Figure 4-46 for quick access to this command.

Figure 4-46 Save Project Button

Search for Help On Command (Help Menu)

Use this command to search for information in the Design Manager/Flow Engine online help.

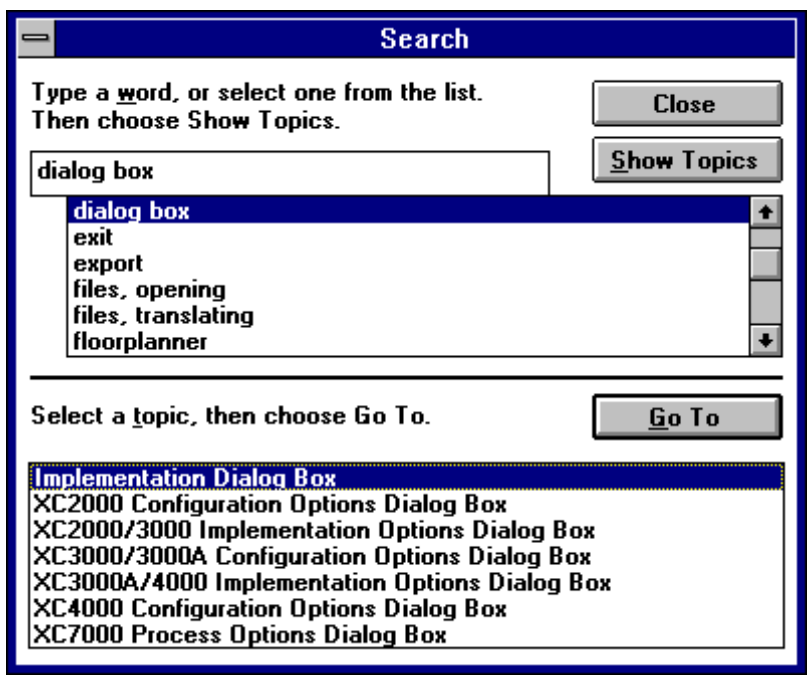


Figure 4-47 Microsoft Help Search Window

Step Command (Flow Menu)

Use this command to run the next operation in the processing flow. This allows you to single step through the compile process.

Stop Command (Flow Menu)

Use this command to interrupt the current Flow Engine execution.

Template Manager Command (Utilities Menu)

Use this command to create or modify option templates. The two types of templates available are Implementation and Configuration. These templates are used to set various compile options. This command opens the Template Manager dialog box shown in Figure 4-48. The options in this dialog box are described below. For more information on how to use the Template Manager, see "Setting Custom Template Options" on page 3-18.

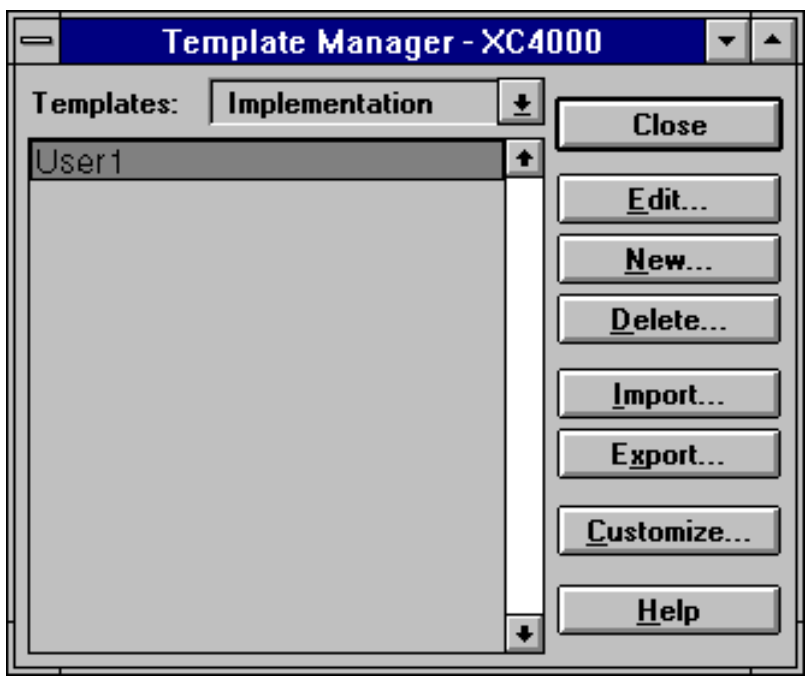


Figure 4-48 Template Manager Dialog Box

Template Manager Dialog Box Options

Templates

Specifies the type of template you wish to work with in the Template Manager — implementation or configuration. Implementation templates control how a design is optimized, placed, and routed. Configuration templates control the startup, readback, and configuration sequence of the device.

Close

Closes the Template Manager.

Edit

Opens the Implementation Template dialog box or Configuration Template dialog box to allow you to view and modify the settings for a particular template.

New

Adds a new option template. This allows you to create multiple templates with different settings.

Delete

Deletes the selected option template

Import

Imports an option template. Opens the standard file selection dialog box (see “File Selection Dialog Box” on page 4-63). You can transfer a template from one Design Manager project to another by using the Export command followed by the Import command.

Export

Exports an option template. Opens the standard file selection dialog box (see “Directory Selection Dialog Box” on page 4-65). You can transfer a template from one Design Manager project to another by using the Export command followed by the Import command.

Customize (for XC2000, XC3000, XC4000, XC5200)

Opens the Custom Template dialog box shown in Figure 4-49. Use this window to specify custom template options that are not supported by the standard options provided in the Design Manager. You can use any options that these programs support. For more information on the commands and options for these programs, refer to their user manuals.

For Implementation Templates, you can enter options for XNFPREP, XBLOX, XNFMAP (XC2000, XC3000, XC3000A), APR (XC2000, XC3000), and PPR (XC3000A, XC4000, XC5000). For Configuration Templates, you can enter options for MAKEBITS.

To use this window, type the program name in the Custom Template dialog box (see Figure 4-49) followed by the option and appropriate strings. You can enter any number of programs and options in this box. Start each line with the program name followed by the options for that program on that same line.

Warning: It is possible to enter options in the Custom Template dialog box that can conflict with normal Flow Engine options. It is beyond the scope of this manual to explain all the possible conflicts.

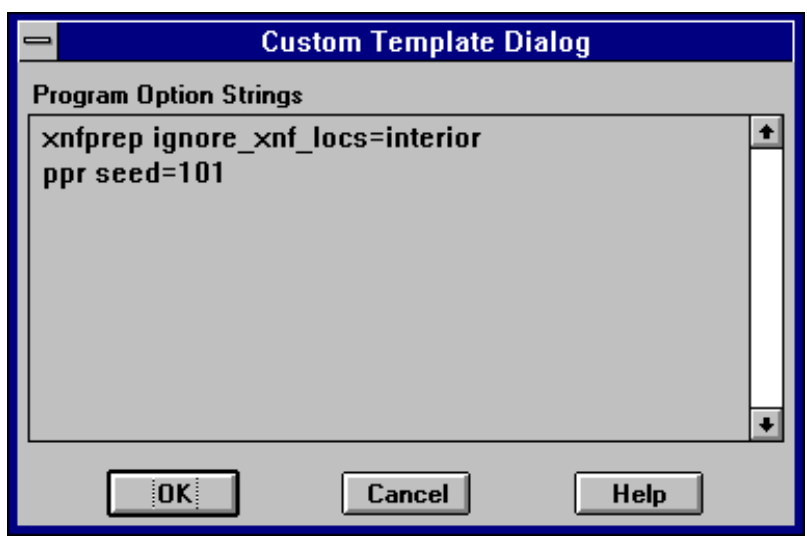


Figure 4-49 Custom Template Dialog Box

Timing Analyzer Command (Tools Menu)

Use this command to launch the Timing Analyzer. You can also use the Toolbox button shown in Figure 4-50 for quick access to this command.

Figure 4-50 Timing Analyzer Button

The Timing Analyzer performs a static timing analysis of a routed FPGA or Fitted EPLD design. A static timing analysis is a point-to-point analysis of a design network. It does not include insertion of stimulus vectors.

The Timing Analyzer verifies that the delay along a given path or paths meets your specified timing requirements. It organizes and displays data that indicate the critical paths in your circuit, the cycle time of the circuit, the delay along any specified paths, and the paths with the greatest delay. It also provides a quick analysis of the effect of different speed grades on the design.

The Timing Analyzer works with synchronous systems composed of flip-flops and combinational logic. In a synchronous design, signals must be stable long enough to allow the clocks to change so that setup and hold violations are avoided.

You use the Timing Analyzer after a design has been routed.

For additional online help for the this tool, get Help from within the Timing Analyzer.

Translate Command (Design Menu)

Use this command to re-import a design that has been changed. The Design Manager automatically translates the netlist and creates a new version icon in the Project View. For example, after making design changes in a schematic entry tool, use this command to read in the new design and create a new version in the Project View. This command opens the Translate Options dialog box shown in Figure 4-51.

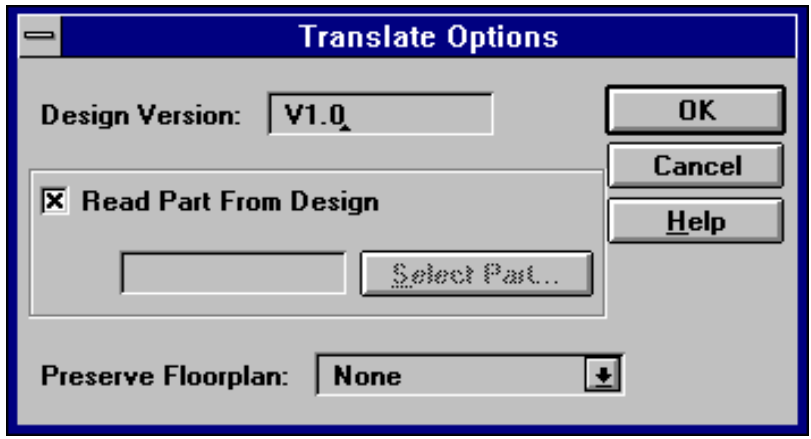


Figure 4-51 Translate Options Dialog Box

Translate Options Dialog Box Options

Design Version

This is the version of the translated design that will be displayed in the Project View.

Read Part from Design

Select this option to have the Design Manager read the part from the input design. Deselect this option to activate the Select Part button.

Select Part

If you deselect Read Part From Design, the Select Part box and button become active. Click the Select Part button to open the Part Selector dialog box in which you can specify the part type.

Preserve Floorplan

If you have floorplanned a previous revision of the design and you would like to carry forward the floorplan information from that revision, select that revision from the Preserve Floorplan popup list in the Translate Options dialog box.

Note: When creating a new project, the only available selection in the Preserve Floorplan pulldown list is None since there is no available revision with floorplan information.

Tutorial Command (Help Menu)

In the Design Manager, use this command to open the Design Manager online tutorial. In the Flow Engine use it to open the Flow Engine online tutorial.

Toolbars

Toolbars provide convenient access to often used commands. Each toolbar button is briefly described below.

If you position the mouse pointer over a toolbar button, a short description appears next to the button and a longer description appears in the status bar at the bottom of the main window.

Design Manager Toolbar Buttons

New Project — Opens a new project

Open Project — Opens an existing project

Save Project — Saves the current project

New Revision — Creates a new implementation revision

Copy Revision — Makes a copy of the selected implementation revision

Browse Reports — Opens the Report Browser tool for viewing reports

Edit Project Notes — Opens a text editor window in which to write notes for the project

View Command History — Opens a command history window

Help – Opens online help

Flow Engine Toolbar Buttons

Design implementation Options Dialog Box — Opens the Design Implementation Options dialog box

Browse Reports — Opens the Report Browser tool for viewing reports

Edit Implementation Template — Opens the Design Implementation Options dialog box

Edit Configuration Template — Opens the Configuration Template dialog box

View Command History — Opens a command history window

Preview Commands — Opens a window to preview the remaining commands that will be run.

Help — Opens online help

Toolbox

The toolbox provides buttons to access the tools in the Xilinx Design System. You can also launch these tools from the Tools menu. If you position the mouse pointer over a toolbox button, a tooltip appears next to the button and a longer description appears in the status bar at the bottom of the Design Manager window.

The toolbox contents depends on the device family that you are working with. It differs for FPGA (XC2000, XC3000, XC4000, XC5200) and EPLD (XC7000) devices as shown in Figure 4-52 and Figure 4-53.

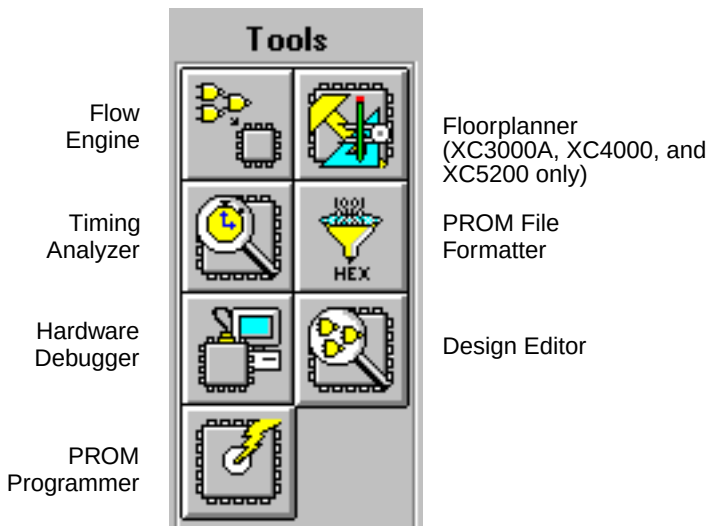


Figure 4-52 Toolbox for FPGA XC2000 XC3000, XC4000, XC5200 Devices

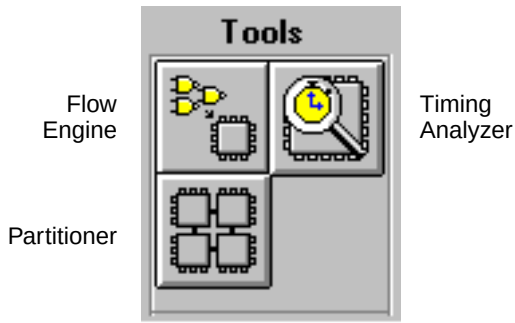


Figure 4-53 Toolbox for EPLD XC7000 Devices

Mouse Accelerator Buttons

The right mouse button provides quick access to often used commands.

Design Manager Mouse Accelerator Buttons

The following mouse commands are active in the Project View in the Design Manager's main window. The mouse commands are listed below with cross-references to the equivalent menu commands.

- *Implement* — Start implementation process.
  See "Implement Command (Design Menu)" on page 4-23.
- *Reports* — View reports.
  See "Report Browser Command (Utilities Menu)" on page 4-42.
- *Export* — Export design data.
  See "Export Command (Design Menu)" on page 4-19.
- *New Revision* — Create a new revision.
  See "New Revision Command (Design Menu)" on page 4-34.
- *Browse Revision* — Edit, copy, move, rename, and delete design revision files.
  See "Browse Revision Command (Design Menu)" on page 4-8.
- *Copy Revision* — Make a copy of the selected revision.
  See "Copy Revision Command (Design Menu)" on page 4-16.

- *Delete* — Delete the selected version, device, or revision. See "Delete Command (Design Menu)" on page 4-17.

Flow Engine Mouse Accelerator Buttons

The following mouse menu commands are active in the Flow Engine's text/message window. There are no equivalent menu commands for these mouse commands.

- *Copy* — Copy selected text to the clipboard.
- *Search* — Search for a text string.

Text Editor Commands

The Design Manager opens the Text Editor (see Figure 4-54) for you to view reports in the Report Browser, to display errors, and also for you to write project notes. Reports are read-only so the Save, Cut, Paste, and Replace commands are not available and are grayed out. All commands are active in the project notes mode. The Text Editor menu command descriptions are listed below in alphabetical order.

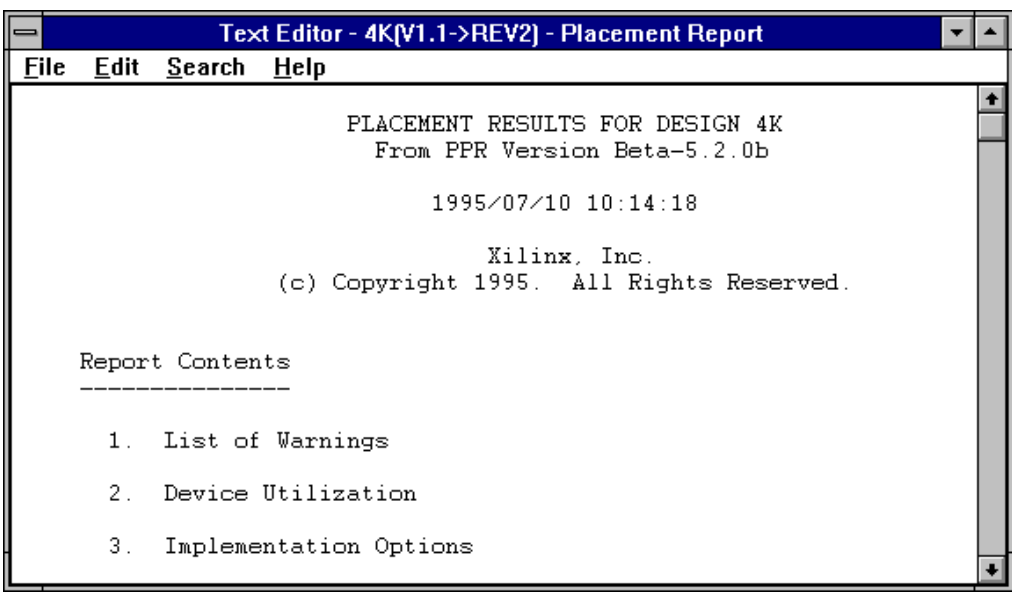


Figure 4-54 Text Editor

About Text Editor Command (Help Menu)

Displays the Text Editor version and copyright information.

Contents Command (Help Menu)

Goes to the contents page of Design Manager Help.

Copy Command (Edit Menu)

Copies selected text and places it on the clipboard, leaving the original text intact and replaces the previous clipboard contents. This command is available only when text is selected.

Cut Command (Edit Menu)

Deletes selected text from a document and places it onto the clipboard, replacing the previous clipboard contents. This command is available only when text is selected. It is unavailable and grayed out in files that cannot be modified such as reports.

Exit Command (File Menu)

Closes the current document and quits the Text Editor. You are prompted to save unsaved changes.

Find Command (Search Menu)

Use this command to search for text in a Text Editor document. This command opens the Find dialog box shown in Figure 4-55. The options are described below.

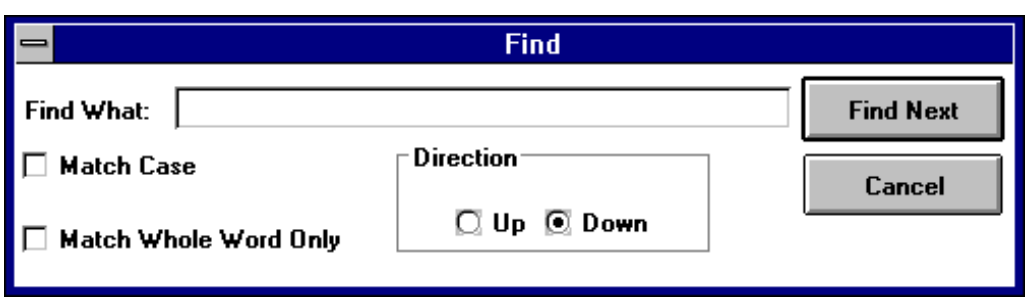


Figure 4-55 Find Dialog Box

Find Dialog Box Options

Find What

Type the word or phrase you wish to search for.

Match Case

Search for the same case as the letters you type in the Find What box.

Match Whole Word Only

Only search for the whole word that you type in the Find What box and do not search for words that contain the search word as part of but not all of its letters.

Direction Up/Down

Set the search direction in the document. You can search from the cursor point up to the beginning of the document or from the cursor point down to the end of the document.

Find Next

Click this button to find the next text phrase.

Find Next Command (Search Menu)

Finds the next occurrence of the string specified in the Find command.

Font Command (Edit Menu)

Opens the Font dialog box (see Figure 4-56) in which you can specify a font type and font size for displaying text in the Text Editor. The Preview box in the Font dialog box shows an example of text displayed with the font type and font size that you specify.

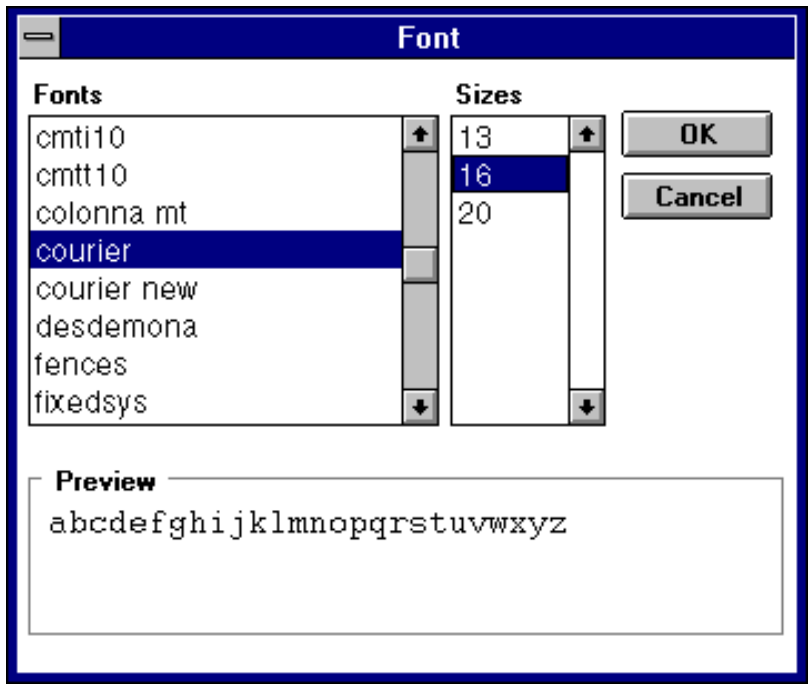


Figure 4-56 Font Dialog Box

Page Setup Command (File Menu)

Opens the Page Setup dialog box (see Figure 4-57) in which you can specify the page margins on the printed pages and the measurement units in either inches or centimeters.

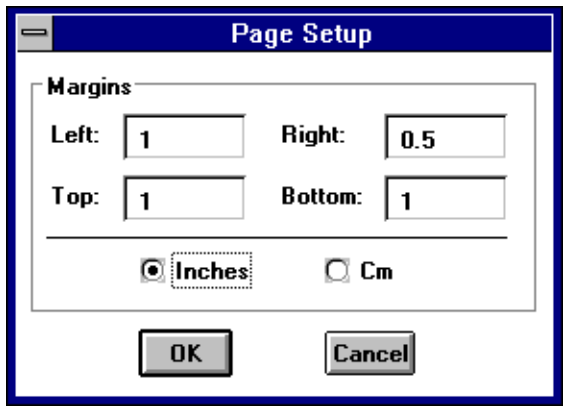


Figure 4-57 Page Setup Dialog Box

Paste Command (Edit Menu)

Inserts the information on the clipboard at the text insertion point. This command becomes available when information has been copied or cut and placed onto the clipboard. It is unavailable and grayed out in files that cannot be modified such as reports.

Print Command (File Menu)

Opens the Print dialog box (see Figure 4-58) in which you specify the number of copies to print and the print quality and send the document to the printer.

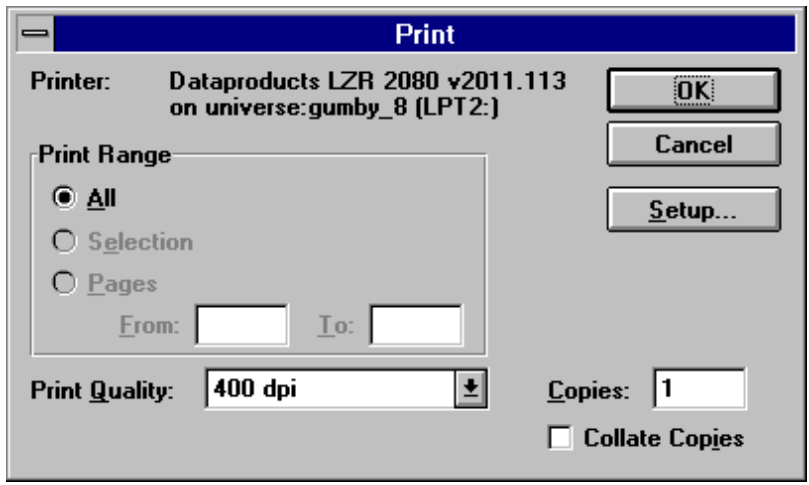


Figure 4-58 Print Dialog Box

Print Dialog Box Options

Printer

Specifies the current printer.

Print Range

The print range is always set to All so that the entire document is printed. The Selection and Pages radio buttons are not supported in the Design Manager and are grayed out.

Print Quality

Set this to the dpi (dots per inch) setting of your printer.

Copies

The number of copies you wish to print.

Collate Copies

Prints one complete copy before starting the next copy.

Setup

Opens the Print Setup dialog box shown in Figure 4-59.

Print Setup Command (File Menu)

Opens the standard Windows Print Setup dialog box for you to specify your printer, page orientation, and paper size.

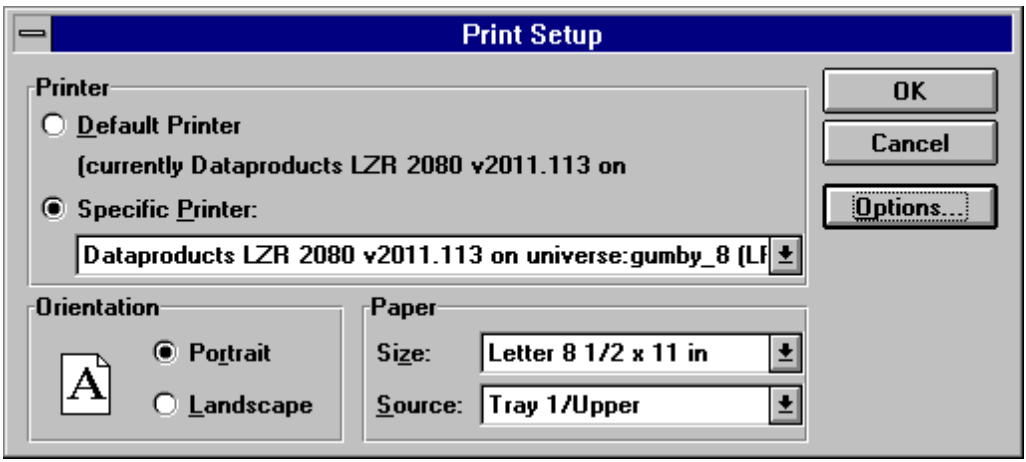


Figure 4-59 Print Setup Dialog Box

Print Setup Dialog Box Options

Default Printer

Uses the your default Windows printer.

Specific Printer

Uses the printer that you select in the Specific Printer popup menu.

Orientation

Specifies the orientation of the output on the printed page.

Portrait

The long edge of the page is in the vertical direction.

Landscape

The long edge of the page in the horizontal direction.

Paper

Specify the paper size and the desired paper tray on your printer.

Options

Opens the standard Windows Print Options dialog box. This box is explained in the Windows online help if you click the Help button in this dialog box.

Replace Command (Search Menu)

Use this command to search for and replace text in a Text Editor document. This command opens the Replace dialog box shown in Figure 4-60.This command is unavailable and grayed out in files that cannot be modified such as reports.

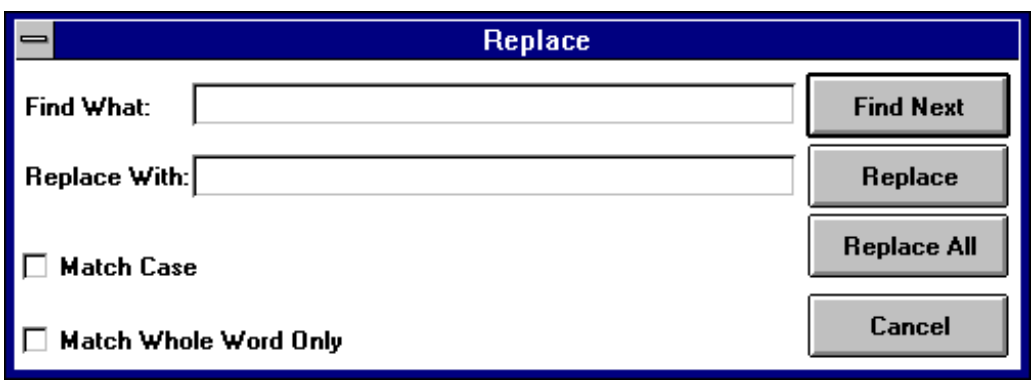


Figure 4-60 Replace Dialog Box

Replace Dialog Box Options

Find What

Type the word or phrase you wish to search for.

Replace With

Type the word or phrase with which you wish to replace the found text.

Match Case

Search for the same case as the letters you type in the Find What box.

Match Whole Word Only

Only search for the whole word that you type in the Find What box and do not search for words that contain the search word as part of but not all of its letters.

Find Next Button

Find the next occurrence of the text in the Find What box.

Replace Button

Replace the found text with the text in the Replace With box.

Replace All Button

Replace all occurrences of the text in the Find What box the text in the Replace With box.

Save Command (File Menu)

Saves changes to the document you have been working on. This command is unavailable and grayed out in files that cannot be modified such as reports.

SaveAs Command (File Menu)

Saves a new or existing document. You can save a new document in text format. You can name a new document or save an existing document under a new name. The original document remains unchanged.

Search for Help On Command (Help Menu)

Opens the Search dialog in the Design Manager Help so you can search for information.

Select All Command (Edit Menu)

Selects all the text in the document.

Word Wrap Command (Edit Menu)

Toggles word wrapping in the Text Editor window. It also toggles the horizontal scroll bar if lines of text are wider than the window.

Standard Dialog Boxes

This section describes standard dialog boxes that are used in several places in the Design Manager and Flow Engine.

File Selection Dialog Box

A standard file selection dialog box (see Figure 4-61) is used in several places in the Design Manager and Flow Engine.

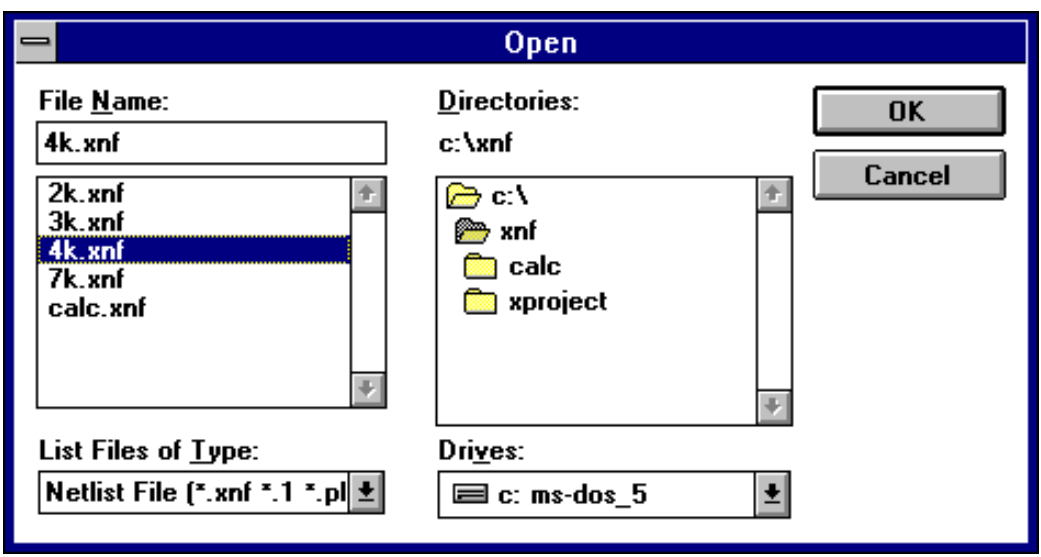


Figure 4-61 File Selection Dialog Box

File Selection Dialog Box Options

File Name

Select or type the name of the file you want to open. This box lists files with the filename extension selected in the List Files of Type box.

List Files of Type

Select the type of file you want to see in the File Name list.

Directories

Select the directory that contains the file you want to open.

Drives

Select the drive that contains the file you want to open.

OK

Exit the dialog box and open the file specified in the File Name box.

Cancel

Exit the File Selection dialog box without causing the software to take any action.

Directory Selection Dialog Box

A standard directory selection dialog box (see Figure 4-62) is used in several places in the Design Manager and Flow Engine.

Figure 4-62 Directory Selection Dialog Box

Directory Selection Dialog Box Options

Directories

Select the directory that contains the directory you want to open. Double click to open a directory.

Drives

Select the drive that contains the directory you want to open.

OK

Exit the dialog box and select the directory specified in the Directory Name box.

Cancel

Exit the Directory Selection dialog box without causing the software to take any action.

Keyboard Shortcuts

You can use the following keyboard shortcuts in the Design Manager and Flow Engine. Most of the things you can do with the mouse, you can also do with the keyboard.

Alt

Access menus in the Design Manager and Flow Engine.

Esc

Cancel a dialog.

Tab

Navigate within a dialog box.

Shift Tab

Navigate within a dialog box in reverse direction.

Enter

Select the specified control.

Chapter 5

Implementation Options

This chapter describes the Flow Engine implementation options. The implementation options control how the Flow Engine implements a design. This chapter covers the following topics:

- Design Implementation Options Dialog Box
- XC2000 and XC3000 Implementation Template Dialog Box
- XC3000A, XC4000, and XC5200 Implementation Template Dialog Box
- XC7000 Implementation Template Dialog Box
- XC2000 Configuration Template Dialog Box
- XC3000, XC3000A Configuration Template Dialog Box
- XC4000 and XC5200 Configuration Template Dialog Box

Design Implementation Options Dialog Box

Use the Design Implementation Options dialog box (see Figure 5-1) to set various settings for implementing a design. There are several ways to open this dialog box:

- From the Design Manager Design menu, choose Implement.
- From the Flow Engine Setup menu, choose Options.
- In the Project View, press the right mouse button, and select Implement from the popup menu
- Double click on a revision in the Project View.

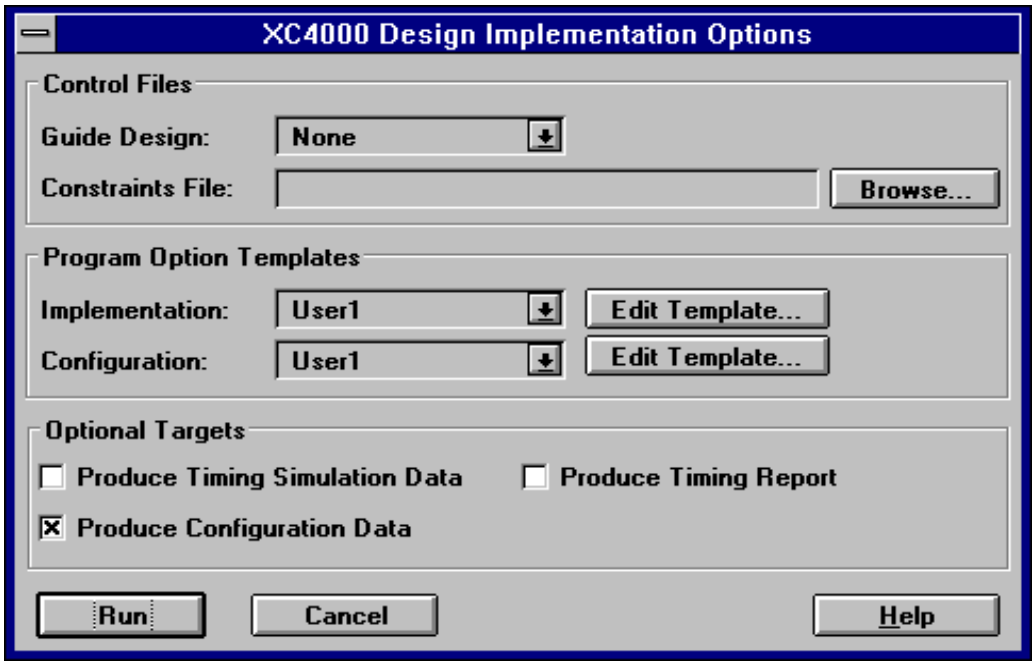


Figure 5-1 Design Implementation Options Dialog Box

Except for the dialog box title bar, the Design Implementation Options dialog box shown in Figure 5-1 is the same for all devices except the XC7000. The XC7000 Design Implementation Options dialog box is shown in Figure 5-2.

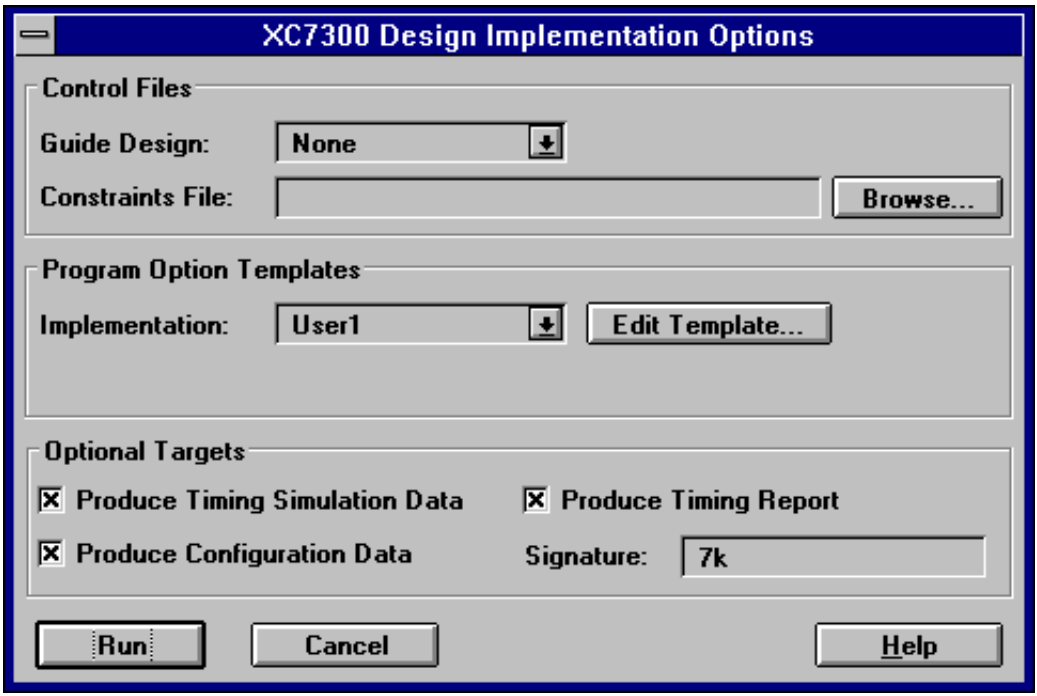


Figure 5-2 XC7000 Design Implementation Options Dialog Box

Design Implementation Options Dialog Box Options

Run/OK

The name and function of this button differs depending on how you open the Design Implementation Options dialog box. It is a Run button if you open the dialog from the Design Manager but is an OK button if you open the dialog from the Flow Engine.

Run

Closes the Design Implementation Options dialog box and starts the implementation process using the read-only Flow Engine.

OK

Closes the Design Implementation Options dialog box and saves any user specified settings but does not start implementation.

Guide Design

Specifies a design revision to use as a guide for this implementation. For more information, see "Guiding a Design" on page 3-20. A guide file is created each time you implement your design and you can reuse this data to maintain design consistency.

Constraints File

Specifies a constraints file to use for this implementation. For FPGAs, you can specify logic placement and timing requirements in a constraints file. For EPLDs, you can specify timing requirements in a constraints file.

Implementation — Pull-Down List

Selects an option template to use for this implementation. All the implementation templates that you have created with the Template Manager command appear when you click on the Implementation pull-down menu.

Implementation — Edit Template Button

Opens the Implementation Template dialog box. The options in this box depend on the target device family. For information on how to use the implementation template options, see one of the following topics:

- "XC2000 and XC3000 Implementation Template Dialog Box" on page 5-5
- "XC3000A, XC4000, and XC5200 Implementation Template Dialog Box" on page 5-7
- "XC7000 Implementation Template Dialog Box" on page 5-13

Configuration — Pull-Down List

Selects a configuration template to use for this implementation. All the configuration templates that you have created with the Template Manager command appear when you click on the Configuration pull-down menu.

Configuration — Edit Template button

Opens the Configuration dialog box. The options in this dialog box depend on the device family that you are using. For information on the configuration options, see one of the following topics:

- "XC2000 Configuration Template Dialog Box" on page 5-20
- "XC3000, XC3000A Configuration Template Dialog Box" on page 5-22
- "XC4000 and XC5200 Configuration Template Dialog Box" on page 5-27

Note: There are no configuration options for the XC7000 device family.

Produce Timing Report

Enables the Flow Engine to produce a timing report. The timing report provides a brief analysis of the estimated maximum clock speed for the design. To obtain a detailed analysis, use the Timing Analyzer tool.

Produce Timing Simulation Data

Enables the Flow Engine to produce timing simulation data. See"Producing Timing Simulation Data" on page 3-24 for more information.

Produce Configuration Data

Enables the Flow Engine to produce configuration data. The configuration data is used to program a device.

XC2000 and XC3000 Implementation Template Dialog Box

When you select the Implementation Edit Template button in the Design Implementation Options dialog box (see Figure 5-1), the Implementation Options dialog box appears. Use this dialog box to set the options described below.

Click OK to accept the template, click Cancel to return to the previous menu, click Default to set the default options, or click Help to get online help.

Implementation Options Dialog Box Options

The XC2000 Implementation Template dialog box is shown in Figure 5-3. The XC3000 Implementation Options dialog box is identical except for the title bar. The options are described below.

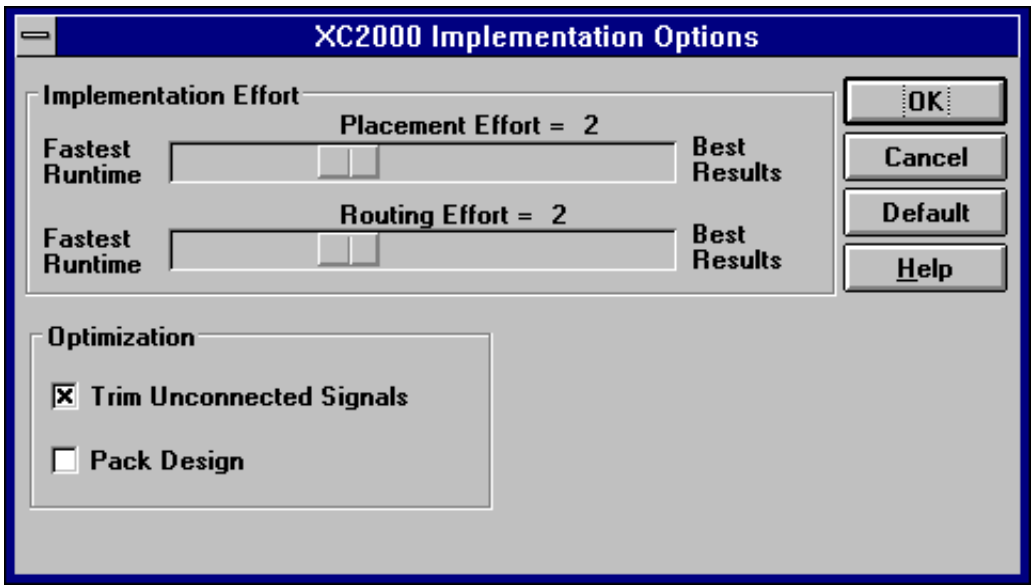


Figure 5-3 XC2000 Implementation Template Dialog Box

Placement Effort

Placement effort level refers to how hard the Flow Engine tries to place a design. Using the Placement Effort slider bar, you can select an effort level setting of 1, 2, 3, or 4. Higher effort provides better placement results at the expense of longer run times.

Routing Effort

Routing effort level refers to how hard the Flow Engine tries to route a design. Using the Routing Effort slider bar, you can select an effort level setting of 1, 2, 3, or 4. Higher effort provides better routing results at the expense of longer run times.

Trim Unconnected Signals

When this option is selected, the Flow Engine trims sourceless or loadless signals. When unselected, the Flow Engine retains sourceless or loadless signals and adds the Savesig "S" parameter to them. Disable this option if you are implementing an incomplete design to prevent partial logic form being trimmed.

Pack Design

This option partitions logic more densely. Normally the Flow Engine partitions logic to maximize signal sharing within CLBs and to minimize routing congestion. The Pack Design option optimizes density by relaxing the requirement for a high degree of signal sharing between logic elements in a CLB, using the DI (direct flip-flop input) pins on CLBs, and reducing minimum signal combining requirements.

Note: Although the Pack Design option makes a design denser, it can also adversely affect place and route performance, resulting in higher delays and more unrouted nets. Use this option if you are willing to trade performance for density.

XC3000A, XC4000, and XC5200 Implementation Template Dialog Box

When you select the Implementation Edit Template button in the Design Implementation Options dialog box (see Figure 5-1), the Implementation Template dialog box appears (see Figure 5-4). Use this dialog box to set the options described below. Except where stated otherwise, all option descriptions in this section apply to the XC3000A, XC4000, and XC5200.

Click OK to accept the template, click Cancel to return to the previous menu, click Default to set the default options, or click Help to get online help.

Dialog Box Options — Implementation Tab

The Implementation tab of the XC4000 Implementation Template dialog box is shown in Figure 5-4. The XC3000A and XC5200 dialog boxes are identical except for the title bar. The options are described below.

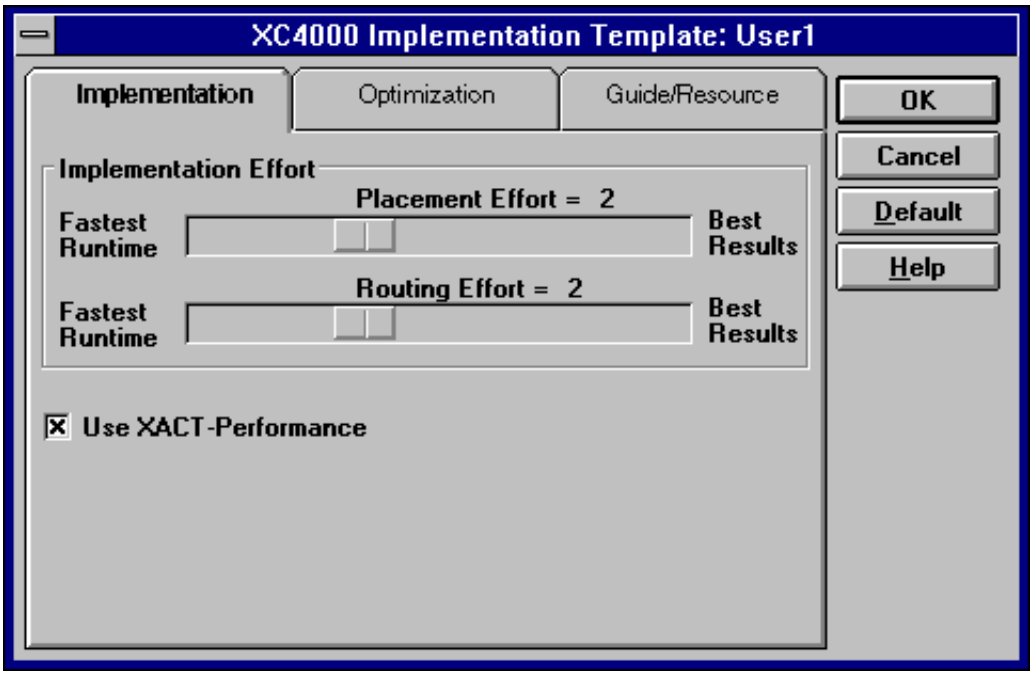


Figure 5-4 XC4000 Implementation Template Dialog Box, Implementation Tab

Placement Effort

Placement effort level refers to how hard the Flow Engine tries to place a design. Using the Placement Effort slider bar, you can select an effort level setting of 1, 2, 3, or 4. Higher effort provides better placement results at the expense of longer run times.

Routing Effort

Routing effort level refers to how hard the Flow Engine tries to route a design. Using the Routing Effort slider bar, you can select an effort level setting of 1, 2, 3, or 4. Higher effort provides better routing results at the expense of longer run times.

Use XACT-Performance

When this option is selected, the Flow Engine uses the timing specifications in the design file and performs path analysis routines to produce a high-performance implementation of the design.

Dialog Box Options — Optimization Tab

The Optimization tab of the XC3000A Implementation Template dialog box is shown in Figure 5-5. The XC4000 and XC5200 dialog boxes are identical except that the title bars are different and do not have the Pack Design option. The options are described below.

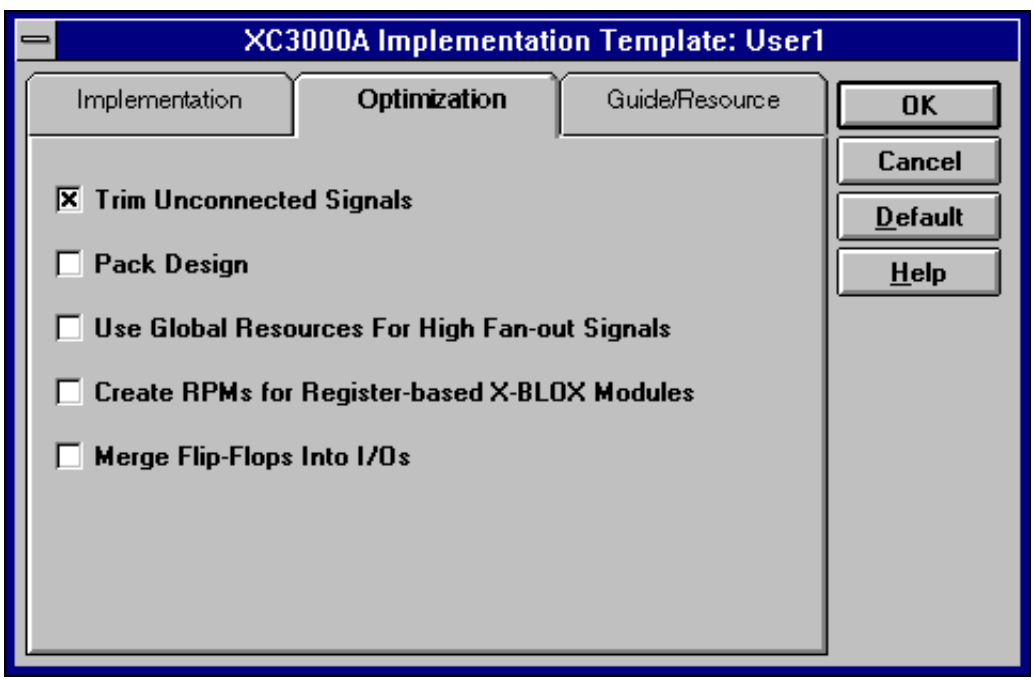


Figure 5-5 XC3000A Implementation Template Dialog Box, Optimization Tab

Trim Unconnected Signals

When this option is selected, the Flow Engine trims sourceless or loadless signals. When unselected, the Flow Engine retains sourceless or loadless signals and adds the Savesig "S" parameter to them. Disable this option if you are implementing an incomplete design to prevent partial logic form being trimmed.

Pack Design (XC3000A only)

This option instructs the Flow Engine to partition logic more densely. Normally the Flow Engine partitions logic to maximize signal sharing within CLBs and to minimize routing congestion. The Pack Design option causes the Flow Engine to ease the requirements for combining logic, permit the use of direct flip-flop input pins, and relax the minimum signal combining requirements.

Note: Although this option makes a design denser, it can adversely affect place and route performance, resulting in higher delays and more unrouted nets. Use this option only if you are willing to trade performance for density.

Use Global Resources for High Fan-out Signals

When this option is selected, the Flow Engine runs the XBLOX program to perform architectural optimizations. This routes high fan-out signals through unused global buffers.

Create RPMs for Register Based Logic

This option allows the Flow Engine to generate RPMs for X-BLOX modules that do not contain carry logic. These modules are DATA_REG, SHIFT, CLK_DIV, and COUNTER for styles other than binary. RPMs for these modules usually result in higher performance. However, excessive RPMs in a design may create difficulty for the placement tools.

Merge Flip-Flops into I/Os

When this option is selected, the Flow Engine runs the XBLOX program to merge flip-flops into IOBs where possible.

Dialog Box Options — Guide/Resource Tab

The Guide/Resource tab of the XC3000A Implementation Template dialog box is shown in Figure 5-6. The XC4000 and XC5200 dialog boxes are identical except that there is no None option for CLBs. The options are described below.

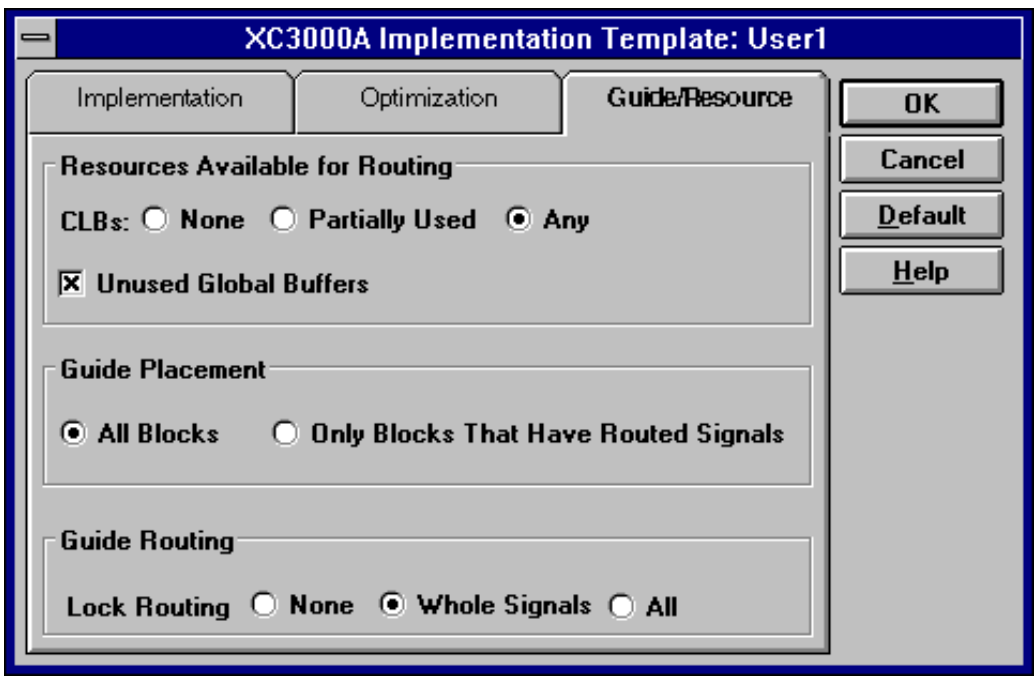


Figure 5-6 XC3000A Implementation Template Dialog Box, Guide/Resource Tab

CLBs

To improve routability and timing, the Flow Engine may use through-routes, which route some signals through CLB or other blocks. This usually improves routing but sometimes you may want to limit this activity. You can do this with the following option settings:

None

Prevents the router from ever routing through a block. This option can make the design more difficult to route and degrade the overall design timing. In some cases it can prevent a design from routing completely. The None setting is not available for XC4000 and XC5200 designs.

Partially Used

The router may route through blocks which are partially used by the design. For example, if the flip-flops in a given CLB are already used, the Flow Engine is allowed to route through the unused function generator in that CLB. This option is useful for incremental design, because it prevents the Flow Engine from using CLBs outside the current functional block's area.

Any

The router may route through any block to improve the routability and timing of the design.

Unused Global Buffers

This option allows the router to route through unused global buffers (BUFGS in the XC4000 or GCLK and ACLK in the XC3000) if doing so is more efficient than using general interconnect.

Guide Placement

This option controls the amount of guiding that will be applied from the guide file to the current design. This parameter may be assigned one of these values:

All Blocks

Instructs the placement tools to guide all blocks from the guide file that are matched in the input design.

Only Blocks that Have Routed Signals

Instructs the placement tools to guide only those blocks that have some routing connected to them in the guide file and that are matched in the input design.

Lock Routing

This option controls whether routing improvements and changes can be made to routing results taken from a guide file. This parameter may be assigned one of these values:

None

Instructs the routing software that none of the guided routing is locked. Thus, all guided routing can be discarded and re-routed to improve timing.

Whole Signals

Instructs the routing software that signals that have all pins matched in the guide file are locked. Signals which have all pins matched in the guide file are not re-routed.

All

Instructs the routing software that all guided signals are locked. No guided signals are re-routed.

XC7000 Implementation Template Dialog Box

When you select the Edit Template button in the Design Implementation Options dialog box (see Figure 5-7), the Implementation Template dialog box appears (see Figure 5-8). Use this dialog box to set the options described below.

Click OK to accept the template, click Cancel to return to the previous menu, click Default to set the default options, or click Help to get online help.

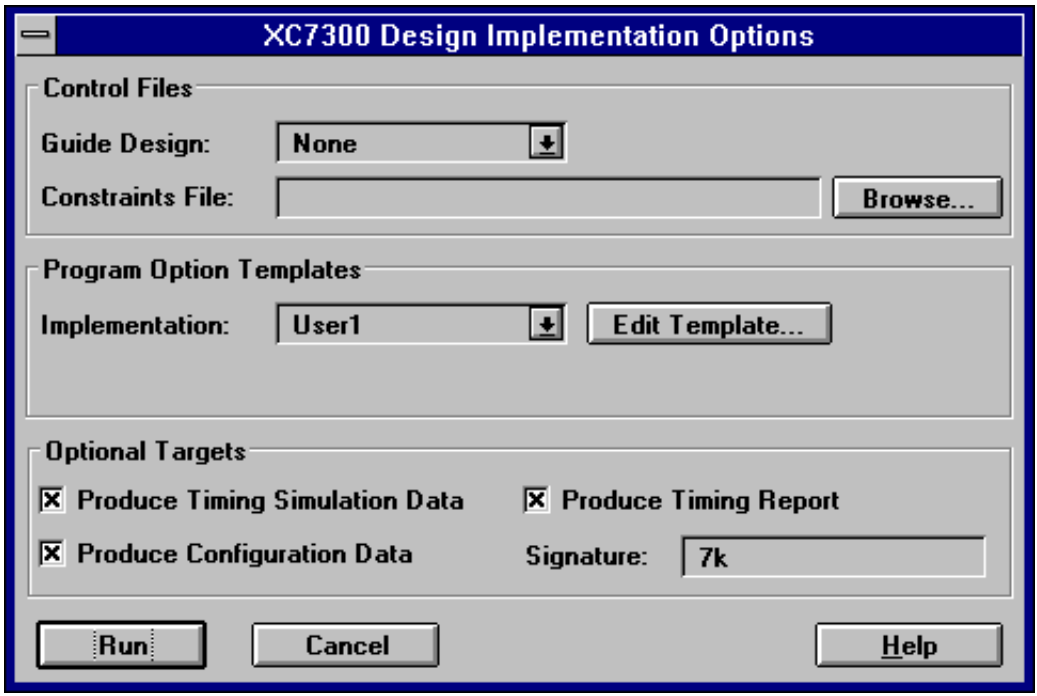


Figure 5-7 XC7000 Design Implementation Options Dialog Box

Dialog Box Options — Fitting Tab

The Fitting tab of the XC7000 Implementation Template dialog box is shown in Figure 5-8. The options are described below.

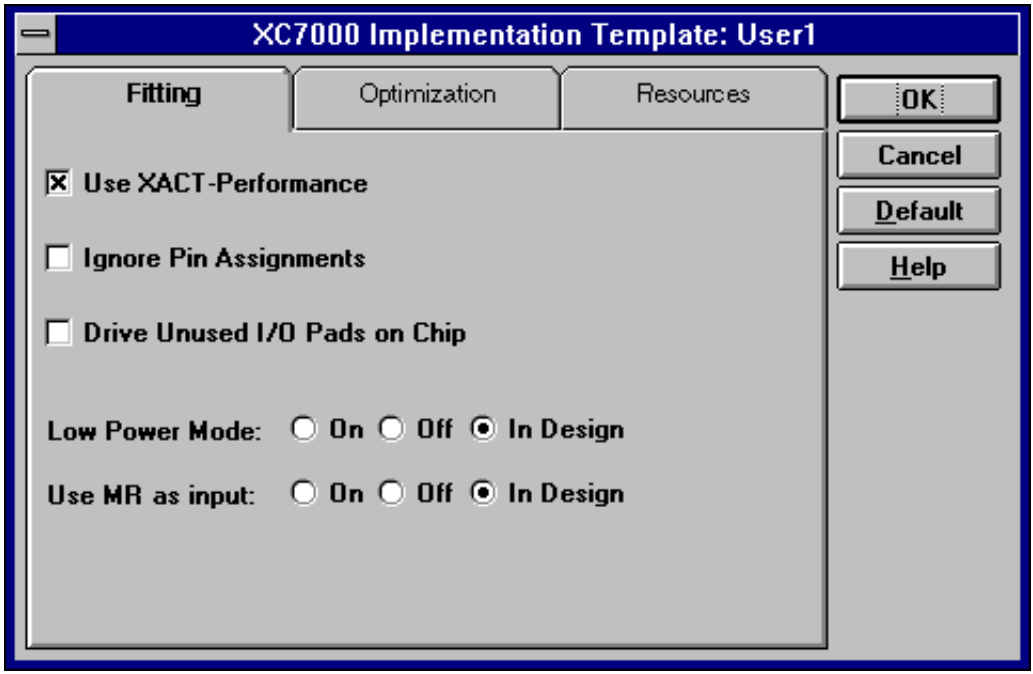


Figure 5-8 XC7000 Implementation Template Dialog Box, Fitting Tab

Use XACT-Performance

This indicates that you want the software to use your T-Spec information and perform timing-driven optimization in the fitting of your design. For this option to be useful, you must have previously created a timing constraints file or you must have placed T-Spec information on your schematic.

Ignore Pin Assignments

This indicates that you do not want to use any pinout information that may be in the design file or in a pin save (CFG) file. This allows the fitter to place pins anywhere.

Drive Unused I/O Pads On Chip

This indicates that you want all unused I/O pads to be actively driven by on chip circuitry. Because all unused I/O signals must be actively driven, this option alleviates the need for external drivers or pullup resistors.

Low Power Mode

Controls device power consumption.

On

Set Low Power mode for the entire design.

Off

Set high performance (higher power mode) for the entire design.

In Design

Allow the power mode to be controlled by information in your design file.

Use MR As Input

Controls the use of the MR Input pin on the XC7318, XC7336, and XC7354.

On

Use the MR pin as an input pin.

Off

Use the MR pin as a Master Reset input pin.

In Design

Allow the pin use to be determined by information in your design file.

Dialog Box Options — Optimization Tab

The Optimization tab of the XC7000 Implementation Template dialog box is shown in Figure 5-9. The options are described below.

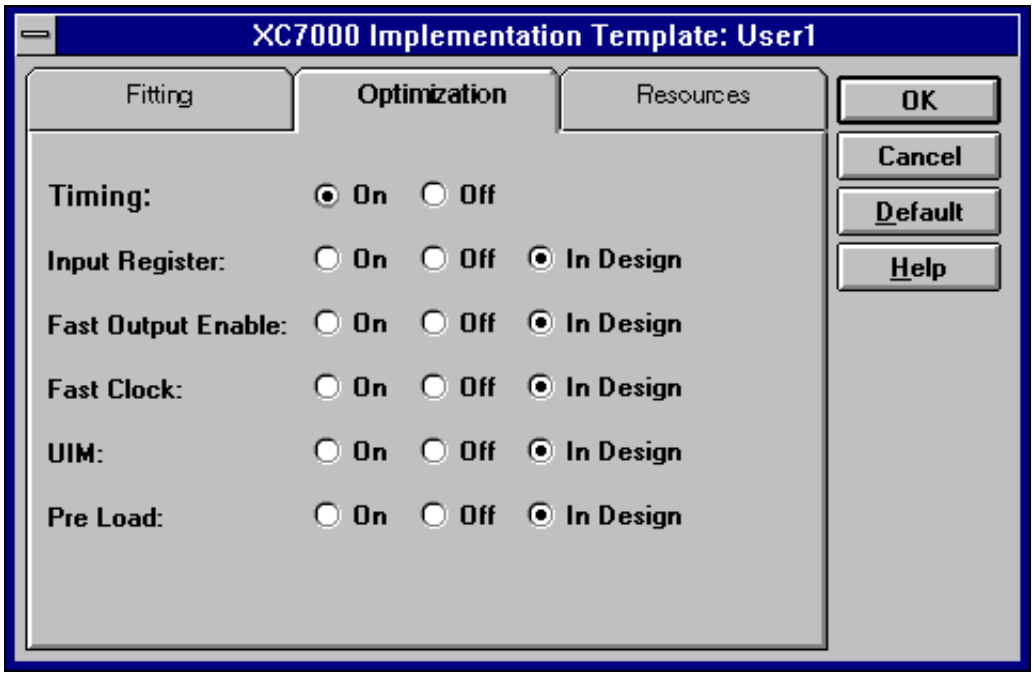


Figure 5-9 XC7000 Implementation Template Dialog Box, Optimization Tab

On, Off, In Design Buttons

You can control the optimization options with the following:

On

The option is activated for the whole design and corresponding schematic attributes, behavioral commands, or VHDL commands are ignored.

Off

The option is turned off for the whole design and corresponding schematic attributes, behavioral commands, or VHDL commands are ignored.

In Design

The option is controlled exclusively by schematic attributes, behavioral commands, or VHDL commands. If the option is not specified in the design, it defaults to On.

Input Register

Determines if unused input registers can be used to implement logic.

Fast Output Enable

Determines if output enable signals can use the dedicated high speed FOE nets.

Fast Clock

Determines if clocks can use the dedicated FastClock nets.

UIM

Determines if the UIM can be used to implement basic boolean logic functions.

Pre Load

Determines if the fitter can optimize registers that have no assigned preload values. This optimization allows the software to choose preload values that simplify fitting.

Note: See the XC7000 data sheets for more information on how these options affect your design.

Implementation Template Options — Resources Tab

The Resources tab of the XC7000 Implementation Template dialog box is shown in Figure 5-10. The options are described below.

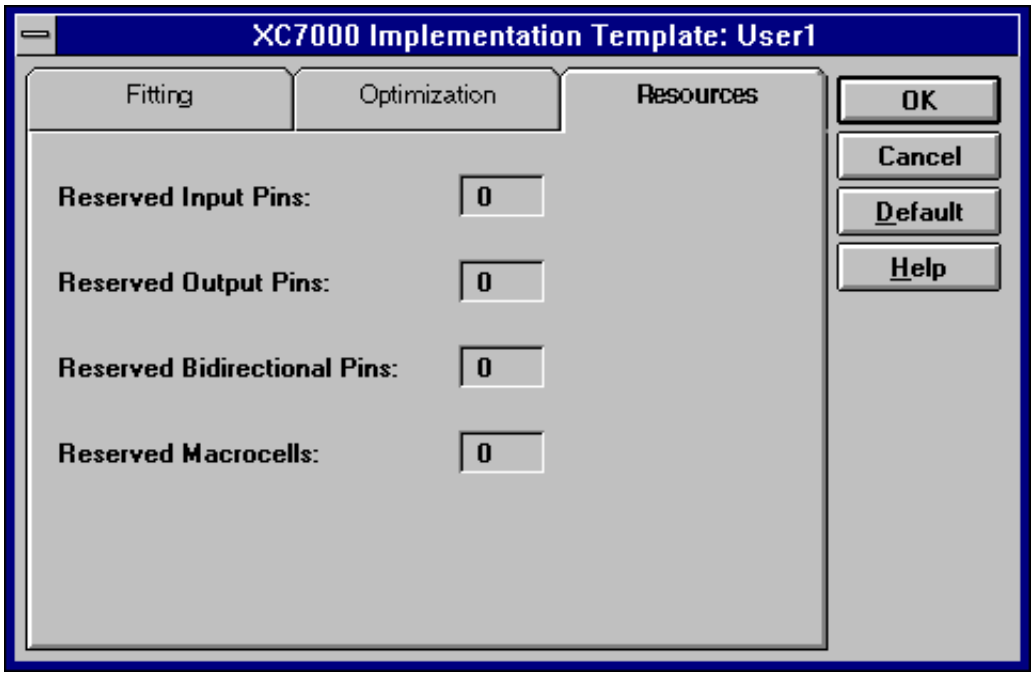


Figure 5-10 XC7000 Implementation Template Dialog Box, Resources Tab

You can control the amount of device resources reserved for future use with the following options.

Reserved Input Pins

Specifies the number of input pins to leave unused.

Reserved Output Pins

Specifies the number of Output pins to leave unused.

Reserved I/O Pins

Specifies the number of I/O pins to leave unused.

Reserved Macro Cells

Specifies the total number of macro cells to reserve.

XC2000 Configuration Template Dialog Box

When you select the Configuration Edit Template button in the Design Implementation Options dialog box (see Figure 5-1), the Configuration dialog box appears. Use this dialog box to set the options described below.

Click OK to accept the template, click Cancel to return to the previous menu, click Default to set the default options, or click Help to get online help.

Configuration Dialog Box Options

The XC2000 Configuration dialog box is shown in Figure 5-11. The options are described below.

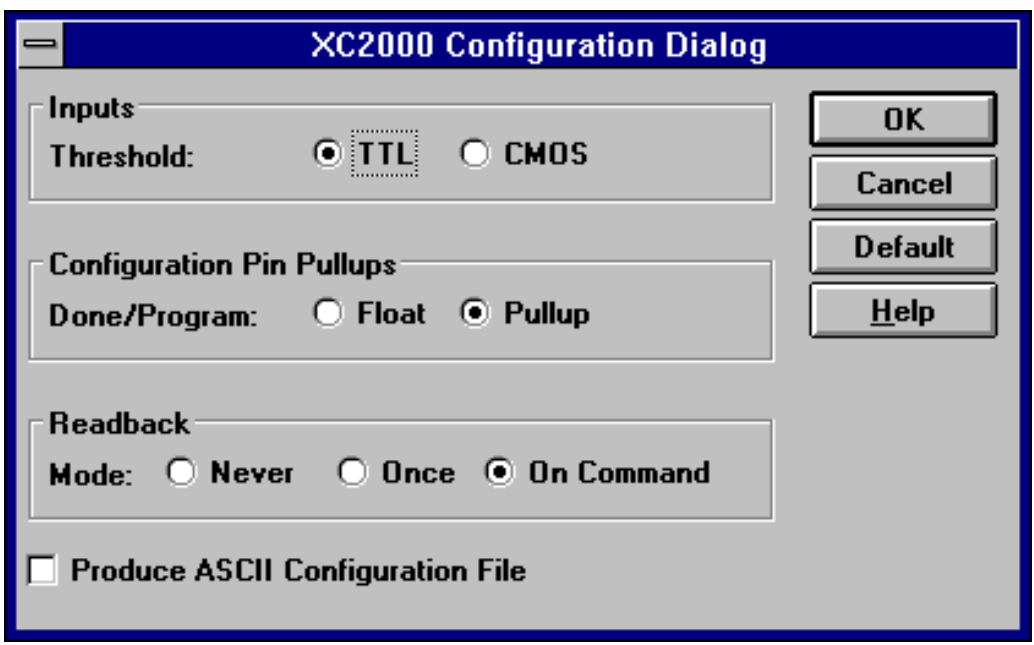


Figure 5-11 XC2000 Configuration Template Dialog Box

Inputs — Threshold

TTL

Specifies TTL compatible inputs except for the special purpose clocks, Tclkin, Bclkin, and Pwrdwn which always require CMOS input signals.

CMOS

Specifies CMOS compatible inputs.

Configuration Pin Pullups — Done/Program

Float

This option disables an internal pull-up resistor on the Done/Program (D/P) pin. The D/P pin is an open-drain output that requires a pull-up resistor to indicate the end of the configuration. If this option is selected, an external pull-up resistor should be connected to the D/P pin.

Pull-Up

This option enables an internal pull-up resistor on the Done/Program (D/P) pin. This resistor has a value of 2 to 8 kohm. The D/P pin is an open-drain driver that requires a pull-up resistor to indicate the end of the configuration. Turn off this option only if you intend to connect an external pull-up resistor to this pin.

Readback Mode

After an LCA is configured, data can be read back and compared with the original configuration data. For security reasons it is sometimes desirable to disable or limit readback capability. The following options control readback:

Never

Disables readback

Once

Enables a one-time readback

On Command

Enables readback on command.

Produce ASCII Configuration File

This option creates a rawbits (RBT) file in addition to the binary BIT file. The RBT file is a text file that contains ASCII 1s and 0s. These characters represent the actual bits that are contained in the configuration bitstream which are downloaded to the FPGA.

XC3000, XC3000A Configuration Template Dialog Box

When you select the Configuration Edit button in the Design Implementation Options dialog box (see Figure 5-1), the Configuration Template dialog box appears as shown in Figure 5-12. The same dialog box is used for the XC3000 and XC3000A. Use this dialog box to set the options described below.

Click OK to accept the template, click Cancel to return to the previous menu, click Default to set the default options, or click Help to get online help.

Dialog Box Options — Configuration Tab

The Configuration tab of the XC3000 Configuration Template dialog box is shown in Figure 5-12. The options are described below.

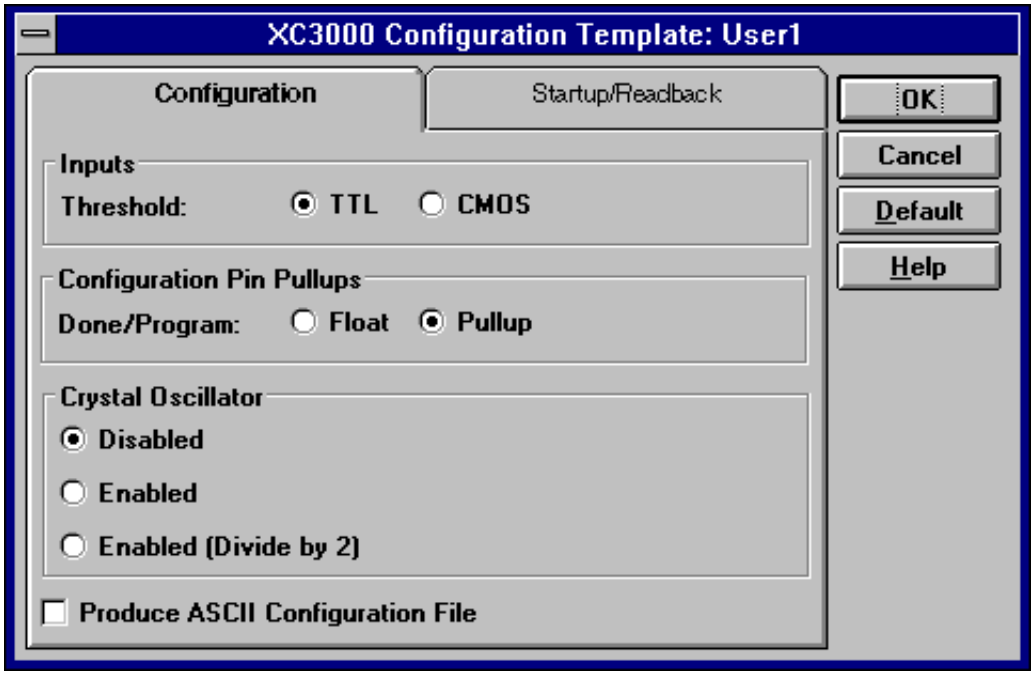


Figure 5-12 XC3000 Configuration Template Dialog Box, Configuration Tab

Inputs — Threshold

TTL

Specifies TTL compatible inputs except for the special purpose clocks, Tclkin, Bclkin, and Pwrdwn which always require CMOS input signals.

CMOS

Specifies CMOS compatible inputs.

Configuration Pin Pullups — Done/Program

Float

This option disables an internal pull-up resistor on the Done/Program (D/P) pin. The D/P pin is an open-drain output that

requires a pull-up resistor to indicate the end of the configuration. If this option is selected, an external pull-up resistor should be connected to the D/P pin.

Pull-Up

This option enables an internal pull-up resistor on the Done/Program (D/P) pin. This resistor has a value of 2 to 8 kohm. The D/P pin configures an open-drain driver that requires a pull-up resistor to indicate the end of the configuration. Turn-off this option only if you intend to connect an external pull-up resistor to this pin.

Crystal Oscillator

The XC3000 family of devices contains an internal high-speed inverting amplifier which you can use to implement an on-chip crystal oscillator. To use this feature, you must include either the GXTL or OSC library element in your design and connect the appropriate external R-C crystal circuit to the amplifier (see the Xilinx *Libraries Guide* and *The Programmable Logic Data Book* for more information). Additionally, you must select the Enabled or Enabled (Divide by 2) option in your configuration template.

Disabled

Disables the crystal oscillator.

Enabled

Enables the crystal oscillator.

Enabled (Divide by 2)

Divides the crystal oscillator frequency by two to generate a symmetrical clock signal.

Produce ASCII Configuration File

This option creates a rawbits (RBT) file in addition to the binary BIT file. The RBT file is a text file that contains ASCII 1s and 0s. These characters represent the actual bits that are contained in the configuration bitstream which are downloaded to the FPGA.

Dialog Box Options — Startup/Readback Tab

The Startup/Readback tab of the XC3000 Configuration Template dialog box is shown in Figure 5-13. The options are described below.

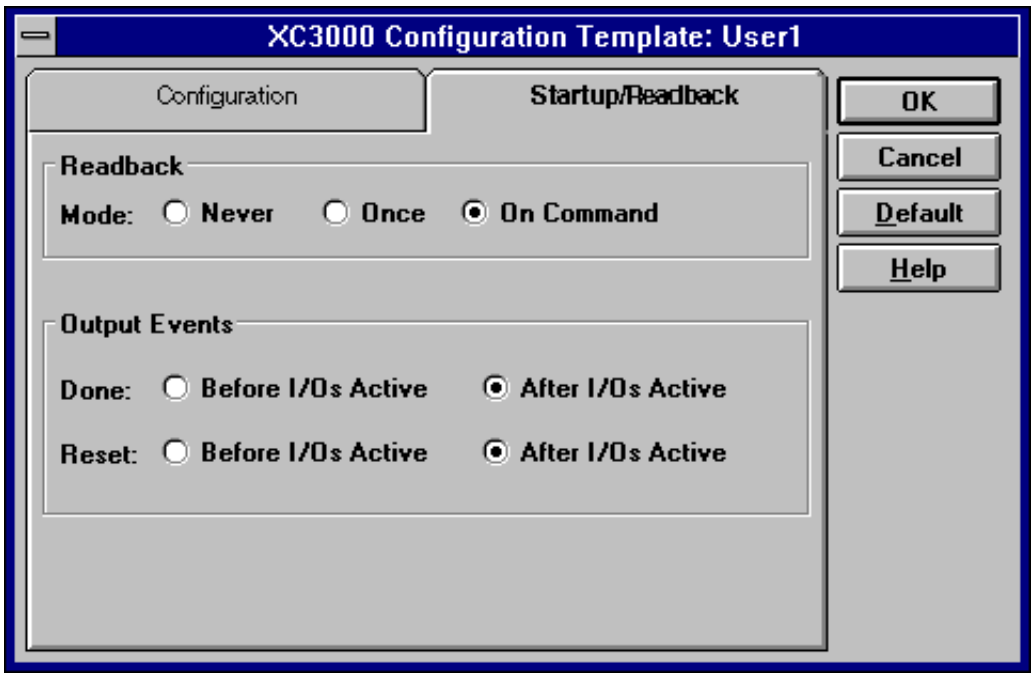


Figure 5-13 XC3000 Configuration Template Dialog Box, Startup/Readback Tab

Readback Mode

After an LCA is configured, data can be read back and compared with the original configuration data. For security reasons it is sometimes desirable to disable or limit readback capability. The following options control readback:

Never

Disables readback

Once

Enables a one-time readback

On Command

Enables readback on command.

Output Events — Done

The Done Signal indicates the completion of the configuration sequence. You can program this signal to be asserted before or after I/Os go active.

Before I/Os Active

The Done Signal is released one Cclk period before the outputs go active. This is the default setting.

After I/Os Active

The Done Signal is released one Cclk period after the outputs go active.

Output Events — Reset

A global reset signal is asserted during the startup sequence. You can program the release of this signal to occur before or after I/Os go active.

Before I/Os Active

The Internal Reset is removed one Cclk period before the outputs go active.

After I/Os Active

The Internal Reset is removed one Cclk period after the outputs go active. This is the default setting.

XC4000 and XC5200 Configuration Template Dialog Box

When you select the Configuration Edit button in the Design Implementation Options dialog box (see Figure 5-1), the Configuration Template dialog box appears. Use this dialog box to set the options described below. Unless stated otherwise, all options in this section apply to both the XC4000 and XC5200.

Click OK to accept the template, click Cancel to return to the previous menu, click Default to set the default options, or click Help to get online help.

Dialog Box Options — Configuration Tab

The Configuration tab of the XC4000 Configuration Template dialog box is shown in Figure 5-14. The options are described below.

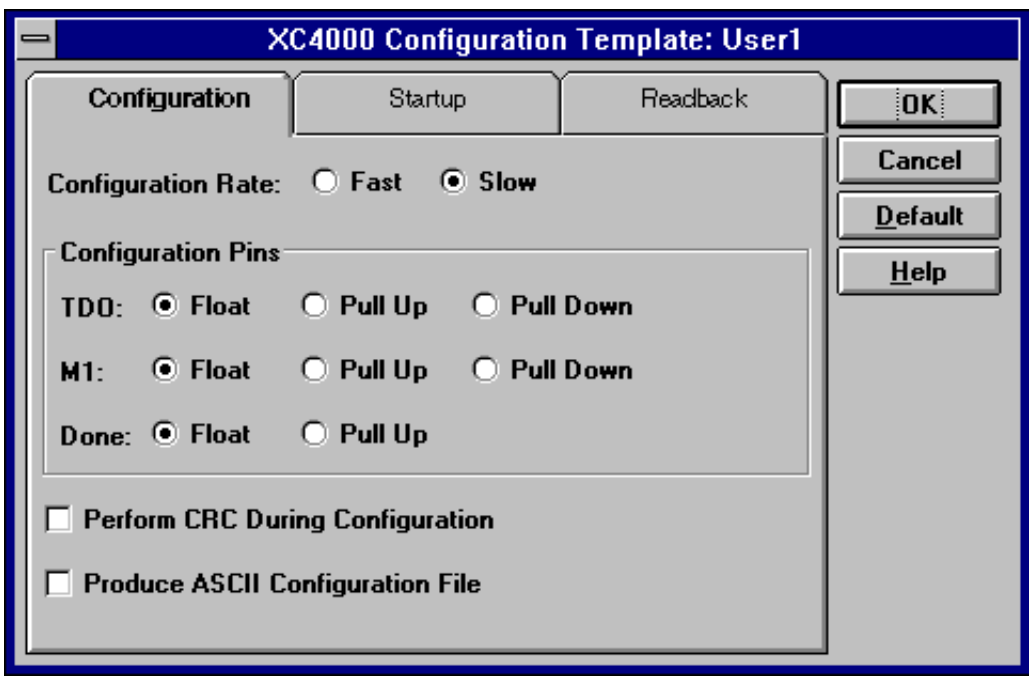


Figure 5-14 XC4000 Configuration Template Dialog Box, Configuration Tab

Configuration Rate

The XC4000 uses an internal configuration clock, CCLK, when configuring in a master mode. The configuration rate option allows you to select the rate for this clock. The options are:

Fast

Equivalent to 6MHz (nominal)

Slow

Equivalent to 1MHz (nominal)

Configuration Pins

TDO

The TDO pin can be used as tristatable output pin. The options are:

Float

Disables both the pullup resistor and pull-down resistor on the TDO pin.

Pull-Up

Enables a pull-up on the TDO pin.

Pull-Down

Enables a pull-down on the TDO pin.

M1

The M1 pin can be used as tristatable output pin. The options are:

Float

Disables both the pullup resistor and pull-down resistor on the M1 pin.

Pull-Up

Enables a pull-up on the M1 pin.

Pull-Down

Enable a pull-down on the M1 pin

DONE

Float

Disables the pullup resistor on the DONE pin. The DONE pin configures an open-drain driver that requires a pull-up resistor to indicate the end of the configuration. If you select this option, be sure you have connected an external pull-up resistor on this pin.

Pullup

This option enables an internal pull-up resistor on the DONE pin in XC4000 devices. This resistor has a value of 2 to 8 kohm. The DONE pin configures an open-drain driver that requires a pull-up resistor to indicate the end of the configuration. Select this option only if you do not connect an external pull-up resistor on this pin.

Perform CRC Check During Configuration

This option enables CRC (Cycle Redundancy Checking) error checking during configuration. If enabled, the software calculates a running CRC and insets a unique four-bit partial check at the end of each data frame in the configuration bitstream. This allows the device to perform a CRC check on the bitstream during the configuration process. If disabled, the device performs a simple check for the 0110 pattern at the end of each frame in the configuration data.

Produce ASCII Configuration File

This option creates a rawbits (RBT) file in addition to the binary BIT file. The RBT file is a text file that contains ASCII 1s and 0s. These characters represent the actual bits that are contained in the configuration bitstream which are downloaded to the FPGA.

Dialog Box Options — Startup Tab

The Startup tab of the XC4000 Configuration Template dialog box is shown in Figure 5-15. The options are described below.

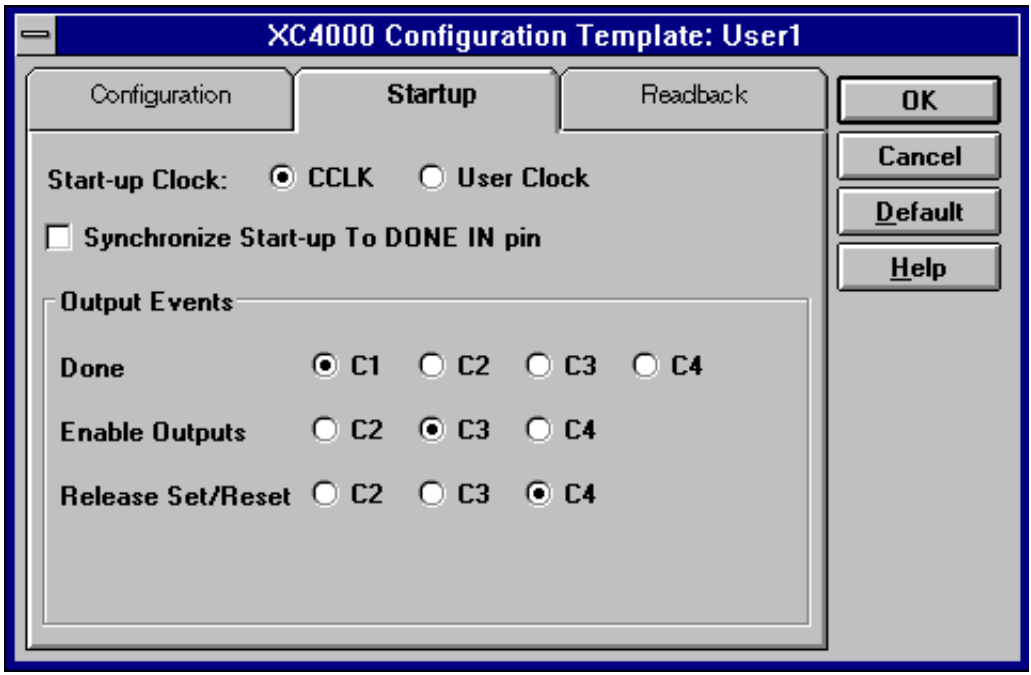


Figure 5-15 XC4000 Configuration Template Dialog Box, Startup Tab

Startup Clock

The startup sequence following the configuration of a device can be synchronized to either CCLK or a User Clock.

CCLK

An internal clock provided in the FPGA device.

User Clock

A user defined signal connected to the CLK pin of the Startup symbol.

Synchronize Start-up to DONE IN Pin

The start-up sequence of the XC4000 can be synchronized with the signal on the DONE pin. If this option is not selected, the start-up sequence begins as soon as the configuration memory is full. If this option is selected, the start-up sequence begins when the signal on the DONE pin goes high.

Output Events

There are three major output events which occur during a device startup:

- Done (DONE pin going high)
- Enable Outputs (device outputs no longer tristated)
- Release Set/Reset (Global Set/Reset signal deasserted)

Depending on the settings for Startup Clock and Synchronize Start-up to Done In pin, the output events can be set to occur as shown in Table 5-1.

Table 5-1 Output Events Options Matrix

	CCLK		User Clock	
	Sync	**No Sync**	**Sync**	**No Sync**
DONE	C1-C3	C1-C4	C1, U2	C1, U2-U4
Enable Outputs	C2, C3, DI, DI+1	C2-C4	U2, DI, DI+1, DI+2	U2-U4
Release Set/Reset	C2, C3, DI, DI+1	C2-C4	U2, DI, DI+1, DI+2	U2-U4

The definitions of the possible output events settings are as follows:

`C1` – first-Cclk rising edge after the length count is met

`C2` — second-Cclk rising edge after the length count is met

`C3` — third-Cclk rising edge after the length count is met

`C4` — fourth-Cclk rising edge after the length count is met

`U2` — second-valid-user-clock rising edge after C1 (first-Cclk rising edge after length count is met)

`U3` — third-valid-user-clock rising edge after C1 (first-Cclk rising edge after length count is met)

`U4` — fourth-valid-user-clock rising edge after C1 (first-Cclk rising edge after length count is met)

`DI` — when the DoneIn signal goes High

`DI+1` — first-Cclk or valid-user-clock rising edge, depending on the selection of start-upClk, after DoneIn goes High

`DI+2` — second-Cclk or valid-user-clock rising edge, depending on the selection of start-upClk, after DoneIn goes High

Dialog Box Options — Readback Tab

The Readback tab of the XC4000 Configuration Template dialog box is shown in Figure 5-16. The options are described below.

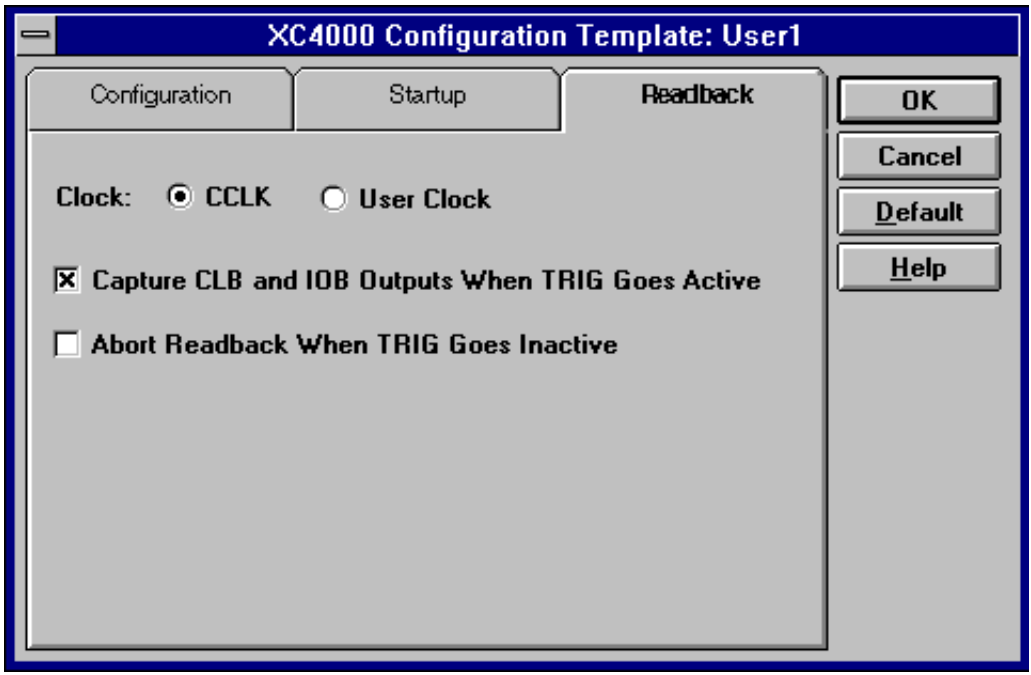


Figure 5-16 XC4000 Configuration Template Dialog Box, Readback Tab

Clock

The readback data can be clocked out by either CCLK or a User Clock.

CCLK

An internal clock provided in the FPGA device.

User Clock

A user defined signal connected to the CLK pin of the Readback symbol.

Capture CLB and IOB Outputs When TRIG Goes Active

Enables or disables the readback capability of the configuration bitstream. To enable this feature, select this option and include the Readback symbol in your design.

Abort Readback When TRIG Goes Inactive

Enables aborting the readback sequence. If this option is selected, the device terminates the readback sequence when it detects a high to low transition on the Trig pin of the Readback symbol.

Appendix A

Glossary

This appendix contains definitions and explanations for terms used in this manual.

asynchronous debug A debug mode that uses a free-running clock.

BIT file Synonym for a bitstream file.

bitstream (BIT file) A stream of data that contains location information for logic on a device, that is, the placement of CLBs, IOBs, TBUFs, pins, and routing elements. The bitstream also includes empty placeholders that are filled with the logical states sent by the device during a readback. Only the memory elements, such as flip-flops, RAMs, and CLB outputs, are mapped to these placeholders, because their contents are likely to change from one state to another. When downloaded to a device, a bitstream configures the logic of a device and programs the device so that the states of that device can be read back.

A bitstream file has a .bit extension.

block A group consisting of one or more logic functions.

bottom-up design Design methodology in which you complete the lowest level portion of your design first. Only after the low-level building blocks are complete do you finish higher- level hierarchical blocks in your design. This methodology is typically used with schematic capture programs.

BUFT Tristate buffer.

byte-wide PROM A PROM that supplies data one byte at a time.

CCLK pin The XChecker pin that provides the configuration clock for the device or devices during a download.

CLKI pin Clock input pin to XChecker. CLK1 provides an external clock to the Hardware Debugger so that in conjunction with the CLK0 pin, the Debugger can control the application of the external clock to the device being debugged.

CLKO pin XChecker clock output pin. CLK0 supplies the Hardware-Debugger-controlled clock to the device being debugged. The source of CLK0 is one of the following: CLKI, logic 1, logic 0, or the internal XChecker clock.

clock input path A path starting at either an input of the chip or at the output of a flip-flop, latch, or RAM, and ending at any clock pin on a flip-flip or latch enable. The clock input path time is the maximum time required for the signal to arrive at the flip-flop clock input. Clock input paths help to determine system-level design timing.

clock skew The difference between the time a clock signal arrives at the source flip-flop in a path and the time it arrives at the destination flip-flop. It is also referred to as clock delay.

clock-to-pad path (C2P) A path starting at the output of a flip-flop or latch and ending at the device output pin. It includes the clock-to-Q delay. The clock-to-pad path time is the maximum time required for the data to leave the source flip-flop, travel through logic and routing, and arrive at the output before the next clock edge occurs.

clock-to-setup path (C2S) A path starting at the output of a flip-flop or latch and ending at an input to another flip-flop, latch, or RAM, where that pin has a setup requirement before a clocking signal. It includes the clock-to-Q delay. The clock-to-setup path time is the maximum time required for the data to propagate through the source flip-flop, travel through the logic and routing, and arrive at the destination before the next clock edge occurs.

console log Record of the commands that you invoked during a session.

control panel An area in the Hardware Debugger that consists of buttons and text boxes for debugging purposes. The control panel is displayed after you select a debugging mode in the Hardware Debugger. The control panel commands offer an alternative to the Debug menu commands.

critical path A signal in a section of combinatorial logic that limits the speed of the logic. Storage elements begin and end a critical path, which may include I/O pads.

daisy chain A concatenation of more than one bitstream. A daisy chain can be used to program several FPGAs connected in a daisy chain board configuration.

debugging The process of reading back or probing the states of a device configured with a design to ensure that the device is behaving as expected.

DIN pin In an FPGA, the pin that loads a bitstream in serial mode. On the XChecker cable, it provides the bitstream data and connects to the DIN pin of the target FPGA.

downloading Configuring or programming a device by sending it bitstream data serially or in parallel mode.

D/P (XC2000/XC3000) pin Dual-function pin. As an input, it initiates a reconfiguration of a configured device. As an output, it signals the end of configuration.

DONE (XC4000) pin

Dual-function pin. As an input, it can be configured to delay the global logic initialization or the enabling of outputs. As an output, it indicates the completion of the configuration process.

EDIF Electronic Data Interchange Format, an industry standard file format for specifying a design netlist. It is generated by a third-party design-entry tool.

EXORmacs (Motorola) A PROM format supported by the Xilinx tools. Its maximum address is 16 777 216. This format supports PROM files of up to (8 x 16 777 216) = 134 217 728 bits.

external clock The system clock that XChecker uses from the target board during synchronous mode debugging. To use an external clock, connect the system clock to the XChecker cable using the CLKI pin and the XChecker clock to the FPGA device using the CLKO pin.

fast function block (FFB) A group of macrocells in an EPLD that can process very high-speed logic.

fit The process of putting logic from your design into physical macrocell locations in the EPLD. Routing is performed automatically, and because of the UIM architecture, all designs are routable.

GND pin Ground (0 volts).

group A collection of common signals to form a bus. In the case of a counter, for example, the different signals that produce the actual counter values can be combined to form an alias, or group.

guide file A previously placed and routed LCA file that can be used in a subsequent place and route operation.

HDL Hardware Description Language. The most common HDLs in use today are Verilog and VHDL. They describe designs in a technology-independent manner using a high level of abstraction.

HEX A simple text dump of the PROM data in HEX format. It has unlimited data capacity.

high-density function block (HDFB) A group of macrocells in an EPLD that can efficiently perform complex logic such as arithmetic operations.

hold time The time following a clock event during which the data input to a latch or flip-flop must remain stable in order to guarantee that the latched data is correct.

INIT pin Device pin indicating when a device is ready to receive configuration data after power-up.

instance One specific gate or hierarchical element in a design or netlist. The term “symbol” often describes instances in a schematic drawing. Instances are interconnected by pins and nets. Pins are ports through which connections are made from an instance to a net. A design that is flattened to the lowest level constituents is described using primitive instances.

internal XChecker clock The clock internal to XChecker that can be applied by the XChecker CLK0 pin to a device being debugged.

IOB (input/output block) A collection or grouping of basic elements that implement the input and output functions of an FPGA device.

loading direction The direction in which data is stored on your PROM. In the Up direction, the data is stored in ascending order. In the Down direction, the data is stored in descending order.

.ll file The logic allocation file, which indicates the bitstream position of storage elements such as latches, flip-flops, and IOB inputs and outputs. The Hardware Debugger uses this file to locate signal values inside a readback bitstream.

logic icon Graphical representation of a logic resource, such as a flip-flop, buffer, or register.

logic icons in transit Selected logic that is being moved from one location to another in the Floorplanner.

logic synthesis A process that starts from a high level of logic abstraction (typically Verilog or VHDL) and automatically creates a lower level of logic abstraction using a library containing primitives.

map The process of assigning a design's logic elements to the specific physical elements that actually implement logic functions in a device.

MCS-86 (Intel) A PROM format supported by the Xilinx tools. Its maximum address is 1 048 576. This format supports PROM files of up to (8 x 1 048 576) = 8 388 608 bits.

main window The background against which windows are displayed.

menu bar The area located at the top of the main window that provides access to the menus.

net A logical connection between two or more symbol instance pins. After routing, the abstract concept of a net is transformed to a physical connection called a wire.

number of clock cycles The number of clocks that have been applied between snapshots during synchronous mode debugging. This value is displayed between the snapshot numbers on the horizontal axis.

one-to-one logic In the context of Xilinx FPGA devices, the exact correspondence between the logic specified in the design entry phase and the logic implemented in the device. For example, if you draw

three inverters in your design, there are three corresponding inverters in the programmed device. This correspondence makes back-annotation of timing delays very straightforward and ensures that there are no differences between your original design and the finished device.

optimize The process of transforming a design to decrease its area or to increase its speed performance.

pad The physical bonding pad on an integrated circuit. All signals on a chip must enter and leave by way of a pad. Pads are connected to package pins in order for signals to enter or leave an integrated circuit package.

pad-to-pad path (P2P) A path starting at an input of the chip and ending at an output of the chip. The pad-to-pad path time is the maximum time required for the data to enter the chip, travel through logic and routing, and leave the chip. It is not controlled or affected by any clock signal.

pad-to-setup path (P2S) A path starting at an input of the chip and ending at an input to a flip-flop, latch, or RAM—wherever there is a setup time against a control signal. The pad-to-setup path time is the maximum time required for the data to enter the chip, travel through logic and routing, and arrive at the output before the clock or control signal arrives.

pin A symbol pin or package pin. A package pin is a physical connector on an integrated circuit package that carries signals into and out of an integrated circuit.

A symbol pin, also referred to as an instance pin, is the connection point of an instance to a net.

place The process of assigning physical device cell locations to the logic in a design.

placer The utility that maps logic from your design into specific locations in the target FPGA chip.

placer effort User-controlled parameter that balances run-time with placement efficiency for the Flow Engine.

primitive A logic element that directly corresponds, or maps, to a basic element.

probing The process of examining the states of an FPGA device.

PROG pin An XChecker pin that provides a reprogram pulse to XC4000 devices.

program The process of configuring an FPGA with a design.

PROM A programmable read-only memory.

PROM file A file consisting of one or more BIT files (bitstreams) formed into one or more datastreams. The file is formatted in one of three industry-standard formats: Intel MCS86 HEX, Tektronics TEKHEX, or Motorola EXORmacs. The PROM file includes headers that specify the length of the bitstreams, as well as all the framing and control information necessary to configure the FPGAs. It can be used only to program one or more devices.

PROM File Formatter The program used to format one or more bitstreams into an MC86, TEKHEX, EXORmacs, or HEX PROM file format.

ratsnest Lines that indicate connectivity between logic placed in the Floorplanner window.

RBT file A raw BIT format file; the ASCII version of the BIT file.

readback The process of reading the logic downloaded to an FPGA device back to the source. There are two types of readbacks:

- A readback of logic usually accompanied by a comparison check to verify that the design was downloaded in its entirety.
- A readback of the states stored in the device memory elements to ensure that the device is behaving as expected.

resource graphics Graphical representation of elements in the target FPGA Floorplan window, such as function generators, registers, tristate buffers in the CLB, and IOBs.

route The process of assigning logical nets to physical wire segments in the FPGA that interconnect logic cells.

router The utility that connects all appropriate pins to create the design's nets.

router effort User-controlled parameter that balances run-time with routing efficiency for the Flow Engine.

RD pin XChecker readback data pin.

RPM Relationally placed macro, which is a macro that defines the spatial relationship of the primitives that constitute its logic.

RST pin An XChecker pin that can be driven Low after configuration to reset the target FPGA internal latches and flip-flops.

RT pin The XChecker readback trigger pin.

schematic A hierarchical drawing representing a design in terms of user and library components.

script A series of commands that automatically execute a complex operation such as the steps in a design flow.

SDF Standard Delay Format, which is an industry standard file format for specifying timing information. It is usually used for simulation.

selecting logic In the Floorplanner, the process of using the mouse to choose logic in either the Design window or the Floorplan window for placement, movement, or processing.

serial PROM A PROM that is read one bit at a time.

setup time The time prior to a clock event during which the data input to a latch or flip-flop must remain stable in order to guarantee that the latched data is correct.

snapshot An individual device state that is captured by the Hardware Debugger.

states The values stored in the memory elements (flip-flops, RAMs, CLB outputs, and IOBs) of a device that together represent the state of that device for a particular snapshot. To each state there corresponds a specific set of logical values. Contrast this term with the logic locations of a device.

static timing analysis A point-to-point delay analysis of a design network.

status bar An area located at the bottom of a window that provides information about the commands that you are about to select or that are being processed.

synchronous debug A debug mode in which you use the XChecker cable to have full control of the clock.

synthesis See logic synthesis.

TCK pin An XChecker pin reserved for future use.

TDI pin An XChecker pin reserved for future use.

TEKHEX (Tektronix) A PROM format supported by Xilinx. Its maximum address is 65 536. This format supports PROM files of up to (8 x 65 536) = 524 288 bits.

time A process that takes the routed nets in the design and calculates the delays associated with each.

timing specifications Definition of the maximum allowable delay on any given set of paths in a design. Timing specifications are entered on the schematic with the XACT-Performance utility.

TMS pin An XChecker pin reserved for future use.

toolbar A field located under the menu bar at the top of a window. It contains a series of icons that you click on to execute some of the most commonly used commands. These icons are an alternative to the menu commands.

top-down design A process that starts a design with the highest level of abstraction and gradually designs underlying blocks until the complete design is implemented in the target technology. Top-down design is often technology-independent at the highest levels of design abstraction.

TRIG pin An XChecker external trigger pin that causes the Hardware Debugger to initiate a readback of the device being debugged.

trigger An external signal that tells the Hardware Debugger to start the readback operation. It applies the clock to the bitstream.

TTY Textual command line interface.

universal interconnect matrix (UIM) The routing matrix for EPLD devices. This fully populated switching matrix allows any output to be routed to any input, guaranteeing 100% routability of all designs. The UIM can also function as a very wide AND gate, which can allow more logic to be placed in macrocells.

VCC pin Power (5 volts).

verification The process of reading back the configuration data of a device and comparing it to the original design to ensure that all of the design was correctly received by the device.

Verilog Commonly used Hardware Description Language (HDL). It is a hardware description language that can be used to model a digital system at many levels of abstraction ranging from the algorithmic level to the gate level.

VHDL An acronym for VHSIC Hardware Description Language (VHSIC is an acronym for Very High-Speed Integrated Circuits). It is a hardware description language that can be used to model a digital system at many levels of abstraction ranging from the algorithmic level to the gate level.

waveform The graphical representation of one or more snapshots. Each snapshot represents a particular state of the memory elements of the device.

WIR file An intermediate design file that the Viewlogic design tools generate.

workspace In the PROM File Formatter, a frame and an empty data stream. When you add files into the data stream, the horizontal arrows indicate the concatenation of files.

XB Xilinx binary file. This internal file format is used by the Xilinx software to describe a design.

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4,855,619; 4,855,669; 4,902,910; 4,940,909; 4,967,107; 5,012,135; 5,023,606; 5,028,821; 5,047,710; 5,068,603; 5,140,193; 5,148,390; 5,155,432; 5,166,858; 5,224,056; 5,243,238; 5,245,277; 5,267,187; 5,291,079; 5,295,090; 5,302,866; 5,319,252; 5,319,254; 5,321,704; 5,329,174; 5,329,181; 5,331,220; 5,331,226; 5,332,929; 5,337,255; 5,343,406; 5,349,248; 5,349,249; 5,349,250; 5,349,691; 5,357,153; 5,360,747; 5,361,229; 5,362,999; 5,365,125; 5,367,207; 5,386,154; 5,394,104; 5,399,924; 5,399,925; 5,410,189; 5,410,194; 5,414,377; RE 34,363, RE 34,444, and RE 34,808. Other U.S. and foreign patents pending. Xilinx, Inc. does not represent that devices shown or products described herein are free from patent infringement or from any other third party right. Xilinx assumes no obligation to correct any errors contained herein or to advise any user of this text of any correction if such be made. Xilinx will not assume any liability for the accuracy or correctness of any engineering or software support or assistance provided to a user.

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