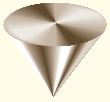
XILINX®

ONLINE

FLOORPLANNER REFERENCE/USER GUIDE

TABLE OF CONTENTS

INDEX



GO TO OTHER BOOKS

XACT™ STEP

0401311

Contents

Chapter 4 Using the Floorplanner

Appendix A Glossary

Chapter 1

Introduction

This chapter describes the graphical interface and the important features and capabilities of the Xilinx Floorplanner.

The Floorplanner is a graphical placement tool that gives you control over placing a design into a target FPGA using a “drag and drop” paradigm with the mouse pointer.

The Floorplanner displays a hierarchical representation of the design in the Design window using hierarchy structure lines and colors to distinguish the different hierarchical levels. The Floorplan window displays the floorplan of the target device into which you place logic from the hierarchy. Refer to Figure 1-1, which shows the windows on the PC version.

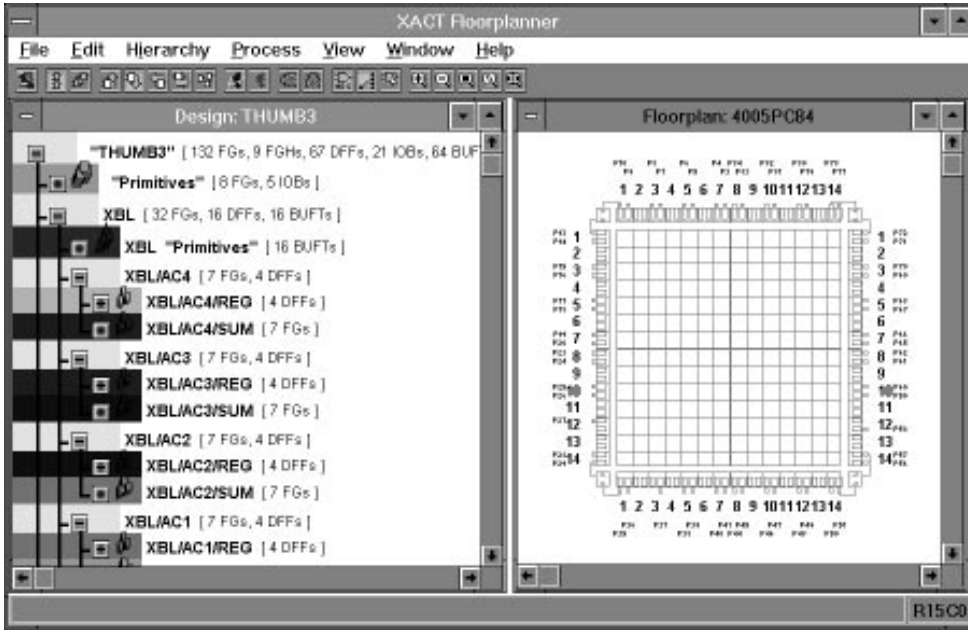


Figure 1-1 Design and Floorplan Windows

Logic symbols represent each level of hierarchy in the Design window. You can modify that hierarchy in the Floorplanner without changing the original design.

You use the mouse to select the logic from the Design window and place it in the FPGA represented in the Floorplan window.

Alternatively, you can automatically place, or place and route design logic in the FPGA by invoking PPR from the Floorplanner, or from the Design Manager.

Why Floorplan?

Floorplanning is an optional methodology to help you improve performance and density of a fully, automatically placed and routed design. Floorplanning is particularly useful on structured designs

and data path logic. With the Floorplanner, you see where to place logic in the floorplan for optimal results, placing data paths exactly at the desired location on the die.

With the Floorplanner, you can floorplan your design prior to or after running PPR. In an iterative design flow, you floorplan and place and route, interactively. You can modify the logic placement in the Floorplan window as often as necessary to achieve your design goals. You can save the iterations of your floorplanned design to use later as a constraints file for PPR.

Features of the Floorplanner

The Floorplanner provides an easy-to-use graphical interface that offers the following features.

- Interacts at a high level of the design hierarchy, as well as with low-level elements such as, I/Os, function generators, tristate buffers, flip-flops, and RAM/ROM.
- Captures and imposes complex patterns including sorting order, which is useful for repetitive logic structures such as interleaved buses
- Automatically distributes logic into columns or rows
- Uses dynamic rubberbanding to show the ratsnest connections
- Uses a Congestion Map to show potential routing congestion areas
- Finds logic or nets by name or connectivity
- Contains a direct interface to placement and routing software
- Permits design hierarchy rearrangement to simplify floorplanning
- Groups logic by connectivity or function
- Identifies placement problems in the Floorplan window
- Provides online help
- Includes an interactive, online tutorial that you run on the PC.

Supported Architectures

The Floorplanner supports all Xilinx architectures in the XC3000A, XC3100, XC4000, and XC5200 device families.

The Floorplanner does not support the XC3000, XC6200, XC7000 or XC8100 device families.

Online Help and Tutorial

The Floorplanner contains online help that gives you quick access to necessary information about the interface, dialog boxes, and floorplanning procedures. You can access online help from any Floorplanner window using the Help menu and from any dialog box that contains a Help button.

The Floorplanner software also contains an online interactive tutorial that you should examine before actually using the Floorplanner. This tutorial explains important floorplanning tasks with descriptive overviews and step-by-step procedures. It combines hands-on tasks with automated procedures to familize you with the tool's operation.

Input Files

The Floorplanner can read in the following input files:

- MAP

  This file is generated using the XMake -X option on an XNF file. It is the only required file for the Floorplanner.

- FPN

  This optional file is a snapshot that describes the state of the floorplanner for the design when you use the Save command.

- LCA

  This optional file is generated by PPR. You can read in an LCA file using the Read Placed Design command.

- PM

  This file is read in for the XC5200 family when you use the Read Placed Design command.

- CST

  This optional constraints file contains floorplanned logic placement information about the design. This file, which you can create with a text editor, is read in by the Read Constraints command.

Output Files

The Floorplanner generates the following output files:

- CST

  This is a constraints file that you generate on the floorplanned logic using the Write Constraints or Save commands.

- FPN

  This optional file is a snapshot that describes a previous floorplan for the design when you use the Save command.

- LOG

  This file contains relevant information about your floorplanning efforts, including place and route results and warning and error messages.

- MAP

  This file is required input for PPR for the XC3000A and XC3100 device families.

- XTF

  This file is required input for PPR for the XC4000, and XC5200 device families.

Design Flow

This chapter describes the four unique design flows that you can use with the Floorplanner to implement your design in a Xilinx FPGA. Accompanying each design flow is a comprehensive flow chart that indicates the programs you use, the input files required, and output files that are generated.

For HDL designs, you can use the Floorplanner to specify areas in the floorplan in which you want to place hierarchical groups of logic, such as state machines and blocks.

Xilinx strongly recommends that you read the *High-Density Design Guide* application note and the *HDL Synthesis for FPGAs Design Guide* before attempting to floorplan your HDL designs. Those documents explain HDL-specific design issues and understanding them will make floorplanning your HDL designs easier and more effective.

The design flows in this chapter present a general picture of where the Floorplanner fits in the Xilinx design flow; in some instances the descriptions of the design flows are more relevant to designers using schematic capture tools than to designers using HDL.

Floorplanning Prior to PPR

The first design flow describes how to floorplan your design before using PPR to place and route it. In this flow, you enter your design using either a schematic capture tool or HDL. Use the Floorplanner to define placement constraints by manually placing selected logic into the resources of the target device. Next, run PPR to fit the design into the target FPGA. Refer to the design flow in Figure 2-1.

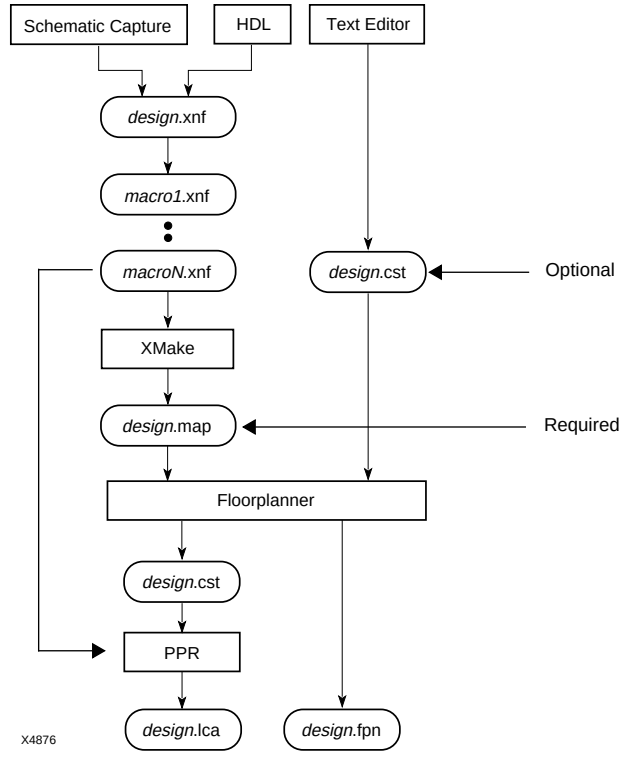


Figure 2-1 Floorplan First Design Flow

Note: Synopsys creates an XNF file with an .sxnf extension. For more information, refer to the *Synopsys (XSI) for FGPAs Interface/Tutorial Guide*.

Place and Route, Then Floorplan

In this design flow, you place and route your design before using the Floorplanner. You enter your design using either a schematic capture tool or HDL. Next, run PPR to place and route the design in a target FPGA device. To resolve any unrouted nets or to improve performance, use the Floorplanner to adjust placement. Finally, run PPR with the newly generated constraints file to produce better results. Refer to the design flow in Figure 2-2.

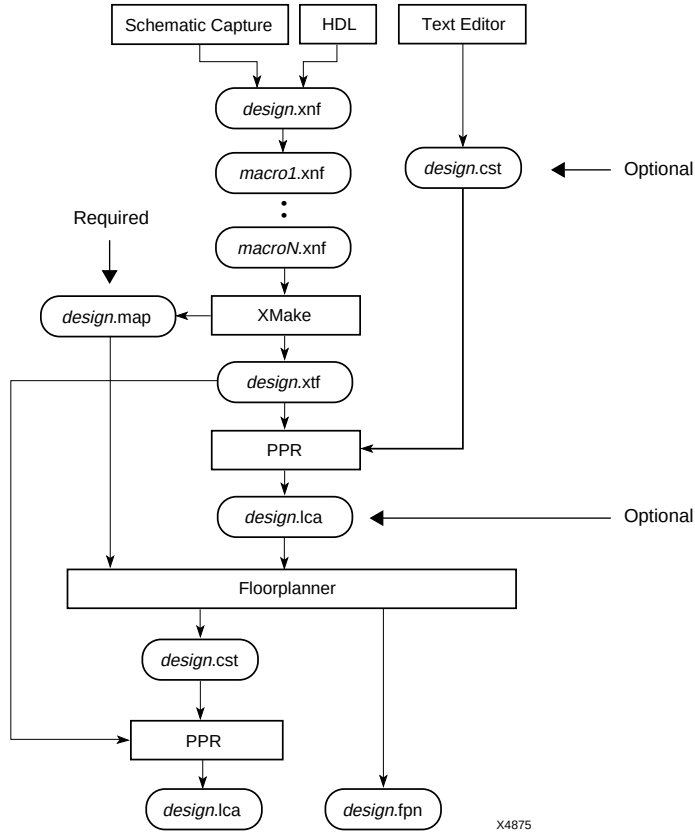


Figure 2-2 PPR Before Floorplanning Design Flow

Note: HDL users should refer to the *High-Density Design Guide* application note for information about improving the performance of their designs.

Incremental Design Changes

In this scenario, you make changes to the schematic of a design that has been previously implemented in an FPGA, with or without floorplanning. You must re-implement the design into the target device while making only minimal changes to the previous implementation. These changes could be one or more of the following:

- Adding logic
- Removing logic
- Changing existing logic

You can use a guide file for incremental design changes. Refer to the design flow in Figure 2-3.

Optionally, if you used the Floorplanner to floorplan the original design, use the Floorplanner now to correlate the logic in that design with the new changes, and adjust the constraints information accordingly.

Next, use the Floorplanner to place the new or changed logic, then use PPR to route the design again. PPR uses the existing LCA file as a guide to routing the unchanged logic in the design.

Note: For HDL users only. Incremental design change is more complex with HDL designs because the synthesis tools change symbol names whenever the compilation method changes. Refer to the *High-Density Design Guide* application note and the *HDL Synthesis for FPGAs Design Guide* for specific information about structuring your hierarchy for use with the Floorplanner.

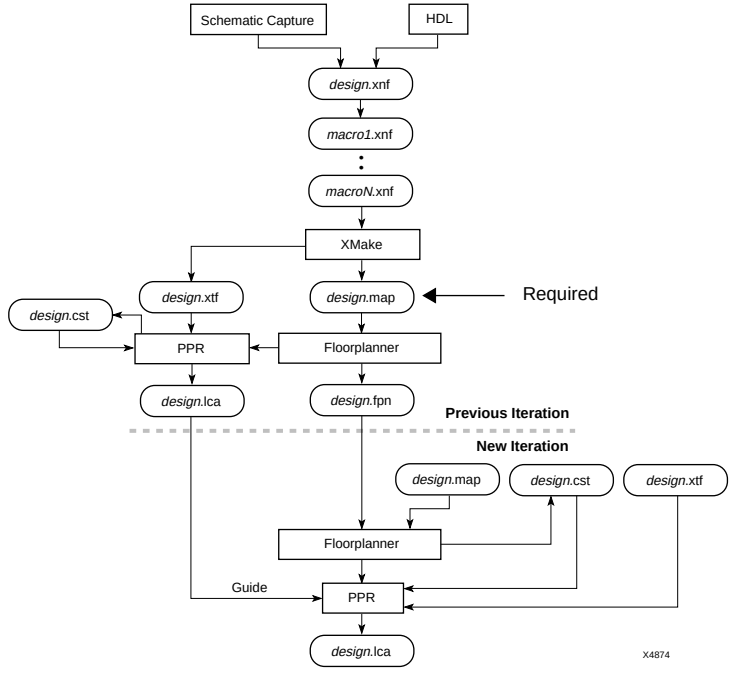


Figure 2-3 Incremental Design Change Design Flow

Note: Synopsys creates an XNF file with an .sxnf extension. For more information refer to the *Synopsys (XSI) for FPGAs Interface/Tutorial Guide*.

Iterative Floorplanning

In iterative floorplanning, you enter the design using a schematic capture tool or HDL. Next, you use the Floorplanner to constrain just a portion of the design. Then, run PPR from the Floorplanner to place and route that portion of the design into the target FPGA.

Select another portion of the design to constrain. Run PPR again with the Guide option. This option uses the previous placement as a guide while placing and routing this new portion of the design.

Repeat this Floorplanner-to-PPR loop until you have implemented the entire design into the target FPGA.

Note: Once you achieve a reasonable placement, Xilinx recommends that you reroute the entire design using PPR. This method allows PPR to consider the timing relationships of the entire design during routing. Use the constraints file that the Floorplanner generates to lock down the design placement. Refer to the design flow in Figure 2-4.

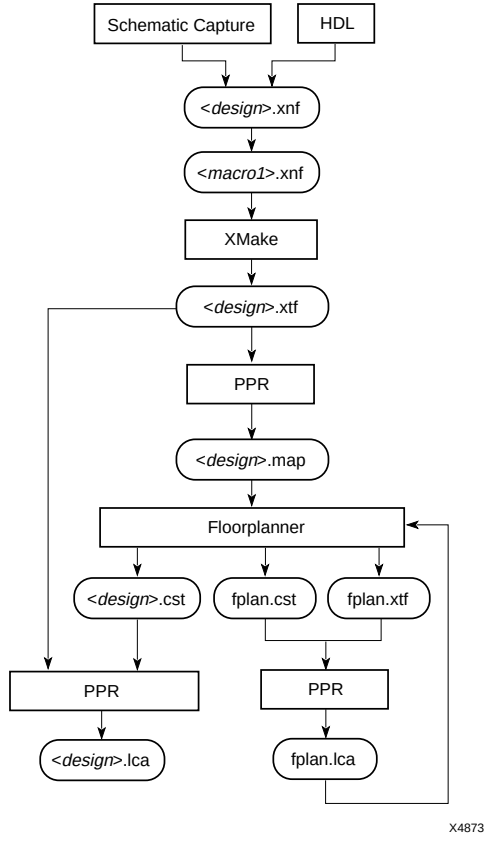


Figure 2-4 Iterative Floorplanning Design Flow

Chapter 3

Getting Started

This chapter describes how to invoke and exit the Floorplanner. It also explains the basic elements and operations of the Floorplanner interface. The last section of this chapter describes how to use the Floorplanner's online help.

Note: Xilinx recommends that you view the interactive, online tutorial before actually using the Floorplanner on your design. This is a PC-Windows based tutorial that provides a clear overview of the tool, and provides details about several basic floorplanning operations.

Running the Floorplanner

You can run the Floorplanner on the PC under the Windows-based Design Manager, or on Unix-based workstations under XDM. You can input either an HDL-based design or a schematic-based design.

This section describes the steps required to prepare your design for use in the Floorplanner.

From the Design Manager

Figure 3-1 shows the Design Manager screen from which you can launch the Floorplanner.

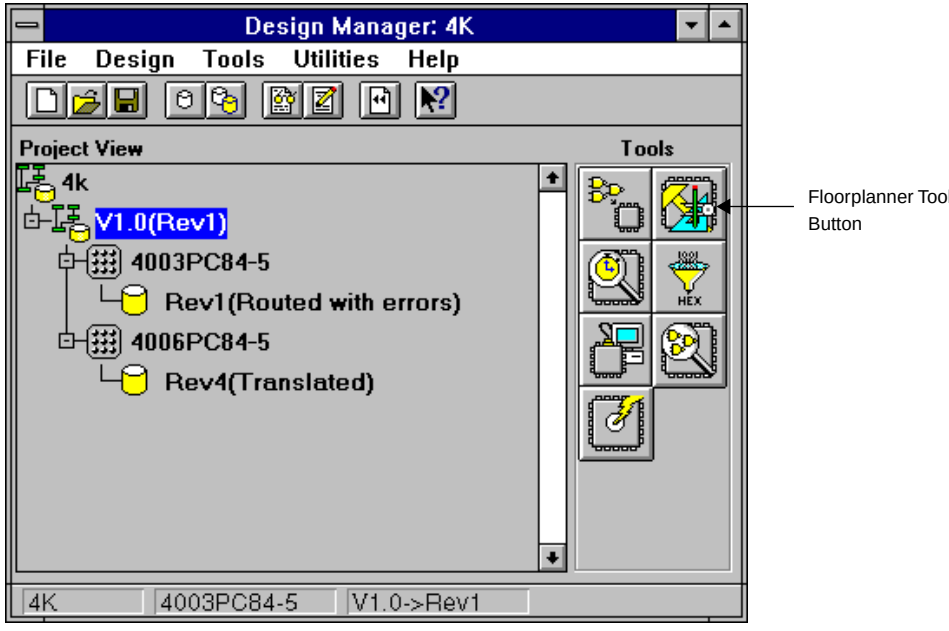


Figure 3-1 Design Manager Window

1. You can invoke the Floorplanner from the Design Manager in either of two ways.

- Select the Floorplanner command from the Tools menu.
- Click on the Floorplanner toolbox button.

Refer to the *Design Manager/Flow Engine Reference/User Guide* for more details about invoking the Floorplanner from the Design Manager.

From XDM (Workstations)

Figure 3-2 shows the XDM screen for workstations.

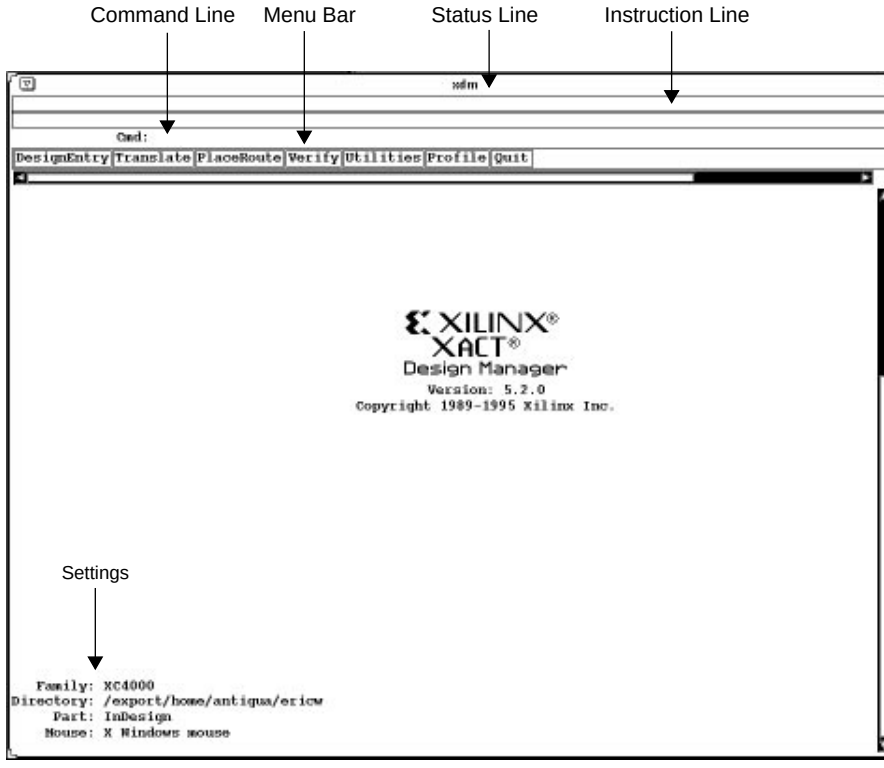


Figure 3-2 XDM Opening Screen (Workstation)

To prepare your design for use with the Floorplanner, perform these steps:

1. Invoke XDM.
2. Select XMake from the Translate menu.

   The XMAKE_popup dialog box displays a list of options.
3. If you have a schematic or HDL-based design, click the Done button.

   The Floorplanner searches for the design.

4. Select the designthat you want to prepare for the Floorplanner from the list that appears in the dialog box.

   This step causes the XMake pop_up menu to appear.

5. Select the Prep for Floorplan option from the menu.
6. Click the Done button.

If you have an XNF file that you are using as input, follow these steps:

1. From the XMake pop_up menu, select the -X option (Use XNF files only) from the dialog box.
2. Click the Done button.

   The dialog box displays a list of XNF files from which to choose.

3. Select the appropriate XNF file.
4. Click the Done button.

   The dialog box prompts you to select a target file for XMake.

5. Select Prep for Floorplanner from the dialog box.
6. Click the Done button.
7. To invoke the Floorplanner, type in the following command at the prompt:

   `fplan`

Exiting the Floorplanner

To exit the Floorplanner, follow these steps:

1. Select the Exit command from the File menu.

   If you have floorplanned any logic, a dialog box displays and prompts you to save changes to the current floorplan.

2. Click the appropriate button.

   If you click the Yes button, the Floorplanner writes out an FPN file that is a snapshot of floorplanned logic and the Floorplanner environment.

   If you click the No button, the Floorplanner simply quits without making changes to the design that had been read in.

If you click the Cancel button, the dialog box closes and you can continue with the current floorplan session.

Closing the Floorplanner

To close the Floorplanner, follow these steps:

1. Select the Close command from the File menu in either the Design window or Floorplan window.

   If you have only read in a design, and not made any changes in the Design or Floorplan windows, the Floorplanner simply closes those windows and displays the Task window. From this window you can open another design in the Floorplanner.

   If you have made any changes to the design in the Floorplanner, a dialog box prompts you to save those changes.

2. Click the appropriate button.

   If you click the Yes button, the Floorplanner writes out an FPN file that is a snapshot of floorplanned logic and the Floorplanner environment.

   If you click the No button, the Floorplanner closes without making changes to the design that had been read in.

   If you click the Cancel button, the dialog box closes and you can continue with the current floorplan session.

Floorplanner Interface

The Floorplanner interface consists of three windows; the initial XACT-Floorplanner window(Task window), Design window and the Floorplan window, pull-down menus, dialog boxes, and toolbar.

The Floorplanner uses a graphical user interface with pull-down menus that contain all of the necessary commands to floorplan your design. The menus contain many commands that open dialog boxes, from which you can select various options and parameters for that command. Other commands act immediately on the selected logic.

Window operations, such as opening, closing, sizing, and moving are consistent with the window environment of your particular platform.

Toolbar

The toolbar is a feature on the Floorplanner that gives you pushbutton access to many floorplanning tasks. You can zoom in and out of the Floorplan window and enable the display of resource graphics, labels, and ratsnest lines.

It also gives you pushbutton access to changing the distribute mode and allocation direction for placing logic symbols. The allocation direction function is only available from the toolbar.

You can use the toolbar buttons shown in Figure 3-3 in lieu of the pull-down menus to perform several basic operations in the Floorplan window. For a complete description of the toolbar buttons, refer to the "Menu Command Reference" chapter.

Figure 3-3 Floorplan Window Toolbar

Mouse

The mouse is integral to many floorplanning operations. Use it to select and place logic, access commands from the menus, and perform various window operations. Selecting logic in the Floorplanner windows is a "drag-and-drop" paradigm using the mouse pointer. You select logic from the hierarchical design in the Design window by placing the pointer over the symbol icon, or macro name and clicking the left mouse button. Then you drag the pointer to the Floorplan window (a ghost image of the selected logic moves with the pointer) and release the mouse button to drop the logic at the pointer's location in the window.

Multiple logic selections in the Floorplanner follow these windows standards:

- To make multiple consecutive selections, click the left mouse button when the pointer is over the item, then press and hold down the Shift key, move the pointer to the last item, then click the left mouse button.
- To make multiple, nonconsecutive selections, move the mouse pointer over each item, then while holding down the Control (Ctrl) key, click the left mouse button.

Keyboard

The Floorplanner uses the keyboard function keys that are mapped to specific menu commands and Floorplanner functions for ease of use. Table 3-1 lists the keyboard shortcuts for the Floorplanner and shows the related toolbar button, if any. You should exercise care when using the keyboard shortcuts.

Table 3-1 Floorplanner Keyboard Shortcuts

Function Key	Menu Command/Function	Toolbar Button
F1	Help → Contents	None
F2	View → Resources	None
F3	Hierarchy → Group	None
F4	Edit → Colors	None
F5	View → Refresh	None
F6	View → Zoom to Selected	
F7	View → Zoom In	
F8	View → Zoom Out	
F9	View → Zoom to Box	
F10	Change focus to the menu bar	None
F11	View → Zoom Full View	

Function Key	Menu Command/Function	Toolbar Button
F12	View → Ratsnest	None
Del	Floorplan → Remove	None
Esc	Cancel current opertion	None

The Windows

The Floorplanner has three windows; XACT-Floorplanner (Task), Design, and Floorplan. Descriptions of the three windows follow.

Task Window

When you invoke the Floorplanner, the Task window, shown in Figure 3-4 is the first Floorplanner window to display on your monitor. From the File menu, you use the Open command to load a design file into the Floorplanner and begin floorplanning. The Help menu allows you use the online help. On PCs, you can launch the online interactive tutorial from the Help menu and use the Window menu to arrange windows and window icons.

Note: The online tutorial is shipped with the Floorplanner software, but runs only on the PC.

Figure 3-4 XACT-Floorplanner Task Window

When you load a file using the Open command, the Floorplanner displays a small pop-up window that indicates the device part type designated for the target device and shows the progress of the design

being loaded. When the Floorplanner loads in the display, this overlay window disappears and is replaced by the Design and Floorplan windows.

XACT-Floorplanner Window (PCs only)

This window , shown in Figure 3-5 appears only in the PC version of the Floorplanner and frames the Design and Floorplan windows.

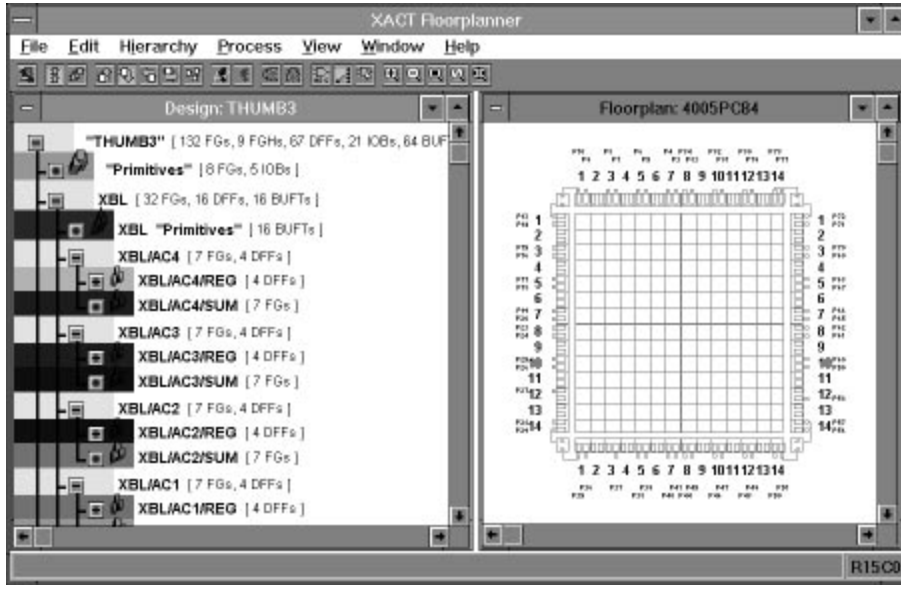


Figure 3-5 XACT-Floorplanner Window (PCs)

Design Window

The Floorplanner generates a hierarchical representation from the MAP file input. The Design window, shown in Figure 3-6, displays a fully expandable and annotated hierarchy.

The design hierarchy is a MAP file that was created from the schematic file or high-levelHD descriptions of the design. The header line indicates the name of the design that is currently loaded.

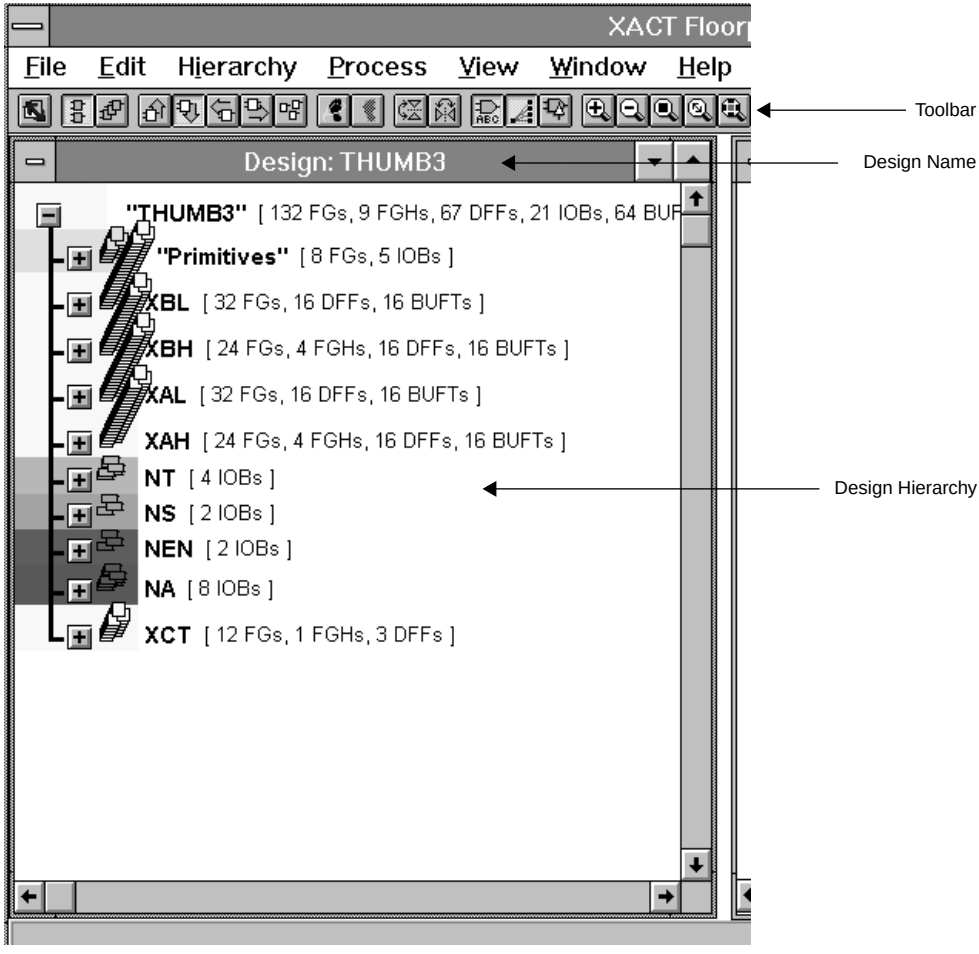


Figure 3-6 Design Window (PCs)

Hierarchy Display

The Floorplanner uses colors in the hierarchy display to distinguish the levels in the hierarchy, which are annotated with the instance name from the MAP file. Hierarchy structure lines are black lines that traverse the colored areas and show the hierarchy of each macro.

Each macro has a gray box with a minus sign, “–”, or a plus sign, “+”. The “–” indicates that the macro is expanded to show the next lower level of hierarchy. The “+” indicates that the macro is collapsed, and that lower levels of hierarchy exist for that macro.

Selecting Logic

When you place the mouse pointer over a macro instance name or its logic symbol icon (in the Design window) and click the left mouse button, you select that logic. The Floorplanner displays selected logic in in the Design window in reverse video. (If you keep Flashing enabled, the selected logic in the Floorplan window flashes.) When you select a macro, you also select all the sub-hierarchy in that macro. When you select logic at some lower level, the Floorplanner draws a rectangular box around all associated higher levels of hierarchy. Figure 3-7 shows an example. The $7I586/REG primitive macro is the selected logic, as indicated by the reverse video. The macros hpmvsel and $7I586/REG are the higher-level associated logic, as indicated by the box around those macro names.

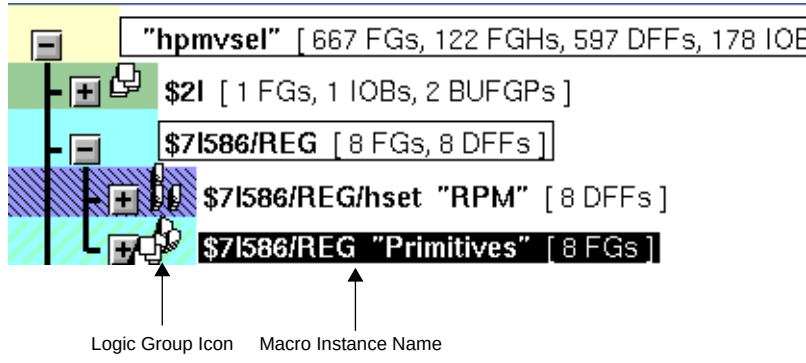


Figure 3-7 Selected Logic in the Design Window

Expanding and Collapsing Macros

Click the left mouse button on the Expand/Collapse button when it displays the "+" sign to expand a macro and display the next level of hierarchy. The logic elements that comprise each macro appear as an icon between the Expand/Collapse button and the instance name. Figure 3-8 shows a sample hierarchy.

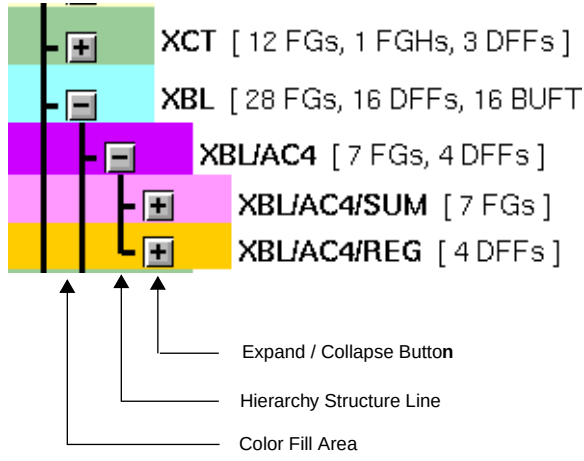


Figure 3-8 Hierarchical Macro Display in the Design Window

Hierarchical Macro Annotation

Each macro in the design hierarchy contains the instance name, macro or source name, and symbol counts. The symbol count is the number of FPGA resources required to accommodate that macro in the floorplan. Groups that you create with either the Group or Group By commands contain a non-hierarchical name and symbol count.

In the case of the XC4000 family, the FPGA resources are categorized by type, such as FG, function generator; BUFTs, tristate buffers; DFFs, registers; IOBs, input/output pads, RAM/ROM, and related logic. Figure 3-9 labels the important parts of a hierarchical macro.

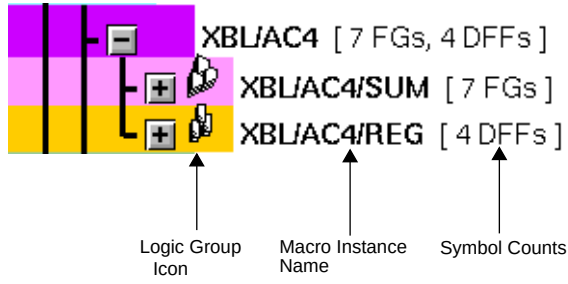


Figure 3-9 Hierarchical Macro Annotation

Symbol Annotation

The symbol line represents the lowest hierarchy of any macro. It represents a single resource requirement of the design. The symbol line contains a logic group icon, the symbol name, symbol type, and the list of pin:net pairs. Figure 3-10 shows one of symbol instances of the expanded macro, XBL/AC4/SUM (shown in Figure 3-9). It labels the important parts of the symbol line.

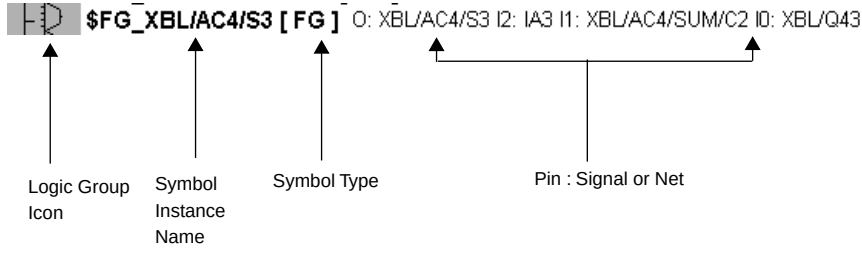


Figure 3-10 Symbol Annotation Explanation

In Figure 3-10 the logic icon that is shown represents a single 4-input function generator (FG) named $FG_XBL/AC4/S3; its output connects to net XBL/AC4/S3; its inputs connect to the nets IA3, XBL/AC4/SUM/C2, and XBH/Q43.

The symbol name is the corresponding symbol in the source netlist. For function generators or CLBs, it is a name that the mapping software provides (XNFMAP for the XC3000 family; PPR for the

XC4000, and XC5300 device families). For other symbols, it is the name in the schematic that either you or the schematic entry tool chooses.

The symbol type refers to the type of resource that the symbol requires. Examples of symbol types are DFF (D-type flip-flop), IOB (Input/Output buffer), CLB (configurable logic block), FG (function generator), and BUFT (tristate buffer).

Floorplan Window

The Floorplan window displays the die for a selected part type, such as XC4005PC84. This window, shown in Figure 3-11 is a scrollable, scalable view of a resource map of the device that is specified in the design.

You floorplan by dragging selected logic from the Design window and dropping it into this window.

The status bar is at the bottom of the window. In this area, the Floorplanner displays various resource information. To the far right it displays current row and column coordinates when the mouse pointer is in the Floorplan window. When you enable the resource display with the Resources command from the View menu or Resource Graphics toolbar button, the status bar identifies the logic resource with the row and column number.

The status bar also provides information about the toolbar buttons. When the toolbar is enabled and you move the mouse pointer over a toolbar button, the Floorplanner displays the name of that button and its function. When you use the Find Nets and Find Logic commands, the status bar displays the number of found nets or found logic.

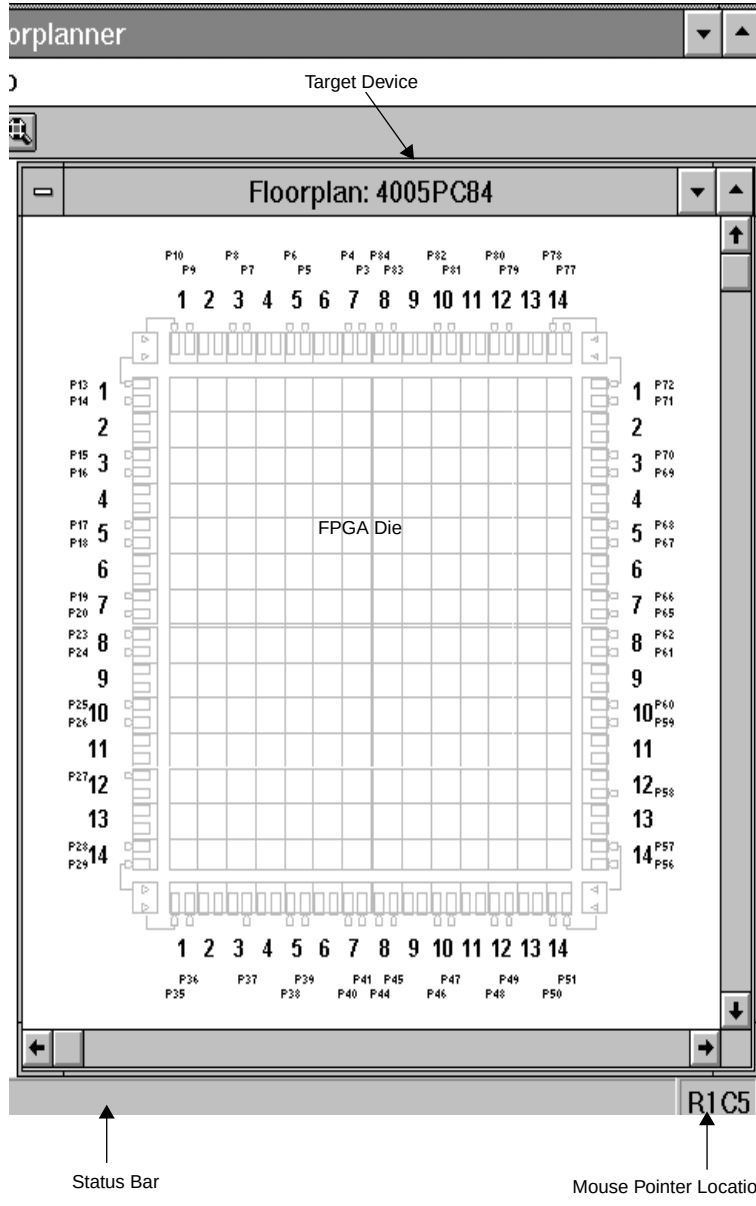


Figure 3-11 Floorplan Window (PCs)

Resource Graphics

Each device family architecture has specific resources on the die. Optionally, you can display these resources using the Resources command from the View menu or the Resource Graphics toolbar button. For example the resource graphics for the XC4000 family include I/Os, function generators, registers, RAM/ROM, and BUFTs in the CLBs . With this feature, you control the view of the logic and available device resources. The fewer resources you display in the window, the faster the screen refreshes.

In the XC4000 family devices, flip-flops display as rectangles, function generators as trapezoids, and BUFTs as triangles. Figure 3-12 shows an example of the resource graphics available in a quadrant of the Floorplan window.

Note: The global buffers have a pair of dedicated I/O pads that can also connect to other logic. The lines in the floorplan die show which I/O pad is dedicated to that buffer.

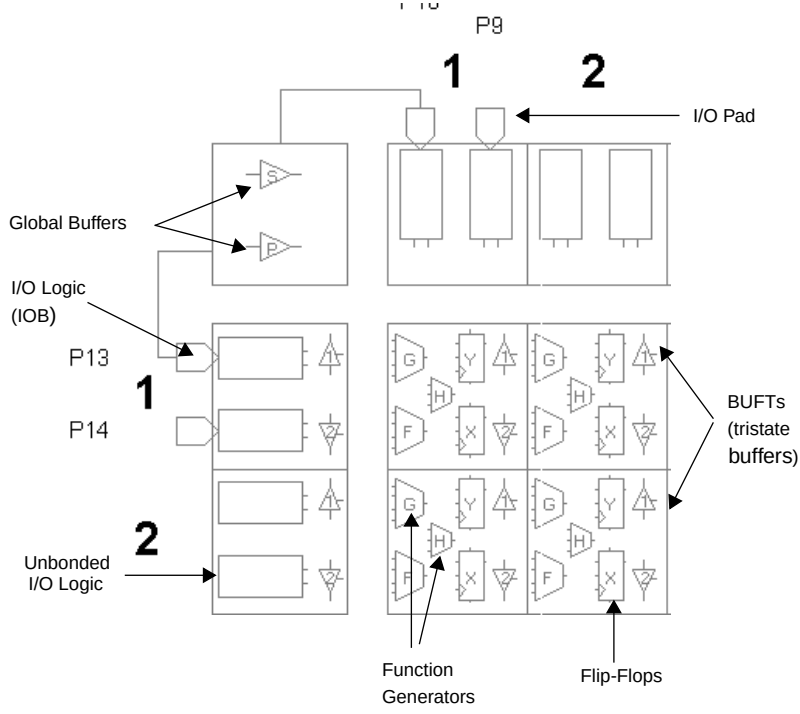


Figure 3-12 Resource Graphics for a XC4000 Device

Dialog Boxes

The Floorplanner has many commands that, when invoked, open dialog boxes that contain default settings for command execution. These types of commands have an ellipsis (...) after the command name.

The dialog boxes are composed of edit boxes inwhich you can type in information, such as a different path name; list boxes, which lists design information, such as net names; and buttons, which allow you browse information and easily change the way a command will function.

Many dialog boxes contain a Help button. Clicking on this button opens the online help to the associated command description and provides access to the entire online help facility.

Chapter 4 provides a detailed description of the Floorplanner dialog boxes in the command descriptions.

Online Help

The Floorplanner provides online help that gives you quick access to information that explains the use of dialog boxes, procedural tasks, and a glossary.

You can access the online help from several locations in the Floorplanner.

- The Contents command from the Help menu in any Floorplanner window (Task, Design, or Floorplan) opens the Contents page, which is the top online help screen. From here you have access to all of the online help information about the Floorplanner.
- The Help button on any dialog box opens the online help for that command and describes the fields and buttons that comprise that dialog box. From here, you can navigate to any part of the online help.
- The F1 key, when pressed, opens the Contents page of the online help.

Using the Floorplanner

This chapter provides step-by-step instructions for performing the important floorplanning tasks.

These procedures are presented in sequential order; however, not every task that can be performed is documented in this chapter. Floorplanning a design may require you to repeat some procedures several times. Consult the design flows in Chapter 2 to aid your floorplanning efforts.

Note: Xilinx recommends that you view the interactive online tutorial to get an overview of the Floorplanner.

Preparing a Design to Floorplan

To prepare your design for use with the Floorplanner, perform these steps:

1. Invoke XDM.
2. Select XMake from the Translate menu.

   The XMAKE_popup dialog box displays a list of options.
3. If you have a schematic file or HDL-based design, click the Done button.

   The Floorplanner searches for the design.
4. Select the design from the list that appears in the dialog box.

   This step causes the XMake pop_up menu to appear.
5. Select the Prep for Floorplan option from the menu.
6. Click the Done button.

If you have an XNF file that you are using as input, follow these steps:

1. From the XMake pop_up menu, select the -X option (Use XNF files only) from the dialog box.
2. Click the Done button.

   The dialog box displays a list of XNF files from which to choose.
3. Select the appropriate XNF file.
4. Click the Done button.

   The dialog box prompts you to select a target file for XMake.
5. Select Prep for Floorplanner from the dialog box.
6. Click the Done button.
7. To invoke the Floorplanner, type in the following command at the prompt:

   `fplan`

Opening a File

To load a design file in the Floorplanner, follow these steps:

1. Choose the Open command from the File menu.

   This command opens the standard File Open dialog box where you specify the MAP file to load. In this dialog box, you can also change directories if the desired MAP file is in a directory other than the current directory.
2. Scroll the File Name (for PCs) or Files (for workstations) list box until you find the desired design file in the list.
3. Double-click on the design file name or click OK to open a Design window and a Floorplan window that contains the specified MAP file.

   When you load in a MAP file, the Floorplanner reads the file, loads the correct device (part type), opens the Design window with a hierarchical design, and opens the Floorplan window with the correct FPGA die.

Note: If an FPN file exists in the current directory and it is newer than

the MAP file, then the Floorplanner reads in the FPN file; otherwise, it reads in the MAP and a constraints file, if one exists.

Saving a File

To save your floorplanned design, follow this simple step:

1. Choose the Save command from the File menu.

   The Save command creates a file with the same name as the current design. The information stored in this file includes the design's hierarchy organization, floorplanned logic, and net and logic selection and color assignments.

   This file represents a snapshot of the current state of the floorplan which you can use later.

Note: The Save command creates an FPN file. Should you try to open a MAP file and there is an associated FPN file for the design, the Floorplanner automatically opens the FPN file, not the MAP file. If the MAP file is newer than the FPN file, the Floorplanner opens both files.

Exiting from the Floorplanner

To exit from the current floorplanning session, follow this procedure:

1. To quit the current session of Floorplanner, choose the Exit command from the File menu.

   If you have not made changes, the Floorplanner exits.

   If you have made changes to the design or the floorplan, this command opens the Confirmation dialog box where you have three options:

- Enter Yes, to save your changes and exit from the application.
- Enter No, if you do not want to save the changes to the design or floorplan, and you want to exit from the application.
- Enter Cancel, to return to the Floorplanner.

Saving the Floorplan as a Constraints File

This procedure explains how to save the floorplanned logic as a constraints file.

1. Select the Write Constraints command from the File menu.

   On workstations, the standard File Open dialog box appears. The Filter box contains the path of the MAP file that the Floorplanner read in.

   On PCs, the Save as dialog box appears. The File Name edit box contains a list of available constraints files.

   By default, the constraints file is named with the same name as the MAP file with the .cst extension.

2. For PCs users, edit the File Name box with the name that you want for the constraints file. Edit Directories if you want to store the constraints file in a different directory.

3. For workstations users, edit the Save as box with the name of the constraints file if you want to store that file in a directory different from that of the MAP file, or if you want to name the constraints file.

4. Click the OK button when you are done.

   The Floorplanner writes the constraints file to the current or specified directory.

Reading and Writing Constraints Files

Constraints files play an important part in floorplanning your design. You can use constraints files as input to both PPR and the Floorplanner. The Floorplanner can read in a constraints file and generate a constraints file that you can use with PPR.

Note: The Floorplanner only recognizes constraints that designate a single location for a given symbol. The Floorplanner does not accept constraints that use wildcards, such as R*C3 or R4C*. If you are tyring to read a CST file that was generated with a text editor, make sure that you have expanded all wildcards.

Reading a Constraints Files

To read in a constraints file, follow this procedure:

1. Choose the Read Constraints command from the File menu.

   The standard file dialog box displays. On PCs the dialog box is labelled, Select constraints file.

2. Choose the desired constraints file.

   When you have selected the file, the Floorplanner reads it in and updates the Floorplan window to reflect its contents, placing logic symbols into the die.

The Read Constraints command ignores previously floorplanned logic, unless the constraints file identifies the specific logic or the occupied resources in the floorplan.

Writing a Constraints File

To write a constraints file, follow this procedure:

1. Choose the Write Constraints command from the File menu.

   If there is no placed logic in the Floorplan window, a dialog box appears with the message, “There are no constraints to write.”

2. Click on OK to continue.

   If there is logic placed in the Floorplan window, the standard file dialog box opens.

3. Edit the dialog box with the desired file name.

   You can give the constraints file any name you want. The Floorplanner saves the file with the .cst extension. You can change the name of the constraints file and its directory in the standard file dialog box.

By default, the Floorplanner generates a *design*.cst file with the name of the current design that represents the current floorplan. The Floorplanner writes this constraints file to the current directory.

Floorplanning Logic Icons in Stacks

This procedure explains how to move groups of logic in stacks. You can place selected hierarchical macros from the Design window as a single group into the floorplan using the stack mode. When you use the stack mode, the Floorplanner treats the placed logic as a single unit. In stack mode, any operation that you perform on a stack, such as selecting, moving, or changing allocation direction, the Floorplanner performs on the entire stack.

Figure 4-1 shows how placed logic appears when you use distribute mode. Notice that each logic symbol occupies a specific resource in the die.

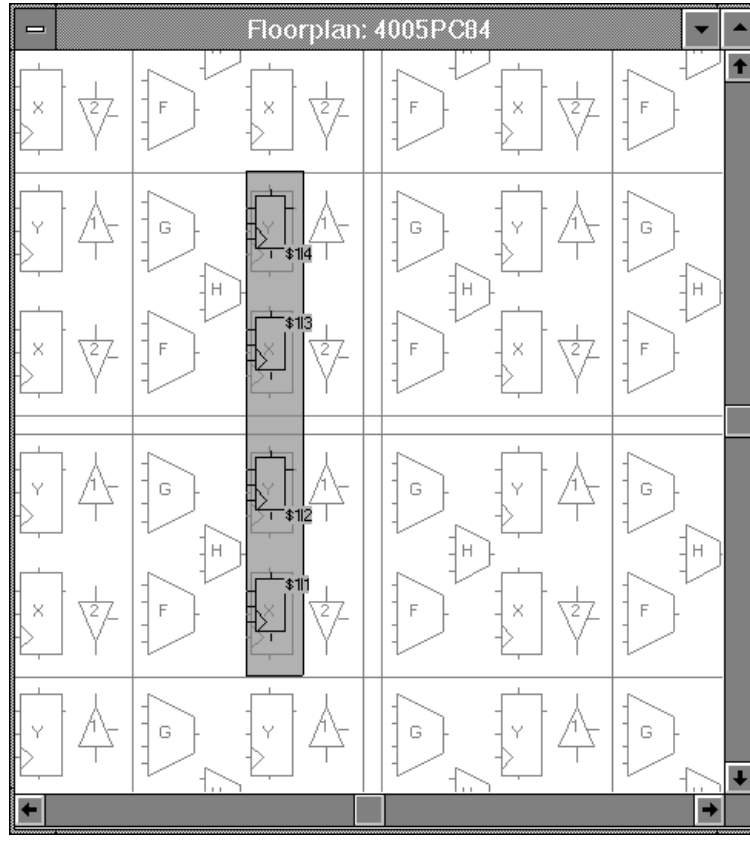


Figure 4-1 Placed Logic (Distribute Mode)

Figure 4-2 shows how placed logic appears when you use the stack mode. Notice how the same resources are occupied, but the logic icons are grouped at the top of the stack.

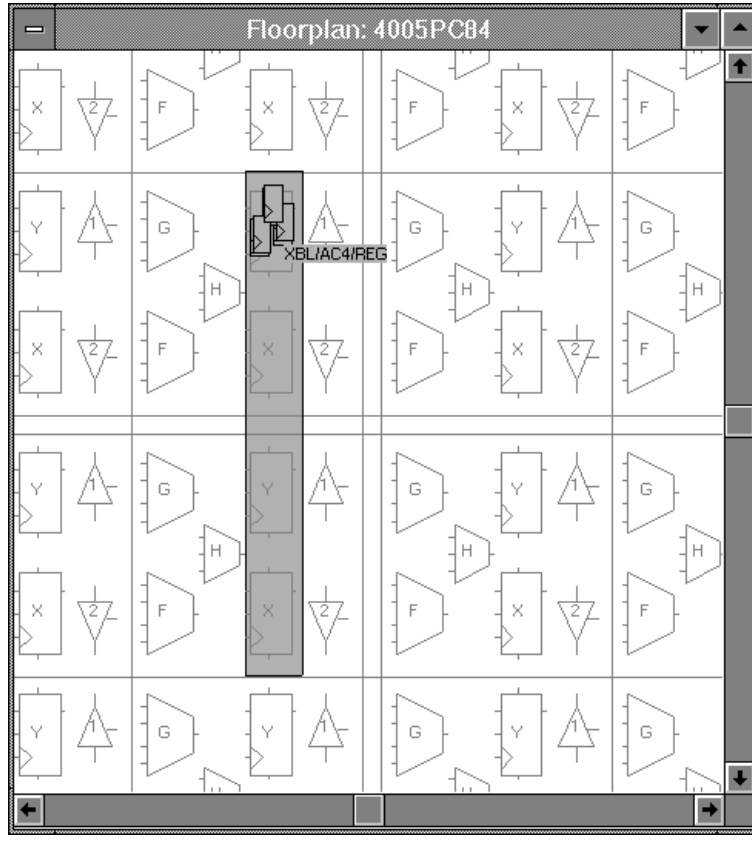


Figure 4-2 Placed Logic (Stack Mode)

When you use the distribute mode to place logic, each element in the stack occupies a specific location in the die. When you use stack mode to place logic, the place and route software determines the location of each element within the area of the die that the stack occupies. Using stack mode essentially creates an area constraints for the stack that is dropped. The area is exactly the size necessary to accommodate all the elements of the stack.

By default, the Floorplanner uses the distribute mode.

Follow these steps to floorplan with stack mode:

1. Change the distribute mode to stack by clicking the Stack Icons toolbar button, shown in Figure 4-3 or by choosing the Stack command from the Floorplan menu.

Figure 4-3 Stack Icons Toolbar Button

2. Use the mouse to select a hierarchical macro from the Design window.
3. Move the group of logic icons that is associated with the selected macro from the Design window, and place it in the Floorplan window.

   The Floorplanner places the stack of logic icons at the nearest appropriate resource where you drop it. The Floorplanner also allocates resources from that point, in the allocation direction, sufficient to accommodate the logic represented by the stack.

Using Colors

The Floorplanner automatically assigns unique colors to hierarchical macros when it reads a new design. Hierarchical nodes that have one lower level of hierarchy are set to the color of that lower level node. Hierarchical macros with more than one lower level of hierarchy, as well as individual symbols are not assigned colors. Individual symbols without assigned colors inherit the color of the lowest level of associated hierarchy.

You can change the colors of any hierarchical macro using the Colors command. If you assign a color to a symbol, that symbol is always shown in that color in both windows. If you assign a color to a hierarchical macro, the colorless symbols under that node will appear in that macro's color when you collapse the node in the Design window.

Note: You can remove color assignments using the Auto Assign button in the Colors dialog box.

The following sections describe using colors in the Design window and in the Floorplan window. The last section describes how to use colors to distinguish between floorplanned logic and place and routed logic.

In the Design Window

1. Select the macros and symbols for which you want to change colors.
2. Select the Colors command from the Edit menu.

   This command opens the Colors dialog box.
3. Click on the button that displays the color you want to use.
4. Click the Apply button to change to the new color.

In the Floorplan Window

1. Select the logic by dragging out an area around the desired logic for which you want to change colors, or click the left mouse button on an individual symbol; double-click the left mouse button on a macro.
2. Floorplan the selected logic that you want to place and route with PPR.
3. Select the Colors command from the Edit menu.

   This command opens the Colors dialog box.
4. Click on the button that displays the color you want to use.
5. Click the Apply button to change to the new color.

Distinguishing Logic

You can use the Color command to distinguish placed and routed logic and floorplanned logic. You can change the color of the floorplanned logic to a color not used in the hierarchy. Then, when you read in the LCA/PM file, the unique color distinguishes the placed and routed logic from other logic in the design.

1. Select all the logic in the design.
2. Select the Colors command from the Edit menu.

3. Choose a new color for the selected logic from the palette in the Colors dialog box.

Note: When colors are automatically assigned, the first two and the last two colors are not included. You can use one of those colors to make the logic distinguishable from the rest of the design.

4. Click the Apply button
5. Select the floorplanned logic by dragging the mouse pointer over the entire Floorplan window.
6. Select the Colors command.
7. Choose a different color from the palette in the Colors dialog box for the selected floorplanned logic.
8. Select the entire design again, and repeat step 5.
9. Select the Place or Place and Route command from the Process menu to run PPR.

   When PPR completes, the Floorplanner reads in the resulting file and updates the Floorplan window as appropriate. Logic that was placed by PPR will appear in the first color selected; the original floorplanned logic will appear in the second color selected.

Note: You can use the Auto Assign button in the Colors dialog box to return to a normal display.

Floorplanning Logic

This procedure explains how to select, move, and manipulate logic symbols from the Design window to the Floorplan window.

First, you must select the desired logic from the Design window. There are two ways to do this:

1. Using the mouse, place the pointer on the logic group icon of the desired macro and click the left mouse button.
2. Alternatively, choose the Find Logic command from the Edit menu to find and select the desired logic.
3. You can type in the instance name, choose a specific type of logic, such as I/O for IOBs, Flip Flops for DFF, or type of connection.
4. Click the Apply button.

If the search criteria that you applied in step 3 is correct, the name of the instance appears in the lower half of the Find Logic dialog box and an arrow will point to the applicable instance or macro in the Design window.

5. Click on the Select All button to select the found logic.
6. Use the mouse and click on the logic icon (between the gray box and the macro instance name) to move a group of icons at one time.
7. If you want to move an individual piece of logic, expand the macro and click on the desired logic icon.

   The logic icons change to a ghost image as you move the mouse pointer.

   You must use the toolbar icons (one of four directional arrow toolbar buttons) to determine the allocation direction. The default direction is from top to bottom.
8. Move the mouse pointer to the desired location on the FPGA in the Floorplanner window.

   The selected logic moves with the pointer as you move the mouse.
9. At the desired location in the Floorplanner window, click the left mouse button to place the logic. The Floorplanner places the logic according to the allocation direction you have chosen.

The following three figures Figure 4-4, Figure 4-5, and Figure 4-6 illustrate the aforementioned procedure, using the mouse to select logic from the Design window.

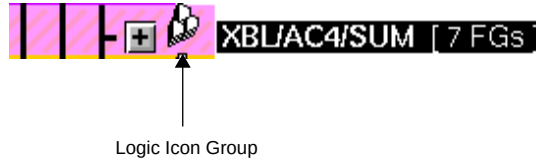


Figure 4-4 Step1: Select an Icon Stack from the Design Window

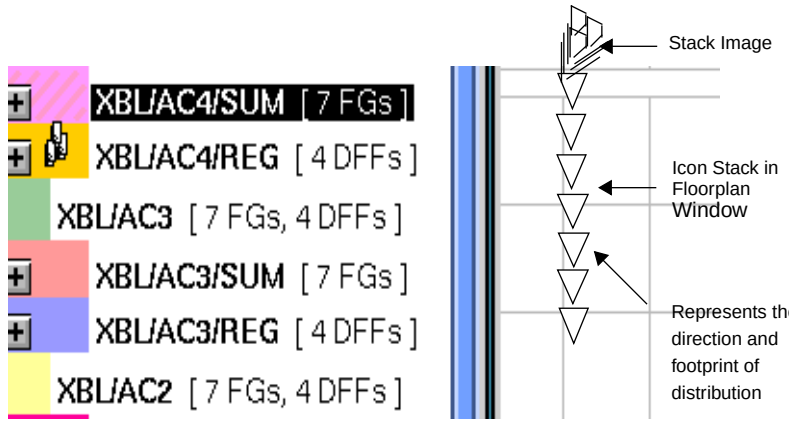


Figure 4-5 Step 2: Icons in Transit from the Design Window to the Floorplan Window

As you move the pointer from the Design window to the Floorplan window, a ghost image of the logic icons showing the allocation direction moves, too.

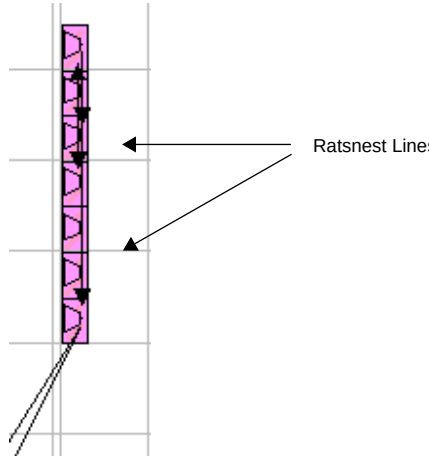


Figure 4-6 Step 3: Logic Icons Placed Using Distribue Mode; Ratsnest Turned On

The Floorplanner uses the allocation direction (in this case, from top to bottom) to place the logic group. You can choose to drop the group in a stack or locked into specific floorplan resources. If you choose distribute mode, each logic symbol is locked into a specific resource as shown by logic symbol drawn on it. If you use stack mode, the logic symbols are drawn in a group at one end of the colored block.

If you have Ratsnest turned on, you will see black lines indicating logic connectivity to the macro you have just selected and placed.

Placing a Stack of IOBs

Placing IOBs in the floorplan is similar to placing other selected logic elements into the Floorplan window, except that the allocation direction changes from a horizontal orientation to a vertical orientation, and vice versa, depending upon the orientation of the IOB resources under the mouse pointer.

When the pointer is over the I/O pads on the left or right of the FPGA die, the allocation direction, by default, is from top to bottom. When the pointer is over the I/O pads on the top or bottom of the FPGA die, the allocation direction, by default, is from left to right. Depending upon where you begin placement you may not have enough IOB resources remaining on the edge of the die to accommodate the stack of selected IOBs.

Note: When placing bonded IOBs, you can only use bonded IOB resources. When placing unbonded IOBs, all IOB resources are available in the die.

To place a stack of IOBs, follow these steps:

1. Determine how many IOBs are in the stack of logic that you have selected.
2. Determine how many IOB resources are available on the edge of the die that you want to use.

   If you do not have a requisite number of IOB resources available to accommodate your stack, the Floorplanner places as many of the IOBs as it can. The unplaced IOBs remain as selected logic as indicated by the ghost image that follows the pointer.
3. To place the remaining stack of IOBs, move the pointer to an area where there are enough IOB resources for the remaining IOBs.

Floorplanning Designs that Contain RPMs

This procedure explains how to floorplan designs that contain RPMs (Relationally Placed Macros). RPMs are optimized macros that have the relative positions of the logic locked down. For this reason, you can only place RPMs as a whole unit into the Floorplan window.

You must have enough resources in the Floorplan window to accommodate the entire RPM, since it must be placed in its entirety. For example, if an RPM is four CLBs in height and the largest vacancy in the die is 3 CLBs high, the RPM will not fit.

1. Select the desired RPM from the Design window.
2. Place the selected RPM into the Floorplan window in an area that can accommodate the entire RPM.

Setting Boundaries in the Floorplan Window

This procedure explains how to set boundaries in the Floorplan window and use the Stack mode to place selected logic. Setting a boundary in the Floorplan window defines an area on the FPGA die into which you place selected logic.

1. From the design hierarchy, select the logic that you want to place into the Floorplan window.
2. Move the pointer to the Floorplan window and click on the Allocate Area toolbar button shown in Figure 4-7 (the leftmost button in the toolbar).

Figure 4-7 Allocate Area Toolbar Button

After clicking on the Allocate Area toolbar button, the pointer changes to a large plus sign (+).

3. Move the pointer to an area in the Floorplan window, then press and hold the left mouse button, dragging out a rectangular area.

   The Floorplanner draws this boundary with broken lines.

4. Place the selected logic into the newly created boundary by releasing the left mouse button.

As you drag out the area, the status bar (at the bottom of the window) displays a message indicating either how many additional resources are needed, or are in excess.

5. Select the Check Floorplan command from the Process menu.

   If you have allocated an area in the floorplan large enough to accommodate the logic, a dialog box appears indicating that the floorplan passes all basic placement checks.

   If you have not defined an area large enough, the Check Floorplan Warnings dialog box appears with a message that more logic resources are needed in the boundary to accommodate the selected logic.

Creating Groups

The hierarchical representation of your design is a result of mapping your original design; it might not be optimized for your floorplanning preferences. To make floorplanning easier, you can rearrange and regroup the design hierarchy.

Note: The function or connectivity of logic elements may be a reason for you to place them together as a group.

Manual Grouping

1. In the Design window, select the logic that you want to group.
2. Select the first piece of logic with the left mouse button and subsequent logic with the middle mouse button. Or, select subsequent logic by holding down the shift key and pressing the left mouse button.
3. Choose the Group command from the Hierarchy menu, or press the F3 key.

   The Floorplanner creates a new group and assigns an arbitrary name to the group “GRP0”. The text line looks like this:

   `GRP0 “Grouped by: User” [`*symbol count*`]`

   where: [*symbol count*] is the number of logic elements

   The Floorplanner labels subsequent new user-created groups “GRP1”, “GRP2”, and so on.

4. You may want to use the Rename command from the Hierarchy menu to give the new group a better name.

   The newly created group occupies a position in the hierarchy, which is in the lowest level of hierarchy, that is common to all logic that comprises the group.

   Figure 4-8 and Figure 4-9 illustrates how to create a new group in the design hierarchy.

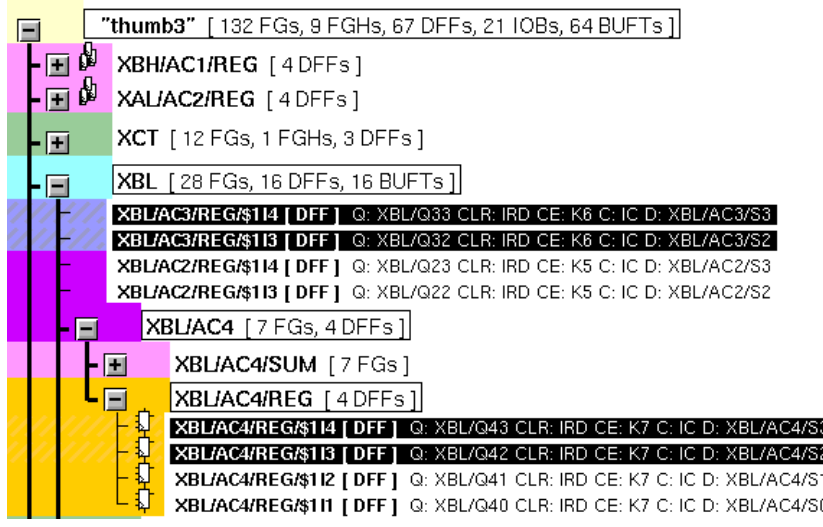


Figure 4-8 Step1: Select Logic for Grouping

Look at Figure 4-8 and note the four D-type flip-flops that appear in reverse video. These are the logic symbols that have been selected to form a new group.

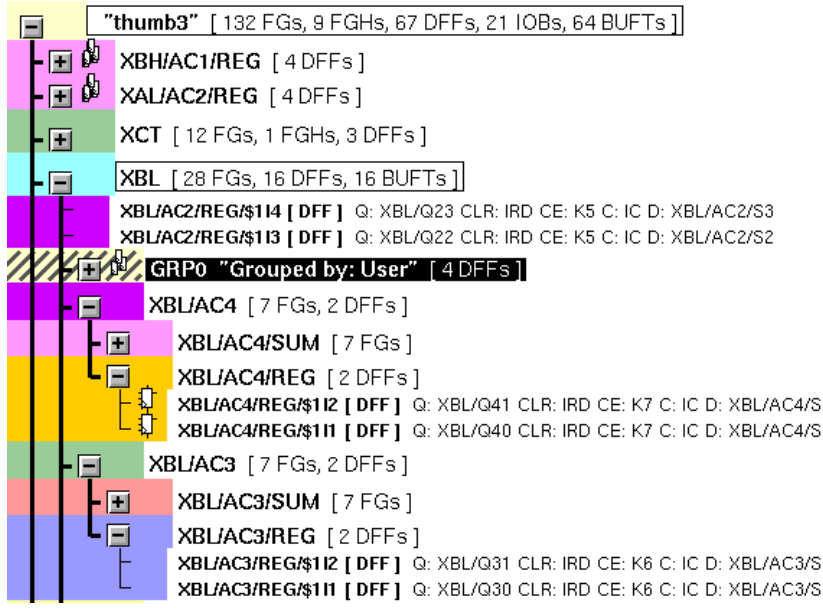


Figure 4-9 Step 2: The Floorplanner Creates New Group

Figure 4-9 shows the new group. Note the new group is named GRP0 (highlighted in reverse video). It is the first new group to be created in the design. Note, that the four flip-flops are no longer part of XBL and AC4, respectively, as indicated by the new symbol counts.

The Floorplanner places the new group in the hierarchy near the macro XBL; the lowest level of hierarchy that is common to the four flip-flops chosen for the group. When you expand the new group you will see that the four flip-flops are now in the new group.

Figure 4-10 shows the new group expanded. You can place this new group as a unit on the floorplan die.

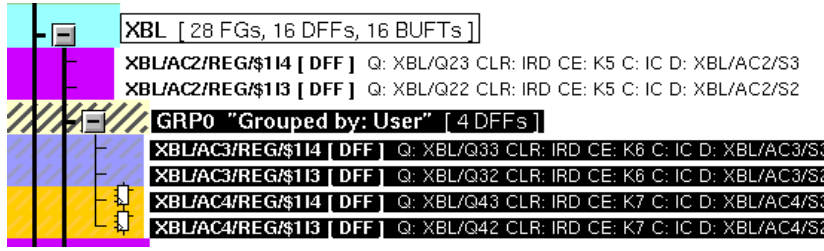


Figure 4-10 GRP0 Expanded to Show Logic Elements

Automatic Grouping

Often, it is more convenient to group logic by common type or signal names. Creating such groups can make it easier to floorplan.

For example, you might want to make a group of all the BUFTs that have a common output enable. In this case, you do the following steps:

1. Choose the Find Logic command from the Edit menu.

   This command opens the Find Logic dialog box.

2. Select a BUFT in the Design window that contains the enable signal of interest by clicking the mouse on the appropriate line (on the BUFT's instance name).

3. Click the triangle in the Connection box to bring up a list of connections from which to choose.

4. Select Common enable (BUFTs).

5. Click the Apply button.

6. Click the Select All button.

   The Floorplanner searches throughout the design hierarchy and highlights each BUFT that meets the criteria you have selected.

Note: The Floorplanner automatically expands macros, which have sub–hierarchy that meet the find criteria.

7. Choose the Group command from the Hierarchy menu, or press the F3 key.

The Floorplanner creates a new group and assigns an arbitrary name to the group "GRP0" (if this is the first user-created group). The text line looks like this:

`GRP0 "Grouped by: User" [`*symbol count*`]`

where: [*symbol count*] is the number of logic elements

Note: You can also use the Group By command dialog box to create these types of groups.

Flattening and Building the Hierarchy

You may have floorplanned the design and saved it. Then, you must make a change to the design at the schematic level which deletes some logic. When you read in the FPN file, the Floorplanner reads in the old hierarchy. Due to the changes made at the schematic level, the old hierarchy shows logic where there is none.

Note: Performing this procedure while selecting the top-level hierarchy flattens the entire hierarchy.

Note: You must select a hierarchical node to enable the Flatten command.

This procedure explains how to flatten the hierarchy in the Design window.

1. Select the part of the design hierarchy that you want to flatten.

   You can select just the level of hierarchy that contains the logic that was changed in the schematic.

2. Select the Flatten command from the Hierarchy menu.

   The Floorplanner removes all lower level hierarchy from the selected hierarchical node and moves all of the associated symbols up in the hierarchy.

How to Rebuild the Hierarchy

This procedure explains how to rebuild the hierarchy using symbol instance names. The ReBuild command works immediately; it does not invoke a dialog box.

Note: The ReBuild command works on all logic, not just selected logic.

1. Select the ReBuild command from the Hierarchy menu.

   The Floorplanner builds a hierarchy tree and places the selected logic symbols in their proper positions in that tree.

Reading a Placed Design

The Floorplanner can read an LCA file (for XC3000, XC4000 devices), that is generated by PPR and place the logic in the Floorplan window.

Note: For XC5200 designs, the Floorplanner reads in a PM file.

To read in an LCA/PM file, do the following steps:

1. Choose the Read Placed Design command from the File menu.

   This command opens the standard file open dialog box. On PCs, this dialog box is labelled Select design file.

2. Select the appropriate LCA/PM file from the list.

3. Click the OK button.

   The Floorplanner reads in the LCA/PM file and places the logic into the Floorplan window as dictated by the file.

Note: Xilinx does not recommend reading in an LCA/PM file that does not correspond to the MAP file.

Walking Through the Design

This procedure explains how to select successive logic by connectivity rather than by name. This process helps you see which floorplanned logic elements drive other logic in the design.

Finding Logic

1. Determine the logic that is of interest.

2. Choose the Find Logic command from the Edit menu.

   This command opens the Find Logic dialog box.

3. Click on the triangle in the Connection box to open the list of valid connections.

4. Choose the desired connection from the list, either Loading Selected Logic or Driving Selected Logic.
5. Click the Apply button.
6. Click the Select All button.

   The Floorplanner searches the design for the appropriate symbols. The Floorplanner highlights the "found" symbols in the Design window with an arrowhead at the left of the symbol line text. Matching symbols in the Floorplan window flash (blink) if you have enabled Flashing.

Finding Nets

1. Determine the nets that you want to find.
2. Choose the Find Nets command from the Edit menu.

   This command opens the Find Nets dialog box and the Ratsnest dialog box.
3. Click on the triangle in the Connection box to open the list of connections.
4. Choose the desired connection from the list.
5. Click the Apply button.
6. Click the Select All button.

   The Floorplanner puts an arrowhead to the left of the net name in the list of Available Nets in the Ratsnest dialog box to indicate which nets meet the search criteria.

   For logic that is placed in the Floorplan window, the Floorplanner searches the design and highlights the appropriate nets by drawing them as red lines. Note that only currently selected nets appear in red; previously found nets, which were deselected, are now drawn with black lines.

Displaying the Ratsnest

The Floorplanner shows connectivity between logic symbols in the Floorplan window with the aid of the ratsnest display. A ratsnest is a display of lines between logic blocks that indicate connections between the inputs and the outputs of floorplanned logic.

By default, the Floorplanner automatically displays ratsnest for selected floorplanned logic and selected nets. Whenever you place selected logic in the Floorplan window, the ratsnest displays the connectivity between the logic symbols.

Using the Ratsnest

By default, the ratsnest is on. As you place selected logic in the Floorplan window, the ratsnest lines show connectivity. You can see which logic is connected to a given net by selecting nets in the Ratsnest dialog box and choosing the appropriate connection.

1. Choose the Ratsnest command from the View menu in the Floorplan window.

   This command opens the Ratsnest dialog box with Auto Display Selected Nets on.

2. Select some floorplanned logic. Use the mouse to draw an area around the desired logic or click on an individual piece of logic.

   The Floorplanner draws the ratsnest to the associated logic.

3. Examine the Displayed Nets box in the Ratsnest dialog box to see the nets connected to the selected logic.

4. Select a net from the Displayed Nets area and look at the Floorplan window.

   The names of the visible nets appear in the Displayed Nets box. The Floorplanner draws a ratsnest of the selected net in red.

Figure 4-11 shows an example of a ratsnest display in the Floorplan window. The Ratsnest dialog box appears in the foreground of the figure. The nets in the Displayed Nets list are the nets for which the ratsnest is drawn.

In the example, the macro GRP0 (the user-created group that is associated with the selected net) is highlighted in the Design window in reverse video.

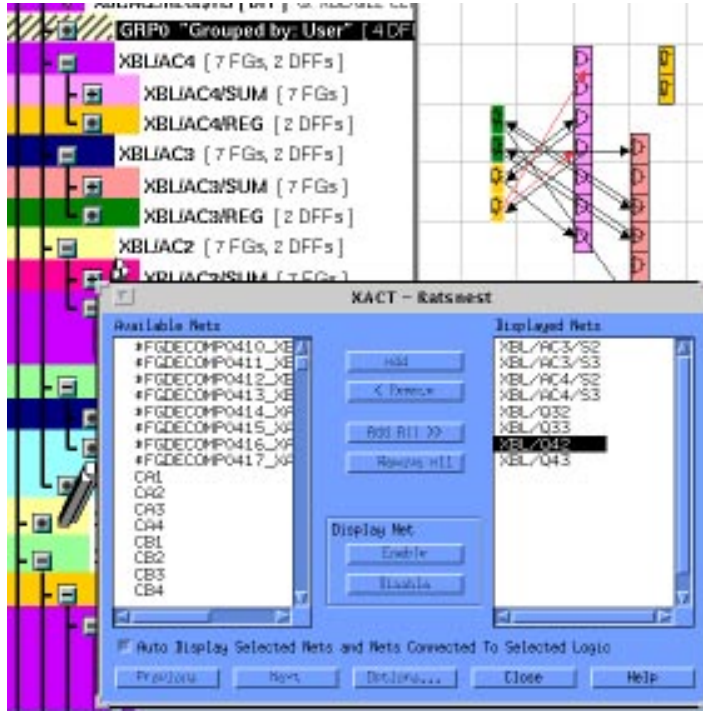


Figure 4-11 Viewing the Ratsnest

Viewing Selected Nets in the Ratsnest

To display a specific net follow these steps:

1. Choose the Ratsnest command from the View menu.

   This command opens the Ratsnest dialog box and lists the available nets that you can display.

2. Click on the Auto Display Selected Nets button to turn off this feature and enable the Add, Add All, Remove, and Remove All buttons.

3. Click on the nets in the list of Available Nets to make a selection.

   With Auto Display Selected Nets off, you can select those nets that you want to display.

4. Click the Add button to include the selected nets in the list of Displayed Nets in the Ratsnest dialog box.
5. Use the Add, Add All, Remove, and Remove All buttons in the Ratsnest dialog box to control which nets appear are in the Displayed Nets list.

   The nets in the Displayed Nets list are the nets that the Floorplanner will show in the Floorplan window.

Analyzing PPR Placement

This procedure describes how to analyze the placement results that PPR generates. You must first run PPR to generate an LCA file (PM file for XC5200).

1. Choose the Read Placed Design command from the File menu.

   The Floorplanner reads the LCA or PM file.
2. Examine the Floorplan for the following potential problems:
   - BUFTs with common output enables that are not vertically aligned or cross over longlines midpoints
   - RAM that is mis-aligned so as to prevent control signals from being routed on longlines
   - RPMs, BUFTs, and other macros source and load nets are close together.
   - Structured logic elements that cross longline splitters into another quadrant.

   Refer to Figure 4-12. Note the positions of the dark–colored BUFTs on the left. The placement is inefficient because two different longlines are required for the output enable signal. These BUFTs are misaligned because they are in two columns, which require different longlines, and are split between two different quadrants, crossing longline midpoints. Now, look at the light–colored BUFTs on the right. These BUFTs represent proper alignment in the FPGA because the common output enable signals connect to same vertical longline.

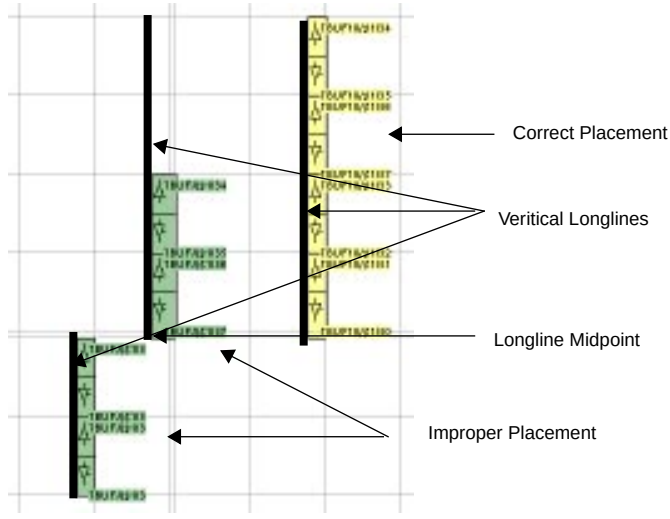


Figure 4-12 BUFT Placement

Figure 4-13 illustrates flip-flop to BUFT alignment in the FPGA. The left half of the example shows ineffective placement; see how the ratsnest lines intersect. The right half of the example shows the proper alignment of the flip-flops and their associated BUFTs as indicated by the parallel ratsnest.

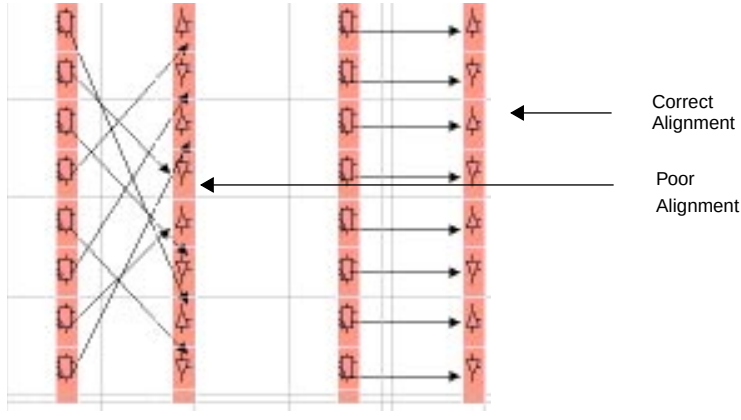


Figure 4-13 RAM/BUFT Alignment Example

Note: For clarity, the flip-flops and BUFTs occupy two different tiles. Normally, you would place this logic in the same tile to minimize the length of the ratsnest.

Figure 4-14 shows an example of placed macros so that the source and load nets are in close proximity. In many cases, where there is sufficient routing resources, you want to place source and load nets close together.

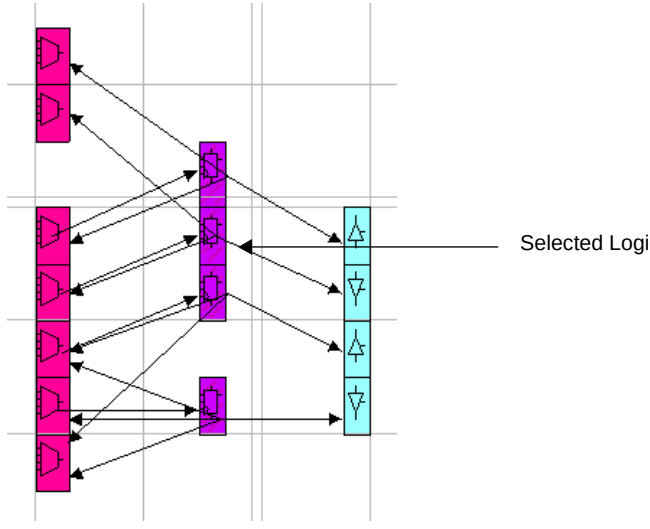


Figure 4-14 Viewing Placed Logic Symbols Using the Ratsnest

Note: In the example, the middle macro is the selected logic from which the ratsnest shows its source nets and load nets.

3. To see that PPR efficiently placed macro symbols, select them from the Floorplan window or the Design window.
4. Step through the design, selecting critical macros, and using the Ratsnest to view the distance between selected macros and their sources and loads.

   The Floorplanner highlights the selected symbols in the Floorplan window.

Analyzing PPR Placement for Timing Specs

This procedure explains how to analyze the placement of floorplanned logic by PPR with respect to TimeSpecs. If you are using the Design Manager, follow the instructions in that section. If you are running Floorplanner on a workstation, follow the instructions beginning with the Examining the PPR Report section.

You should analyze the logic placement in the following sequence:

1. Examine the PPR report for TimeSpecs that were not met.
2. Use Timing Analyzer to find those TimeSpecs that were not met.
3. Use the Floorplanner ratsnest to view the path.
4. Improve the placement of logic to shorten time delays.
5. Rerun PPR with the improved placement.

The example used in this procedure has two TimeSpecs placed in the design. TSO1 is a 30 nanosecond delay from flip-flop to flip-flop. TSO2 is a 12 nanosecond delay from flip-flop to pad.

From the Design Manager

If you are running the Floorplanner from the Design Manager, follow these steps to analyze the placement with regard to your TimeSpecs:

1. Select a routed design revision from the Project View.
2. Open up the Report Browser in one of three ways:
   - Select the Report Browser command from the Utilities menu.
   - Click on the Report Browser toolbar button.
   - With the mouse pointer in the Design Manager window, click the right mouse pointer to bring up the Reports pop-up menu, and select Report Browser.
3. From the Report Browser, double-click on the XACT Performance report icon.
4. Examine the report for any missed TimeSpecs.
5. If you find that there are missed TimeSpecs in your design, click on the Timing Analyzer toolbox button in the Design Manager.

This step opens the Timing Analyzer window which displays the report file.

6. Select the TimeSpec Filters command from the Path Filters menu on the Timing Analyzer window.
7. Select Report Paths Failing TimeSpec item from TimeSpec Filters.
8. Select Performance to TimeSpecs command from the Analyze menu.
9. Select the Save Report command from the File menu on the Timing Analyzer window.

   This step saves the TimeSpec Summary report to the name of the design revision, by default.

Note: You can choose another directory to which you can save the report.

10. Follow the instructions in the "Using XDelay to Find Missed TimeSpecs" beginning with step 5 to locate the design logic that has failed the TimeSpec.

Examining the PPR Report

For workstation users, follow this step to view the PPR report and run XDelay for TimeSpecs that were not met.

1. Review the PPR report (PPR.log or *design*.rpt) for resource utilization, error messages, and warnings.

   The PPR report contains, among other information, a timing analysis summary of the circuits that contain TimeSpecs. Refer to Figure 4-15 to see the Timing analysis summary of the example design. The asterisk to the left of the TSO2 indicates that the current placement in the Floorplan window does not meet the TimeSpec.

```
---------------------------------------------------------------------
Timing analysis summary
---------------------------------------------------------------------

    Deadline  Actual(*)  Specification
    --------  ---------  -------------
(*)   12.0ns   12.2ns    TS02=FROM:FFS:TO:PADS
      30.0ns   22.2ns    TS01=FROM:FFS:TO:FFS
      <auto>    5.5ns    DEFAULT_FROM_PADS_TO_FFS=FROM:pads:TO:ffs

(*) Note: the actual path delays computed by PPR indicate that 1 of 2
timing specifications you provided was not met.  To confirm this result,
please use the -FailedSpec and/or -TSMaxpaths options of the
Xdelay-TimeSpec command, accessible through the XDE or XDelay program.
```

Figure 4-15 Partial PPR Report Showing Missed TimeSpec

Using XDelay to Find Missed TimeSpecs

Once you have the PPR report that indicates missed TimeSpecs, you can use XDelay to get a detailed report of the path.

1. Invoke XDelay in standalone mode, using one of the following methods:
   - On PCs, open the Main window, select the MS-DOS Prompt icon and type **`xdelay`** at the prompt.
   - On workstations, open a shell window and type **`xdelay`** at the prompt.
   - From the Design Manager select the PerformtoTimeSpec command.
2. Select the XDelay-Timespec command from the Timing menu.

   This command opens the XDelay-TimeSpec_popup window, which contains several delay options.
3. Select the -FailedSpec option from the list and click Done.
4. Select the Report command from the Misc menu to output the results to a file.

   XDelay generates the XDelay Report file (XRP), which includes information about which TimeSpecs have failed.

Note: If you invoke XDelay from XDM, select the -o option and the -TimeSpec option then perform steps 3 and 4.

5. Use a text editor to edit the XDelay Report to include just the information for the path that failed the TimeSpec.
6. When you have edited the XDelay report to list the symbol names or net names in that are in the path, write the information to a file.

Later, you will read this file into the Floorplanner to help locate the failed path.

Figure 4-16 shows the edited XRP file for the example design.

```
Source clock net : "CLK" (Rising edge)
 Worst case clock delay from origin "i_bufgp_tl.I" is 5.4ns.
From: Blk $1N18          CLOCK to CLB_R4C1.YQ    :    3.0ns (  3.0ns)
Thru: Net $1N18                to P66.O          :    2.2ns (  5.2ns)
  To: O pin to PAD, Blk $1N16                    :    7.0ns ( 12.2ns)
~
```

Figure 4-16 Edited XDelay Report Showing Path for Missed Spec

Using the Find Nets and RatsNest to Find Critical Nets

With the edited XDelay report, you can use the Floorplanner Find Nets command to display the paths that need fixing.

1. Select the Find Nets command from the File menu.

   This command opens the Find Nets and Rastnest dialog boxes.
2. Type in the name of the edited XDelay report file in the From File area. Or, click the Browse button to display the standard file open dialog box from where you can select the edited file.
3. Click the Apply button in the Find Nets dialog box.

   Figure 4-17 shows the Find Nets dialog box. Note that it indicates that the Floorplanner found two nets from the edited XDelay report file.
4. Click the Select All button in the Find Nets dialog box and look at the Floorplanner window.

Note: You can also identify nets that have long delays by looking at the XDelay report and searching for the net by name.

Note: The Floorplanner does not recognize the names of nets that have been split by PPR. Such names appear in the XDelay report with a trailing "_1", "_2", and so on. You must remove the underscores and numbers from the net names so that the Floorplanner can recognize the net names.

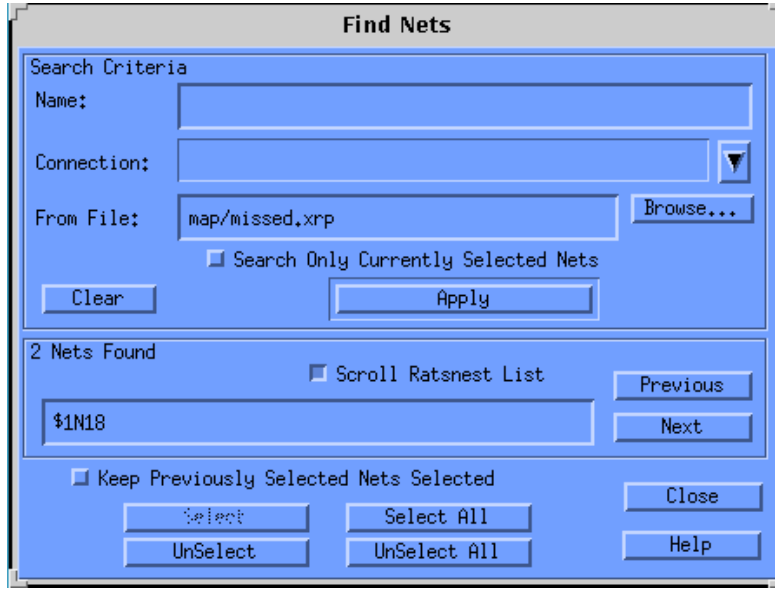


Figure 4-17 Find Nets Dialog Box

The Floorplanner displays the ratsnest in red. The length of the ratsnest does not correlate to a specific time delay. However, by moving logic blocks to shorten the ratsnest, you can improve on the delays.

Figure 4-18 shows the ratsnest for the failed TimeSpec in the example design.

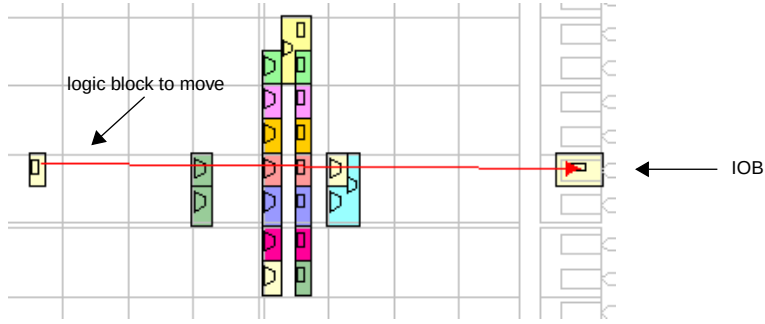


Figure 4-18 Ratsnest of the Failed TimeSpec Path in the Floorplan Window

Now that you know where the routing delay is in the Floorplan window you can manually move logic blocks to shorten the ratsnest and improve the routing delays to meet the TimeSpec.

Figure 4-19 shows the example design.Compare this figure with Figure 4-18 and see that the logic block has been repositioned to be closer to the IOB.

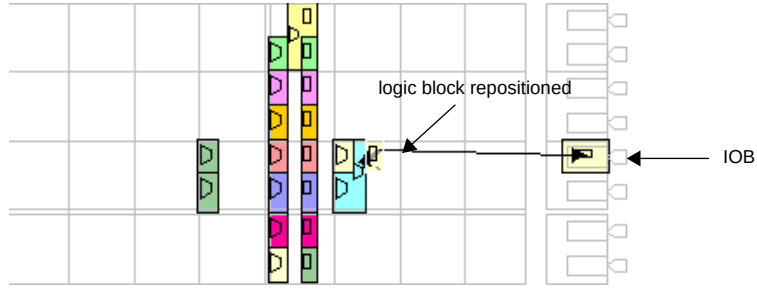


Figure 4-19 Repositioned Logic in Floorplan Window

5. After you have manually repositioned the logic, select the Write Constraints command from the File menu.
6. Run PPR again to see whether the new placement meets the TimeSpec in the design.

Figure 4-20 shows the resulting PPR report for the example. Note that the new placement meets the TimeSpec requirements as shown in the Actual column.

```
--------------------------------------------------------------------
Timing analysis summary
--------------------------------------------------------------------

    Deadline  Actual(*)  Specification
    --------  ---------  -------------
      12.0ns   11.7ns    TS02=FROM:FFS:TO:PADS
      30.0ns   22.2ns    TS01=FROM:FFS:TO:FFS
      <auto>    5.5ns    DEFAULT_FROM_PADS_TO_FFS=FROM:pads:TO:ffs

(*) Note: the actual path delays computed by PPR indicate that ALL timing
specifications you provided have been met.  Please use the -FailedSpec
and/or -TSMaxpaths options of the Xdelay-TimeSpec command, accessible
through the XDE or XDelay program, as a final confirmation of the
performance of your design.
```

Figure 4-20 PPR Report; New Path Meets TimeSpec

Finding Logic Connected to Nets

Often it is difficult to find a specific piece of logic or the nets that connect them. The following procedure explains how to find logic that is connected to nets in the floorplanned design.

You choose the desired selection criteria such as, name or connection. The Floorplanner places a black arrow to the left of the name of the found logic in the Design window. When the ratsnest is turned on, the Floorplanner draws black lines between logic in the Floorplan window, indicating connectivity to the selected logic.

This procedure is more useful when you can view the selected net in proximity to the floorplanned logic.

1. Choose the Find Nets command from the Edit menu.

   This opens the Find Nets dialog box and the Ratsnest box.

2. Select a net name.

   In the Find Nets dialog box, fill in the Search Criteria for the desired net.

3. Click the Apply button.

4. Click the Select All button.

5. Choose the Find Logic command from the Edit menu.

   This command opens the Find Logic dialog box.

6. Click the black triangle in the Connection box to expand the list of valid connections.

7. Choose the connection type (either Loading Selected Nets or Driving Selected Nets) that you want from the list.

8. Click the Apply button.

   For example, if you choose "Driving Selected Nets" the Floorplanner finds all the logic symbols that drive the input to the desired net as indicated by a black arrowhead to the left of the symbol name in the Design window.

9. If any symbols are found, click the Select button or the Select All button to highlight them in the Design window or the Floorplan window (if you have floorplanned logic).

Displaying Resources and Logic

You can display the logic resources that are available on the FPGA in the Floorplan window. For example, the XC4000 family has these resources; F, G, and H function generators, Global Buffers, D-type flip-flops, Tristate Buffers, I/O, and RAM/ROM.

Note: Screen refreshes take longer when you display all of the resource graphics in the Floorplan window than when you just use the default settings.

By default the CLB resources are turned off to reduce the clutter in the Floorplan window. Only the Grid and I/O options are enabled.

1. Choose the Resources command from the View menu, or press the F2 key.

   This command opens the Resources dialog box.

2. Determine the type of resources that you want displayed in the Floorplan window and click those boxes to enable the display.

3. Click the OK button.

Figure 4-21 illustrates a partial display for an XC4000 device with all of the resources in the CLB enabled for display.

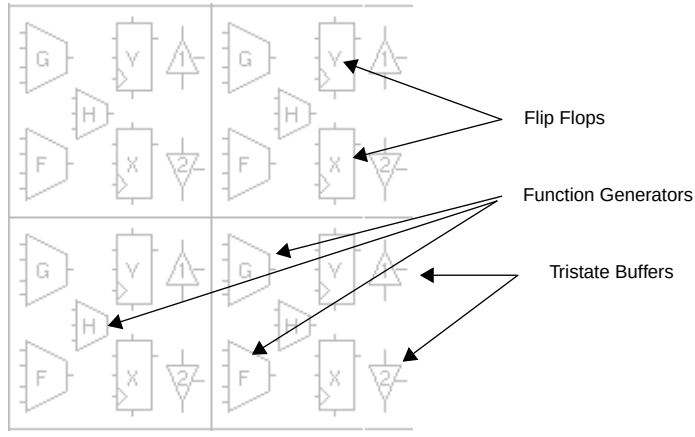


Figure 4-21 Display of Resources in the Floorplan Window

shows how resources and placed logic affect which information the floorplan window displays.

Table 4-1 Resource Graphics Display

Resources	Placed Logic	Display
Off	Off	Blank
On	Off	Shows available resources (not occupied by logic)
Off	On	Shows used resources
On	On	Shows both used and available resources

Performing High-Level Floorplanning

High-level floorplanning is a process to see how the data flow fits into the specified FPGA architecture. It involves working with the macros in the design and a particular logic placement mode.

The Floorplanner supports two placement controls for placing logic into the Floorplan window; the drop mode and the drop direction.

Drop mode is either distribute or stack. The distribute drop mode allows you to place selected logic into the Floorplan window so that you can manipulate individual pieces of logic. The stack drop mode allows logic in a macro to be assigned to a given area where each piece of logic does not have a fixed location. When you select logic placed with this mode, you select the entire macro and manipulate many pieces of logic, at the same time. The drop direction can be up, down, right, left, or spot. You can use combinations of these two modes when floorplanning the design.

One such useful combination for high-level floorplanning is stack drop mode and spot drop direction. In this mode, the Floorplanner places stacks of selected logic on a single resource in the device. Although not a legal placement, it does give you a sense for the connectivity and logic flow of your design. This placement mode also helps you determine how to group the logic in the design for more effective floorplanning.

Once you have established a high-level floorplan, select the logic that forms a group in the Floorplan window and create those groups in the existing hierarchy.

1. From the toolbar, click on the Stack Icons (Figure 4-22) and Drop Icons one at a time (Figure 4-23) buttons to enable the stack drop mode and the spot drop direction.

Figure 4-22 Stack Icons Toolbar Button

Figure 4-23 Allocate Manually (Spot) Toolbar Button

2. In the Design window, select a macro from the design.
3. Place the selected logic in the Floorplan window at the desired location.
4. Choose the Find Logic command from the Edit menu.

   This command opens the Find Logic dialog box.

5. In the Connection box, choose either Driving Selected Logic or Loading Selected Logic from the list of valid connections to identify the next group of logic to place in the Floorplan window.

Once you have traced a path completely through the design, you might want to group the logic of this path, as follows:

6. Select all of the logic symbols in the path.
7. Choose the Group command from the Hierarchy menu, or press the F3 key.

   The Floorplanner creates the new group and assigns the appropriate "GRP" label. The first new group is labelled GRP0.
8. Repeat this process of finding logic and creating groups as necessary.

Performing Detailed Manual Placement

This procedure describes how to manually place logic into the Floorplan window, by selecting individual symbols from the design hierarchy and placing them in the Floorplan window.

You can place an entiresgroup of logic icons, at one time, using the Distribute toolbar button and dropping the icon stack in the floorplan.

You can also select a stack of logic icons in the Floorplan window, and use the Distribute toolbar button to distribute those selected icons within the pre-allocated pattern that you define with the mouse pointer and using the Allocate toolbar button.

Note: You can only place an RPM as an entire macro.

Follow these steps to manually placed selected logic into the Floorplan window:

1. Expand a node in the Design window to show all of the symbols under that hierarchy. Figure 4-24 shows an example of an expanded macro..

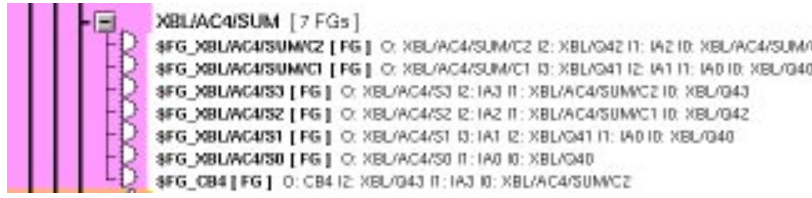


Figure 4-24 Expanded Macro in the Design Window

2. Pick one symbol at a time and place it in the desired location in the Floorplan window. Figure 4-25 shows the cascaded Design and Floorplan windows. Note that the floorplanned logic symbol is highlighted in reverse video in the design hierarchy.

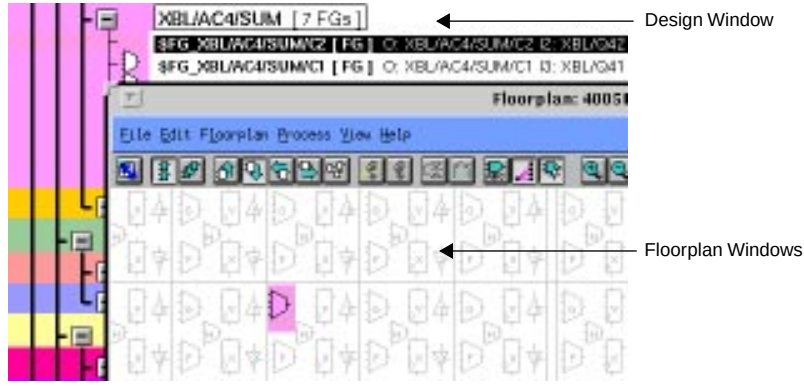


Figure 4-25 Placed Logic Symbol in the Floorplan Window

3. Repeat step 2 until you have placed all the symbols of the selected node in the Floorplan window.

Checking the Floorplan

The Check Floorplan command checks the floorplanned logic for placement problems. The Floorplanner runs the Check Floorplan command from the Process menu automatically when you select the Place or Place and Route commands from the Process menu.

If the Floorplanner finds no placement problems, it generates a message indicating that all basic checks passed.

If you select either the Place command or the Place and Route command, the Floorplanner opens the Check Floorplan Warnings dialog box with a list of warnings when placement problems are found.

1. You can find the logic that is associated with a warning by double–clicking on that warning in the dialog box.

   The Floorplanner zooms in to the problem logic, which appears highlighted.

2. You can also find the problem logic by single-clicking and clicking the Find button on the dialog box.

   If you have flashing enabled, the problem logic flashes in the Floorplan window.

If you choose the Place command or the Place and Route command, the Floorplanner issues a message stating that there are problems, when they are encountered, and asks if you want to continue processing.

Aligning Symbols

This procedure explains how to align symbols. When you are placing logic in the Floorplan window, aligning symbols reduces unnecessary routing between the placed logic elements. Remember, you can use the ratsnest to see the alignment of the placed logic.

The following considerations are important when floorplanning the design:

- Align tristate buffer enable signals. By placing tristate buffers with common enable signals in the same column, PPR will utilize a single longline to connect all the enables to the source.
- Align TBUFs with common output enable (OE) signals in a column.
- Align clock enable signals. By placing flip-flops with common clock enables in the same column, PPR will utilize a single longline to connect all the clock enables to the source.

- If an enable is sourced by an I/O, place the IOBs close to the column in which the longline runs to minimize the routing required for connections to that longline.
- Use the Group by command to create groups of related logic for quicker placement into the floorplan. Figure 4-26 shows the Group by dialog box for the XC4000 family.

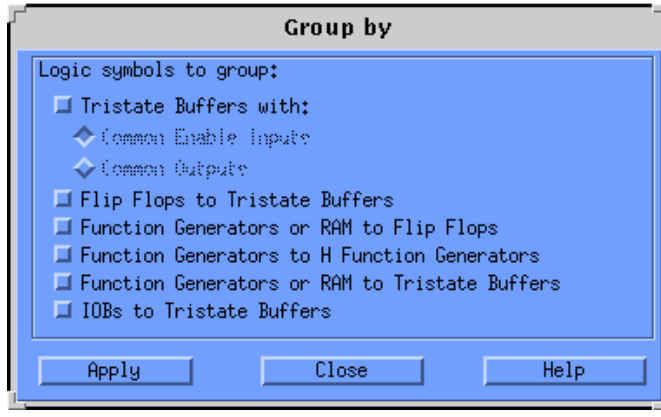


Figure 4-26 Group By Dialog Box for XC4000 Devices

Perform the following steps to align logic symbols in the Floorplan window:

1. Prior to floorplanning, use the Group by command to make groups of flip-flops to tristate buffers.
2. Floorplan the groups of flip-flops to tristate buffers (if small enough) into the same quadrant in the Floorplan window.

   For additional details, refer to the "Analyzing PPR Placement" procedure.
3. Floorplan the IOBs such that they are aligned with the flip-flop to tristate buffer groups. Use the Ratsnest command from the View menu to show the alignment of the placed logic.

The example design shown in Figure 4-27 contains 16 flip-flops, 12 IOBs, 16 BUFTs, and one BUFGP.

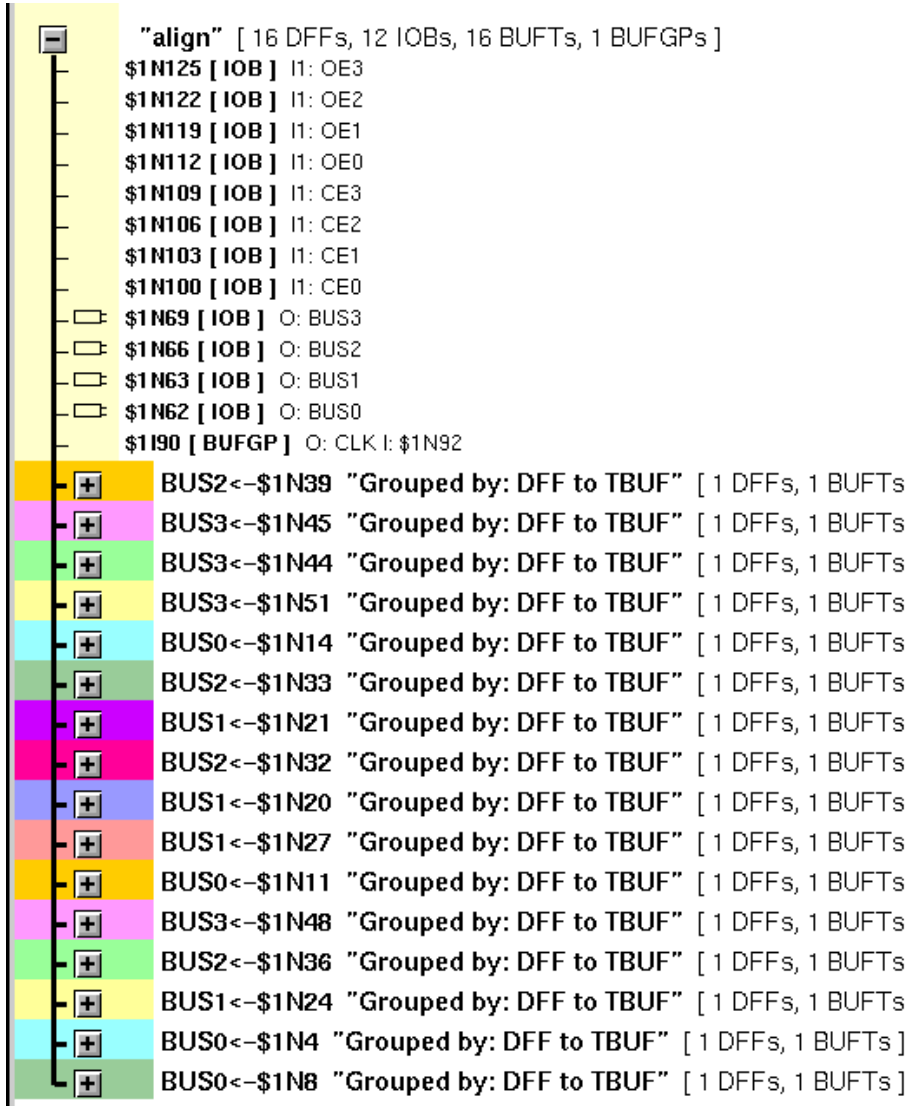


Figure 4-27 Example Design

Figure 4-28 shows the example design, floorplanned such that the logic symbols are aligned.

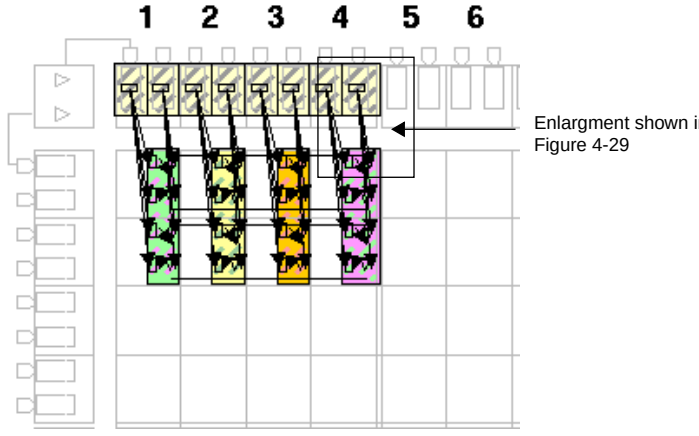


Figure 4-28 Properly Aligned Logic Symbols

Figure 4-29 shows a closer view of a part of the floorplanned design shown in Figure 4-28. Note the alignment of the nets sourced by IOBs $1N100 and $1N112. BUS3 is aligned to a horizontal longline.

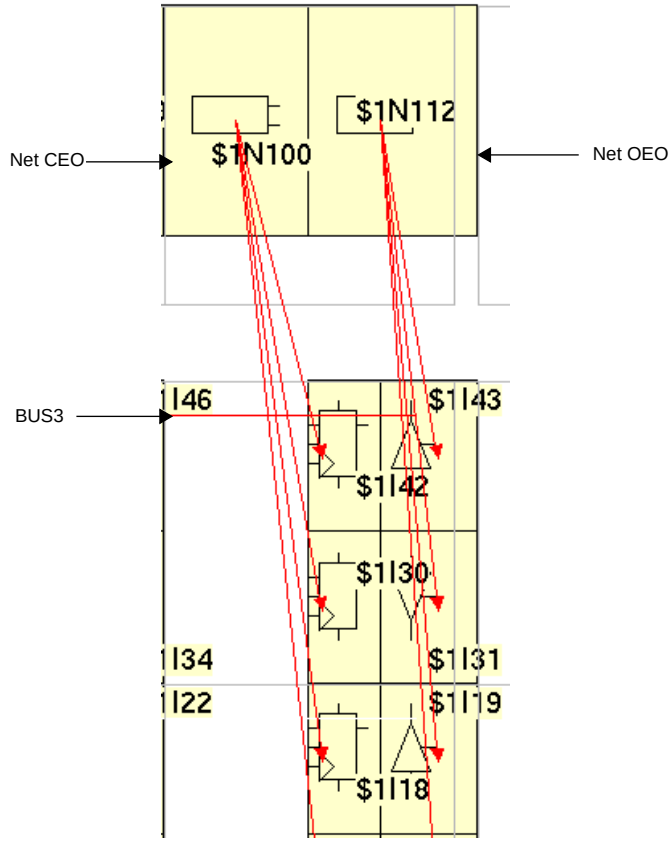


Figure 4-29 Close-up of Aligned Logic Symbols

Working with Patterns

This procedure explains how to work with patterns when you place selected logic in the Floorplan window. You can use the Capture Pattern and Impose Pattern commands from the Floorplan menu or use the Capture Pattern and Impose Pattern toolbar buttons. These commands allow you to create a reference pattern of placed logic that you can use later when you are placing similar logic. The reference pattern represents the relative placement and spacing of individual pieces of floorplanned logic.

Note: Except for RPMs, you must have logic placed in the Floorplan window before you can use the Capture Pattern command. RPMs have a pattern. You can pick up an RPM and capture its pattern before dropping it into the Floorplan window.

Creating a Pattern

You can select the Capture Pattern command from the Edit menu in the Floorplan window or use the Capture Pattern toolbar button shown in Figure 4-30.

Figure 4-30 Capture Pattern Toolbar Button

Follow these steps to create a pattern that captures the placement and spacing information of placed logic in the Floorplan window.

1. Select some logic from the Design window and place it in the desired locations in the Floorplan window.
2. Select the logic in the Floorplan window, which makes the pattern that you want to capture for future use.
3. Select the Capture Pattern command from the Edit menu (in the Floorplan window), or click the Capture Pattern toolbar button.

Using a Pattern

Imposing a pattern can only be done after you have captured a pattern. You can select the Impose Pattern command from the Edit menu in the Floorplan window or use the Impose Pattern toolbar button shown in Figure 4-31.

Figure 4-31 Impose Pattern Toolbar Button

Follow these steps to use a reference pattern to place selected logic from the design hierarchy into the Floorplan window.

Note: Use the Impose Pattern command on logic that is similar to the placed logic whose placement was captured as a pattern.

1. Select the desired logic from the design hierarchy.
2. Select the Impose Pattern command from the Edit menu (in the Floorplan window) or click on the Impose Pattern toolbar button.
3. Move the selected logic into the Floorplan window.

   The Floorplanner reads the placement and spacing information from the reference pattern to place the selected logic.

Note: You can use the Impose Pattern command on transitory logic or selected logic that is already placed in the floorplan die.

How to Interleave Buses

This procedure explains how to interleave buses. The Spacing command in the Floorplan menu makes interleaving easy. Interleaving spreads out the resources associated with a bus, such that other logic can be interspersed with the bus. A goal of interleaving is to minimize the distance between similar bits of interrelated buses.

You should be aware of the following considerations each time you begin this procedure:

- Determine the spacing requirements that suits your particular interleave scheme.
- If not already set, change the allocation mode to distribute, by clicking on the Distribute toolbar button.
- From the Floorplan menu choose the Spacing command to change the spacing value.

Note: A value of 2 causes the Floorplanner to place selected logic in every second available resource in the floorplan; a value of 3 causes the Floorplanner to place selected in every third available resource.

Design Example

Figure 4-32 shows the example design, which contains a 16-bit bus (REGISTER_A/Q) that talks to an 8-bit bus (LITTLE_BUS_OUT).

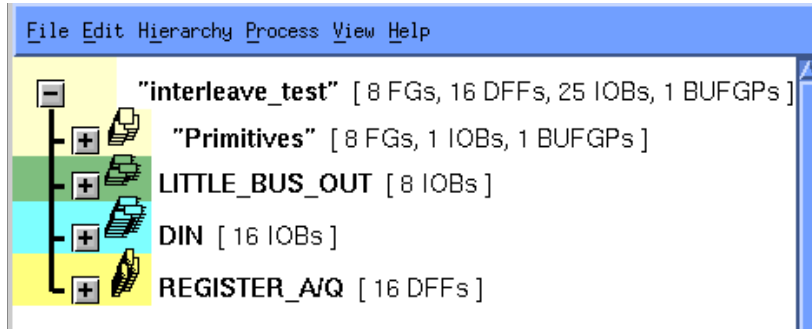


Figure 4-32 Interleave Design Hierarchy

Figure 4-33 shows the expanded hierarchy of the interleave design.

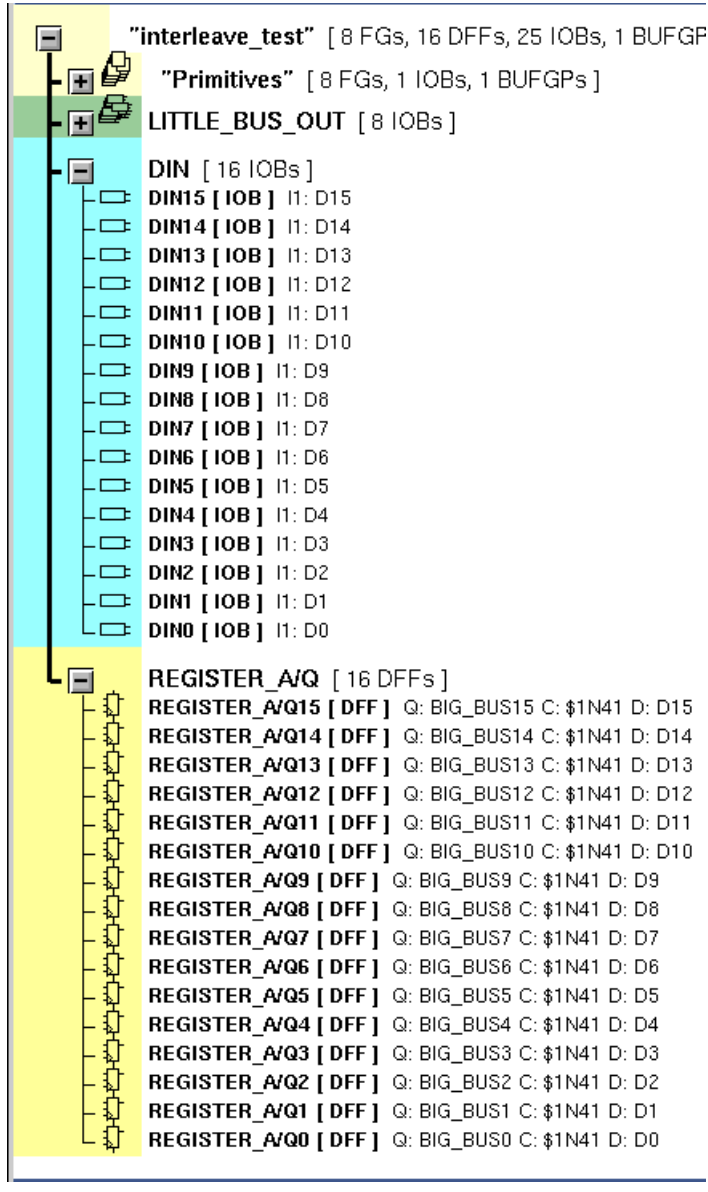


Figure 4-33 Interleave Design Hierarchy Expanded

From the expanded hierarchy, four new groups were created to make floorplanning easier:

- REGISTER_A_LSB and REGISTER_A_MSB
- DIN_LSB and DIN_MSB

Figure 4-34 shows the interleave design hierarchy with the four new groups. Note the `"Grouped by: User"` annotation on the symbol line.

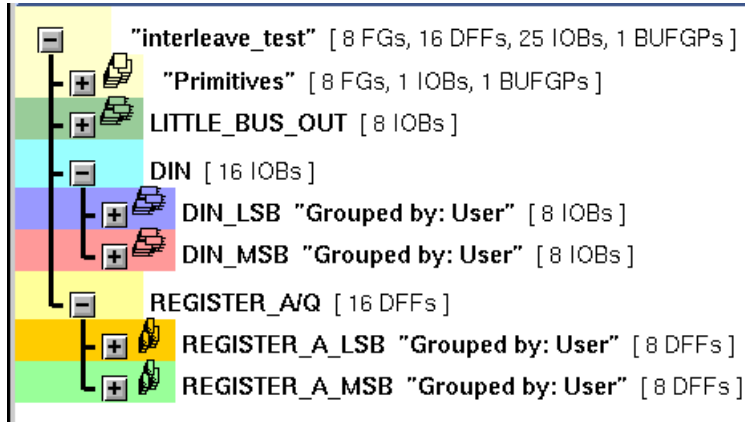


Figure 4-34 Interleave Design with New Groups

Note: The placement used throughout this example is exploded to make it easier to view; it is not optimal floorplanning placement. During floorplanning you would choose a placement that is closer together, resulting in shorter interconnections.

The next set of graphics Figure 4-35 through Figure 4-40 show step-by-step the sequence for placing the groups of logic into the Floorplan window. Figure 4-41 shows the final placement in the Floorplan window of the interleave design. The ratsnest display shows the relative distance and connectivity of the nets.

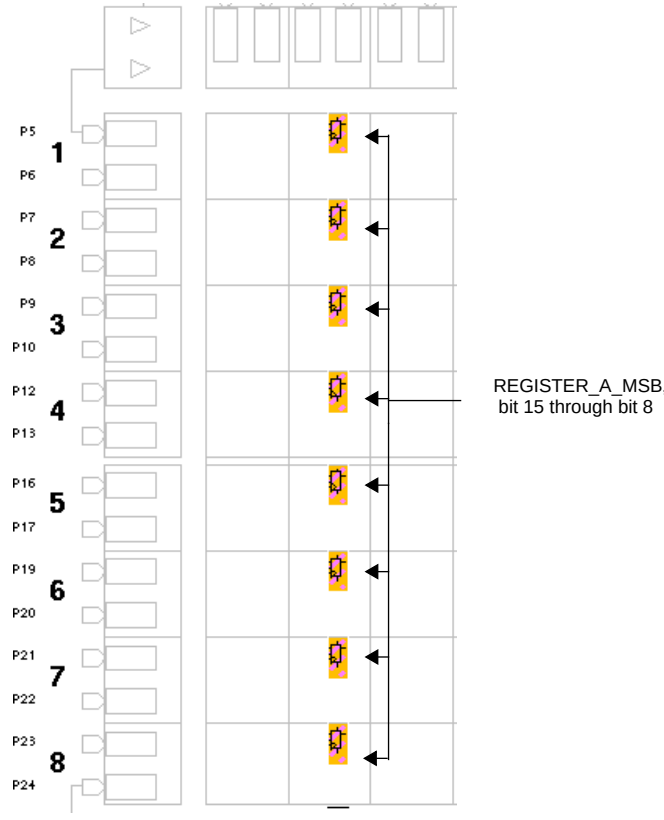


Figure 4-35 Step 1: Placement of the REGISTER_A_MSB Group

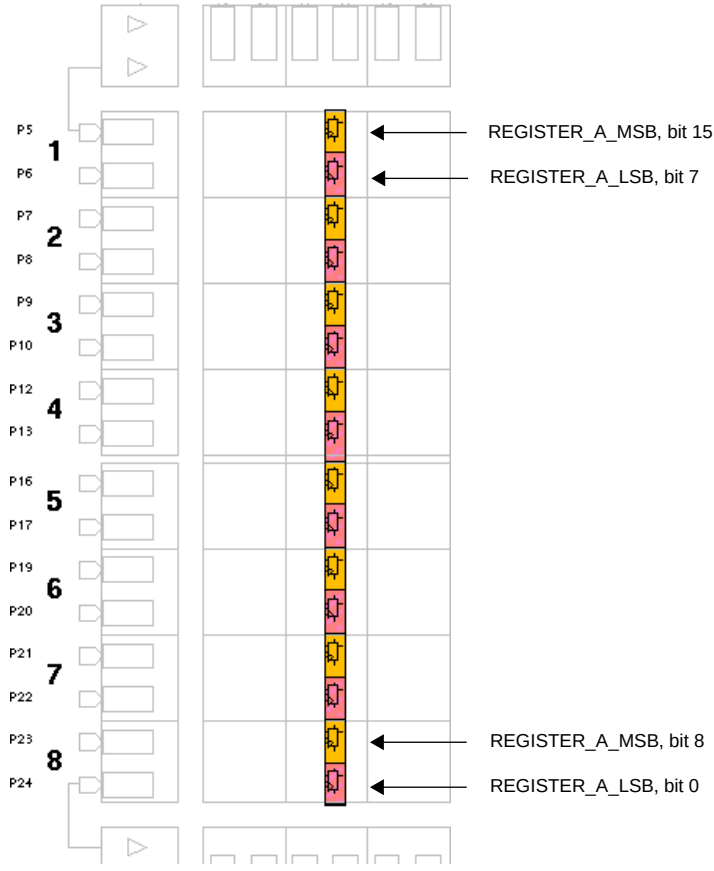


Figure 4-36 Step 2: REGISTER_A_LSB Group Interleaved with REGISTER_A_MSB

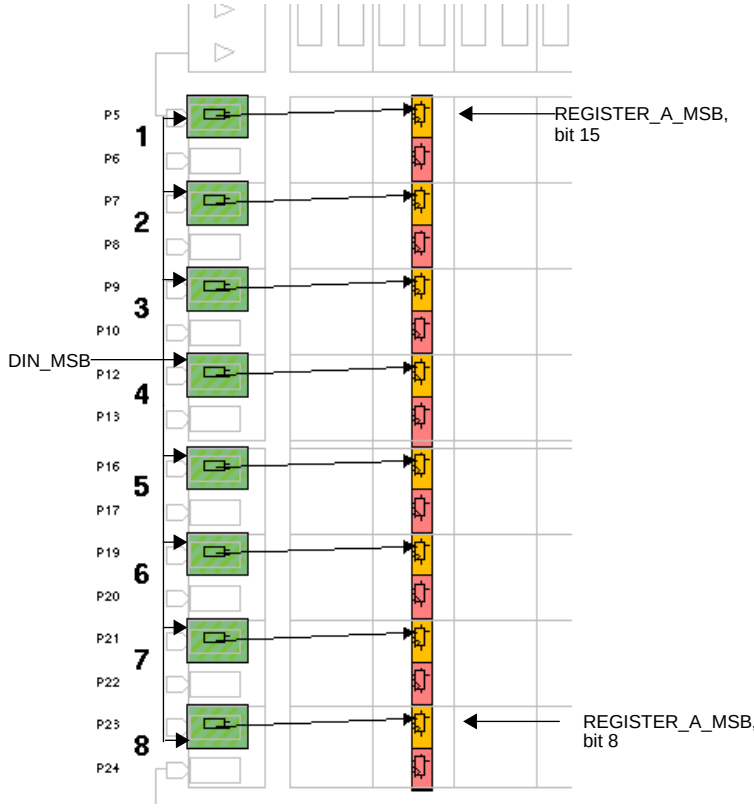


Figure 4-37 Step 3: DIN_MSB Placed to Align with REGISTER_A_MSB

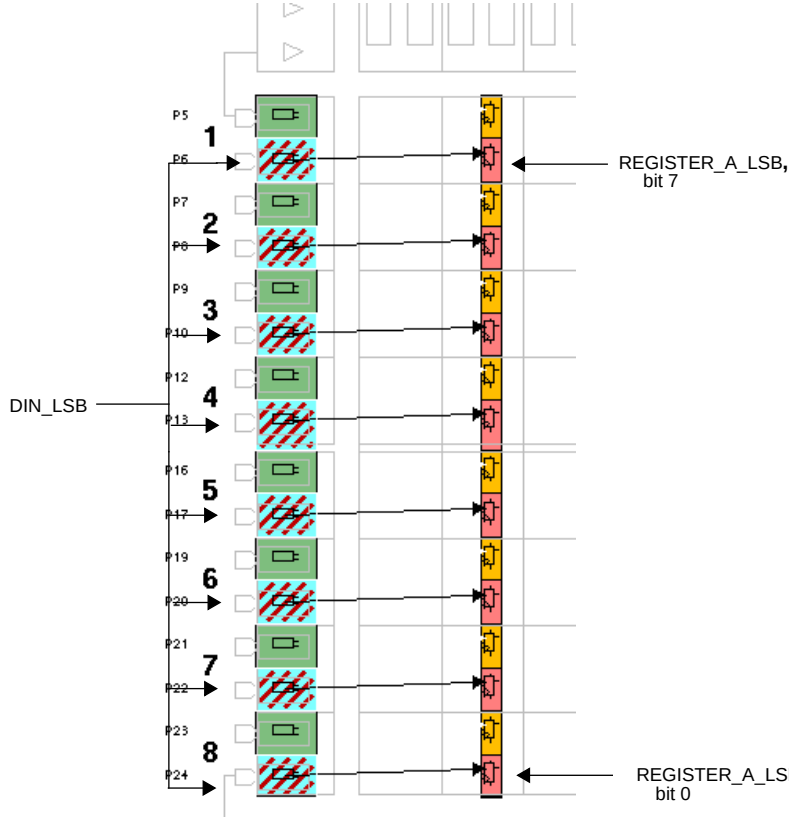


Figure 4-38 Step 4: DIN_LSB Placed to Align with REGISTER_A_LSB

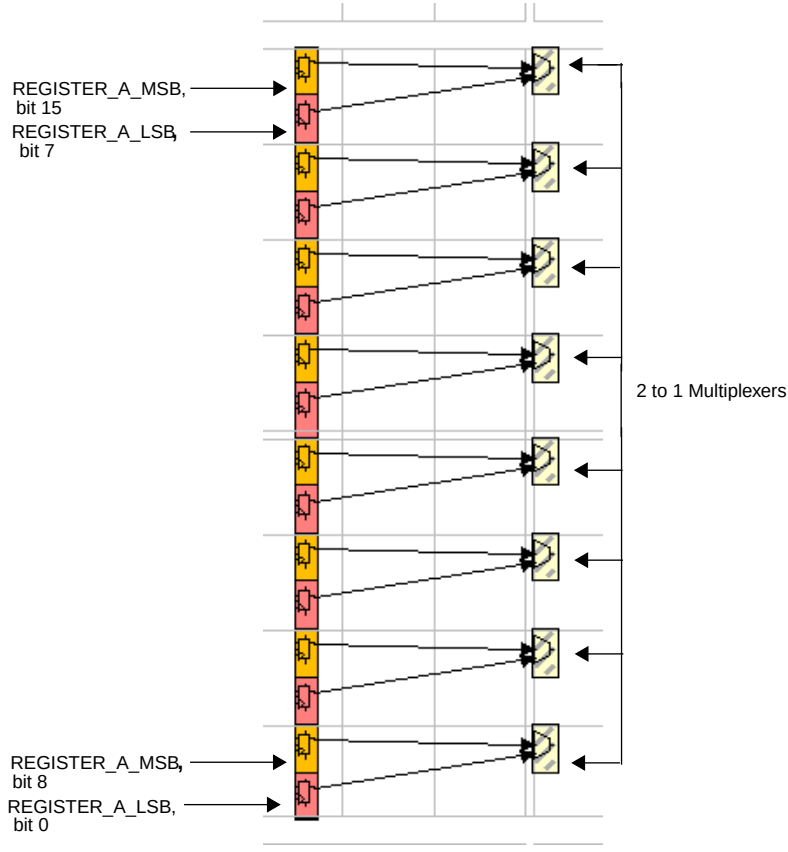


Figure 4-39 Step 5: 2in1 Multiplexers Placed to Align with A/Q Bus

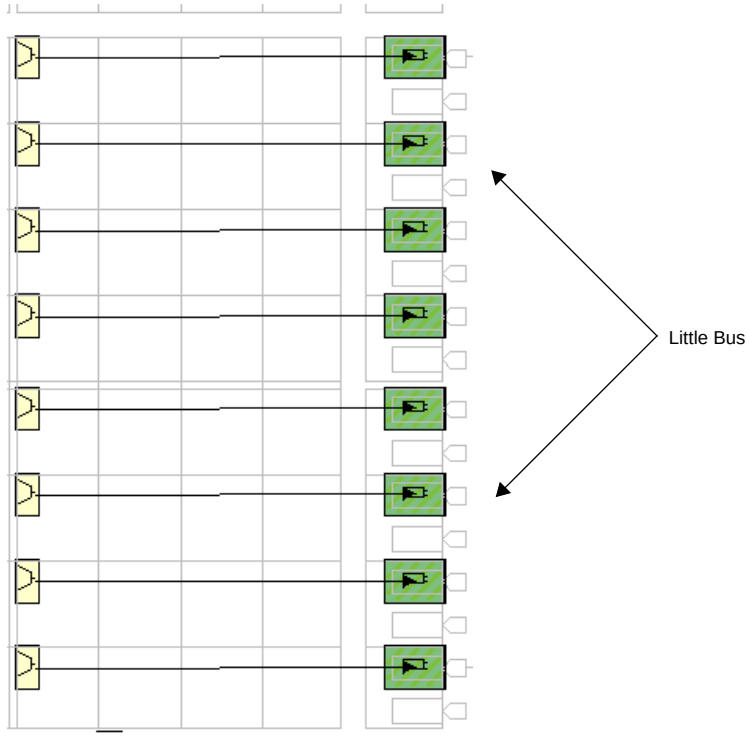


Figure 4-40 Step 6: Little Bus Placed to Align with Multiplexers

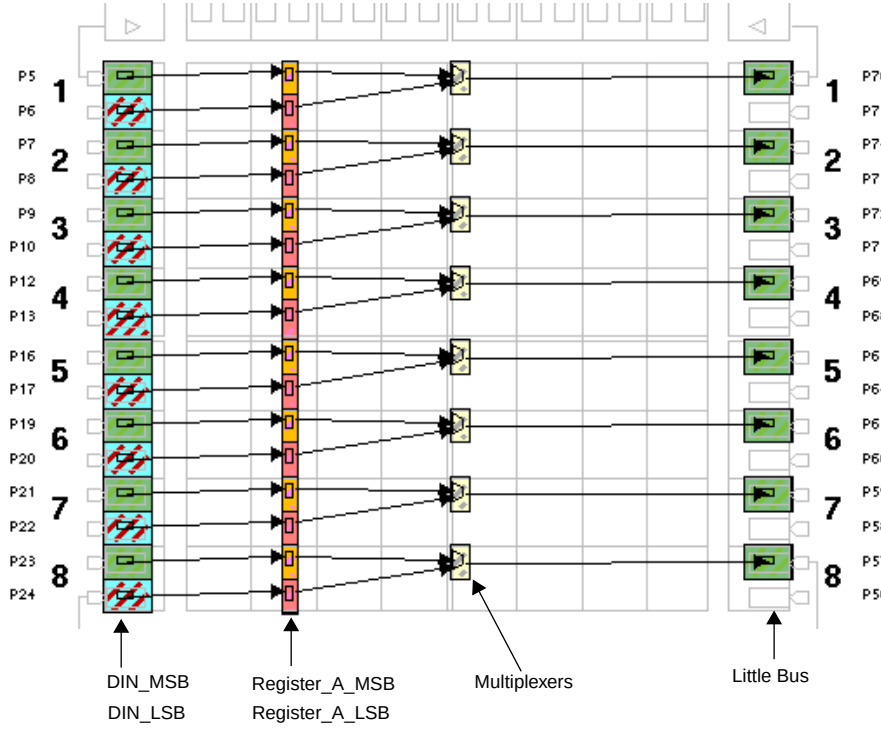


Figure 4-41 Final Placement of Interleave Design

Iterative Floorplanning

This procedure explains how to floorplan your design iteratively. In this method, you manually place the structured logic of the design. Then, run PPR to automatically place the random logic of the design. Repeat this cycle of manual and automatic placement until you have placed the critical paths of the design in the FPGA floorplan.

Perform the following steps to floorplan, iteratively:

1. Work with the most critical path first.
2. From this part of your design, floorplan the structured logic.
3. Next, select the control logic or random logic, if any, and run PPR to place it by selecting the Place command from the Process menu.

When PPR is done, the Floorplanner reads the resulting placed design file. You might want to make changes to the original floorplan and try again, or move on to floorplanning more logic.

Note: Step 4 is optional; it removes the logic placement that PPR has just placed. If you do not do step 4, the placement becomes part of the floorplan, preventing future runs of PPR from finding a more optimum placement for that logic.

4. Use the UnPlace Last command from the Process menu to return the Floorplanner to the state it was in prior to the most recent execution of PPR.

Floorplanning Incremental Schematic Changes

Xilinx defines incremental designing as making changes, at the design entry stage, to a design that has been previously implemented in an FPGA, with or without floorplanning. These changes can include:

- Adding logic
- Removing logic
- Changing existing logic

The following procedure explains only how to make incremental changes when you have used the Floorplanner to floorplan the original design.

Note: This procedure does not apply to HDL designs. For complete details about incremental designs that are HDL-based, refer to the *HDL Synthesis for FPGAs Design Guide*.

Design Example

The schematic-based design has been floorplanned and a change in the design requires that you add of some logic to the original schematic.

1. Make the necessary changes to the schematic design.

Note: Whenever you make changes to the schematic, you must regenerate a new MAP file in order to floorplan.

2. Choose the Open command from the File menu.

This command opens the standard file open dialog box.

3. Select the new MAP file to read in to the Floorplanner.

   The Floorplanner reads in the *design*.fpn. Whenever an FPN file exists for the design, Floorplanner reads it in addition to reading the MAP file. The logic that was floorplanned is again placed into the same location in the Floorplan window.

Figure 4-42, Figure 4-43, and Figure 4-44 show the design example schematic, the design hierarchy of the MAP file, and the floorplanned design, respectively.

Figure 4-42 shows the original schematic of the design example.

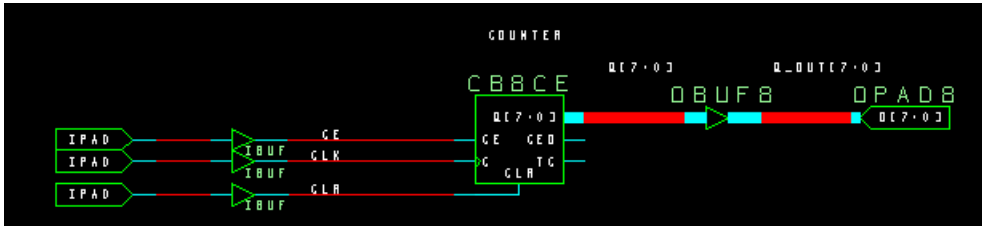


Figure 4-42 Design Example

Figure 4-43 shows the design hierarchy of the example in the Design window.

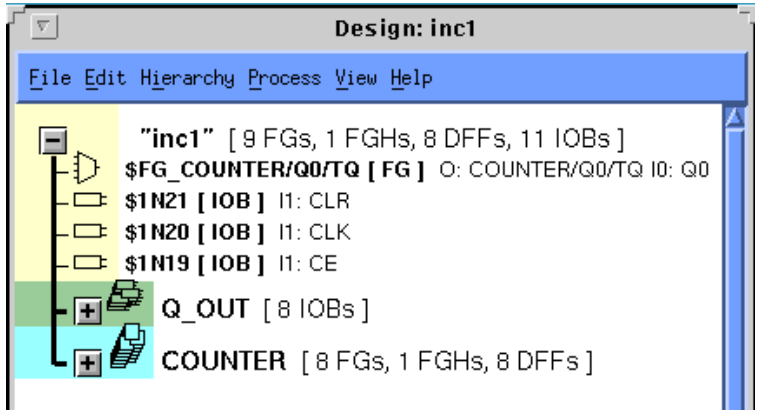


Figure 4-43 Design Example Design Hierarchy

Figure 4-44 shows the floorplanned design example.

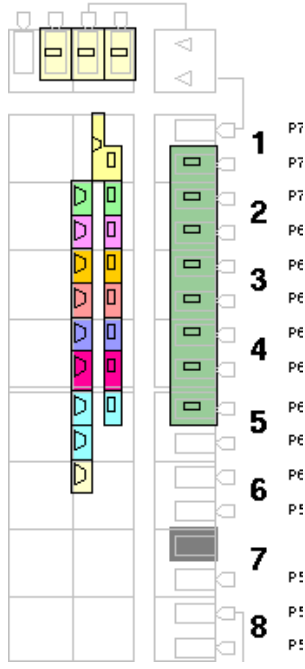


Figure 4-44 Floorplanned Design Example

Figure 4-45 shows the design example schematic that has been modified. A two-input AND gate, an OBUF, and OPAD have been added to the design.

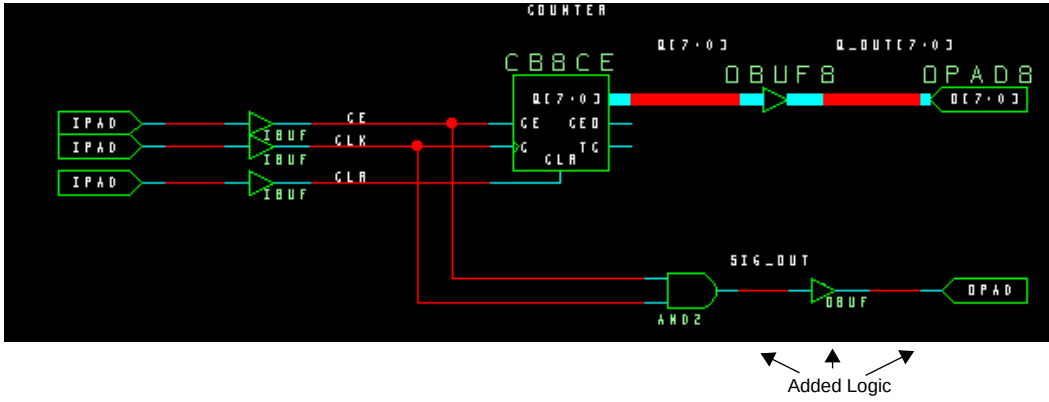


Figure 4-45 Changes to the Original Schematic

When the design is reloaded into the Floorplanner, the newly added logic appears in the Design hierarchy as unplaced since it is not referenced in the FPN file. Refer to Figure 4-46. Two new symbols $1N57 [IOB] and $FG_SIG_OUT [FG] still remain in the hierarchy (as indicated by the logic symbol icon) and may be placed into the floorplan.

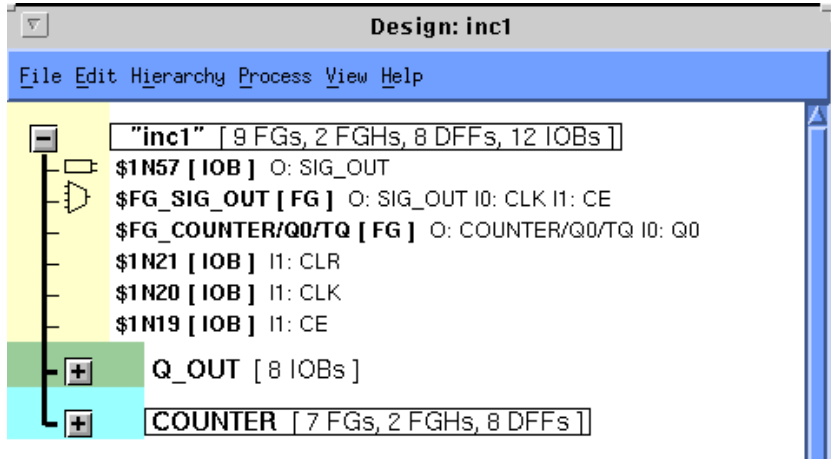


Figure 4-46 Design Hierarchy of New MAP File

Place and Route Incremental Design Changes

Optionally, you can run PPR to place and route the design. You must select the logic that you want PPR to place and route, then follow these steps:

1. Select the Place and Route command from the Process menu to route the design.

   The Process Options dialog box appears on the screen.

2. Choose the desired Placement Effort and Routing Effort by moving the slider bar to the appropriate location.

3. Click the Use Guide File button and enter the path name of the current LCA/PM file in the field.

   PPR uses the existing LCA/PM file of the current design as a guide to routing the unchanged logic in the design.

Setting PPR options in the Floorplanner

This procedure explains how to set PPR options in the Floorplanner. From the Floorplanner interface, you can set the desired levels of placement and routing effort, as well as choose a guide file.

Note: You can select unplaced logic from the Design window and run PPR to place and route it. You can also select placed logic in the Floorplan window and run PPR. Since the logic is already placed, PPR will only route the logic.

1. Select the logic that you want to place or place and route.

2. Select the appropriate PPR command (Place or Place and Route) from the Process menu.

   Either selection displays the Process Options dialog box.

Note: The Routing Effort box is disabled in the Process Options dialog box when you select the Place command.

3. Choose the desired levels for the Placement Effort and Routing Effort with the slider bar.

4. If you are using a guide file, click the Use Guide File button and type in the guide file's path name.

5. Click the OK button.

Routing a Design

This procedure explains how to use PPR from the Floorplanner to route a design. Typically, you want to floorplan the parts of the design that are highly-structured. Use PPR to place and route the less structured parts of the design.

1. In the Design window, select the logic that you want to place and route.
2. Select the Place and Route command from the Process menu.

   The Process Options dialog box appears on the screen.
3. Change the Placement Effort and Routing Effort levels by moving the slider bar if you do not want to use the default settings.
4. If you are using a guide file, click the Use Guide File button and type in the guide file's path name.
5. Click the OK button.

To analyze the results, refer to the procedure, "Analyzing PPR Results" in this chapter.

Getting Started With an Unfamiliar Design

This procedure explains how to use the Floorplanner to familiarize yourself with the connectivity of someone else's design.

There may be occasions when you must floorplan a design with which you are unfamiliar. There are some basic steps you can take to make the floorplanning tasks more efficient.

- View the schematic to understand the structure of the design and data paths.
- Determine the design's structure such as, RAM and buses.
- Try to determine the performance requirements of the design.

When you load a design, the Floorplanner uses net and symbol names to create a design hierarchy. Some designs may contain little information about the hierarchy. For such designs, you could create a fake hierarchy by following these steps:

1. Select the Group By command from the Hierarchy menu.

   This command opens the Group by dialog box.

2. Group columns of tristate buffers, and simple function generator, flip-flop, and tristate buffer relationships.

3. Click the OK button when you are done.

Creating Hierarchy at a Higher Level

To create groups of logic at a higher level, follow these steps:

1. Select the Find Logic command from the Edit menu.

   This command opens the Find Logic dialog box.

2. Use the dialog box find and select all of the IOBs in the design.

3. Create a group of these IOBs using the F3 key, or the Group command from the Hierarchy menu.

   The grouped IOBs appear a stack in the Design window.

4. Expand that stack, then scroll through the list, looking at the pin types on the symbols.

Creating Subgroups

1. Make subgroups of those IOBs with pins named “I” (input IOBs), “O” (output IOBs), and those IOBs with both “I” and “O” pins (bidirectional IOBs).

2. Select the group of input IOBs.

3. Identify the symbols in the group that directly load the new group using either the Select Loads command from Edit menu, or the Find Logic dialog box and choosing the Loading Selected Logic connection.

4. Make a group of those symbols.

5. Repeat steps 3 and 4 to create additional groups of related symbols. Stop when the groups become too large, too small, or too complex to be of value.

Note: Each time you make a subgroup, manually de-select the nodes that have been previously grouped.

6. Next, select the group of Output IOBs.
7. Perform the same sequence (steps 2 through 5) as before, but change the connection type or search criteria to Sourcing Selecting Logic.
8. Each time that symbols are selected, scroll through the lists and adjust the selections as appropriate.

   The goal is to break large groups into more manageable sizes, without creating a large number of small groups.
9. Repeat the process of making subgroups (steps 7 and 8) with the group of bidirectional IOBs, for each direction.
10. If there are other known structures in the design such as RPMs or tristate buffer columns, use them as a starting point for making other subgroups.

Floorplanning the New Hierarchy

Once you have manageable groups of logic for the design, you can begin floorplanning.

1. Floorplan the IOBs.

   Use the Select Loads and Select Sources commands, as well as the Find Logic dialog box to guide you in a systematic manner.
2. Use the ratsnest display in the Floorplan window to identify which symbols need rearranging to reduce interconnect congestion.

Note: A major risk in floorplanning is over-constraining the design.

To reduce the risk of over-constraining the design, you could do the following steps:

1. Floorplan all the logic you can.
2. Select everything except the tristate buffers.

3. Fully expand the hierarchy in the Design window, then click the Stack Icons toolbar button shown in Figure 4-47.

Figure 4-47 Stack Icons Toolbar Button

Clicking the Stack Icons toolbar button, moves the floorplan up one level of hierarchy, such that the logic icons for each hierarchical group are stacked and gives PPR more freedom with which to place and route the design.

Chapter 5

Menu Command Reference

This chapter describes the Floorplanner graphical user interface commands, dialog boxes, and toolbar buttons. The commands are listed in alphabetical order by command name.

Menus

The PC version of the Floorplanner has a menu called Window (for standard basic Windows operations), that is not present on the workstation version. The Edit and View menus contain a different set of commands dependent upon which window (Design or Floorplan) is the active window.

The Floorplan and Hierarchy menus are specific to the Floorplan and Design windows, respectively. When the active window is the Design window, the Hierarchy menu displays on the menu bar. When the Floorplan window is the active window, the Floorplan menu displays on the menu bar.

Note: The dialog boxes shown in this chapter reflect the PC version of the Floorplanner. The different look of the dialog boxes between the PC and workstation platforms is due to the different window environments. The functionality is the same on both platform, though the location of the fields and buttons on the dialog box may vary. The names of some fields may also vary between the PC and workstation versions. For example, on the File Open dialog box, the PC uses File Names while the workstation version uses Files.

File Menu

The File Menu contains commands that open and save designs, read and write constraints files, print and plot floorplanned logic, and exit the Floorplanner. The File menu appears in both the Design and Floorplan windows with the following commands.

Open	Opens a file for processing
Close	Closes windows, unloads current design and floorplan
Save	Creates a floorplan and constraints file
Save As	Creates a floorplan and constraints file under a new design name or design directory
Read Placed Design	Reads placement information from an LCA file or PM file (for XC5200 devices)
Read Constraints	Reads placement information from a constraints file
Write Constraints	Generates a constraints file
Print	Prints out floorplan or design hierarchy
Plot	Plots the floorplan (Workstations only)
Exit	Exits the Floorplanner

Edit Menu

The Edit Menu contains commands that find and select specified logic types and nets in the design, copy and save logic patterns in the floorplan, and change the colors of logic. This menu appears on both the Design and Floorplan windows. The Capture Pattern and Impose Pattern commands appear on the menu when the Floorplan window is the active window. The following commands are in the Edit menu:

Undo	Undoes the last command
Colors	Changes logic and nets colors
Find Logic	Finds and selects logic symbols
Find Nets	Finds and selects design nets

Select Loads	Selects logic connected to outputs of selected logic
Select Sources	Selects logic connected to inputs of selected logic
UnSelect All	Unselects all design logic and nets
Capture Pattern	Copies and saves selected icon pattern
Impose Pattern	Uses saved pattern for logic placement

Hierarchy Menu

The Hierarchy menu contains commands that expand and collapse the hierarchy, group specific logic together; move, rename, and sort hierarchical macros, as well as flatten and rebuild the hierarchy. This menu appears on the menu bar only when the active window is the Design window.

Expand	Expands full branch of hierarchical macros for viewing
Collapse	Collapses selected hierarchical macros
Group	Creates new hierarchical macros containing selected macros
Group By	Creates new hierarchical macros based on connectivity
Remove Group	Removes selected hierarchical macros from hierarchy tree
Move	Uses the mouse to move selected logic to new locations in hierarchy
Rename	Changes a hierarchy macro name
Sort	Changes the order of symbols and hierarchical macros based on sort criteria
Flatten	Removes all sub-hierarchical macros under the selected macro
ReBuild	Uses symbol instance names to build a hierarchy tree

Floorplan Menu

The Floorplan menu contains commands that change the spacing and distribution mode of logic in the floorplan, change the orientation of placed logic, allocate and constrain areas of the floorplan, and remove logic from the floorplan. The Floorplan Menu appears on the menu bar only when the active window is the Floorplan window.

Spacing	Changes spacing of icon stack
Distribute	Sets the distribute mode for icon stack
Stack	Sets the stack mode for icon stack
Flip Vertical	Flips logic symbol placement vertically
Flip Horizontal	Flips logic symbol placement horizontally
Prohibit	Reserves resources on the die to constrain PPR
Allow	Frees up reserved resources on FPGA
Remove	Removes selected logic from the floorplan
Remove All	Removes all logic from the floorplan

Process Menu

The Process Menu contains commands to check design rule on the floorplanned logic, run PPR and modify floorplanned logic. The Process menu appears in both the Design and Floorplan windows.

Check Floorplan	Performs design rule checks on floorplanned logic
Place	Runs PPR (placement only) on selected and floorplanned logic
Place and Route	Runs PPR on selected logic using specified options
UnPlace Last	Undoes all changes to floorplan made by last reading of placed design file

View Menu

The View menu appears in both the Design and Floorplan windows, but contains different commands.

Design Window

The commands in the Design window refresh the screens, and scroll the design hierarchy.

Refresh	Clears and redraws all open windows
GoTo Next	Scrolls next selected logic to the top of Design window
GoTo Previous	Scrolls previously selected logic line to top of Design window
Icon Stacks	Toggles three-dimensional view of hierarchical node icons

Floorplan Window

The commands in the Floorplan window refresh the screens, adjust the view of the FPGA die, displays logic resources in the die, display connectivity lines (ratsnest), show routing density, and enable the toolbar.

Refresh	Clears and redraws all open windows
Zoom Full View	Shows the entire FPGA
Zoom In	Reduces the FPGA view area (objects get bigger)
Zoom Out	Enlarges the FPGA view area (objects get smaller)
Zoom To Box	Uses mouse to specify the FPGA view area
Zoom To Selected	Sets the FPGA view area so that all selected logic is visible
Resources	Controls resource graphics display in the die.
Ratsnest	Controls the display of ratsnest connection lines

Congestion	Displays the probable routing density in Floorplan window
Flashing	Toggles the flashing of selected logic borders
Tool Bar	Toggles the presence of toolbar at top of Floorplan window

Window Menu

The Window menu is available only on the PC and contains commands that are specific to window operations in the PC environment, which include tiling, cascading, sizing, and minimizing the Floorplanner windows, as well as changing the active window.

Tile	Arranges windows so that they do not overlap
Cascade	Arranges windows in an overlapping pattern with title bars visible
Arrange Icons	Arranges minimized windows in rows
Window Design	Makes Design window the active window
Window Floorplan	Makes Floorplan window the active window

Help Menu

The Help Menu appears on both the Design window and Floorplan window and contains commands that the open the online help, search on specified topics, and give copyright information about the Floorplanner. Available on the PC only is a command to invoke the online interactive tutorial.

Contents	Open the online help for the Floorplanner
Search for Help on	Open search list topics
Tutorial	Invokes the online interactive tutorial
About Floorplanner	View copyright information for the Floorplanner

Commands

The following section describes the commands and assoicated dialog boxes that are available in the Floorplanner.

About Floorplanner (Help Menu)

This command opens the About XACT Floorplanner dialog box, which presents copyright and logo information.

Allow (Floorplan Menu)

This command allows you to use the mouse to make available those resources in the FPGA that were marked prohibited.

You invoke the command, then click or drag the mouse on the resources in the Floorplan window that you want to make available.

Arrange Icons (Window Menu)

This command arranges the minimized Design and Floorplan window icons in the lower left quadrant of the XACT-Floorplanner window on the PC.

Cascade (Window Menu)

This command arranges the open windows diagonally down the screen so that they overlap one on top of another. The active window is on top.

Capture Pattern (Edit Menu)

This command makes a copy of the currently selected logic icon pattern, and saves it as the "reference" pattern. The reference pattern represents the relative placement and spacing of individual pieces of floorplanned logic.

You can impose this reference pattern onto other logic of similar makeup, using the Impose Pattern command or the Impose Pattern toolbar button.

The Floorplanner saves the reference pattern as a list, in the same order that the selected symbols are found in the Design window. When you use this command to capture a pattern, the Floorplan Impose Pattern menu and toolbar buttons become enabled.

Check Floorplan (Process Menu)

This command checks the floorplanned logic for the following design rules:

- Tristate buffers with common outputs are aligned horizontally
- No tristate buffers with different outputs lie on the same horizontal longline
- Flip-flops in a single CLB tile have common CLK, CE, RD, and SD signals
- Two 16-bit memory elements in a CLB tile share their write enable inputs
- FG to FGH function generator connections are valid

If there are errors in the floorplanned logic, the Floorplanner opens the Check Floorplan Warnings dialog box shown in Figure 5-1. Consult the error descriptions to pinpoint the logic responsible for each error in both the Design and Floorplan windows.

Figure 5-1 Check Floorplan Warnings Dialog Box

A description of the fields and buttons on the dialog box follow.

Warning Messages

Lists warnings found while checking the floorplan. You can scroll through this list. Double-clicking on an item causes the Floorplanner to zoom the Floorplan window to the problem area.

Find

Finds the warnings when you click the button. The Floorplan and Design windows zoom and pan to the logic causing the current warning. This is the default.

ReCheck

Reinitiates the placement checks, and updates the warning messages to the results. Use this button to recheck the floorplan as you fix the problems causing the errors and warnings.

Close

Closes the dialog box.

Help

Opens the online help for the dialog box.

If the Floorplanner detects no errors, the Check Floorplan Dialog Box shown in Figure 5-2 appears, indicating that the current floorplan passes all placement checks.

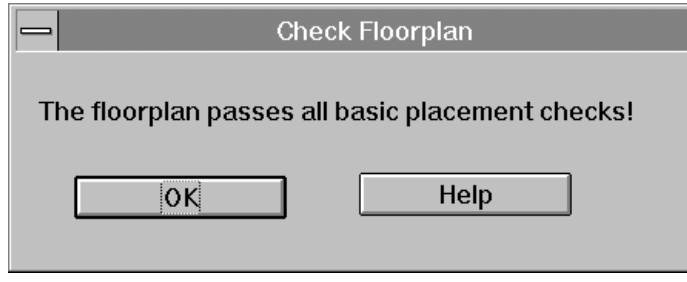


Figure 5-2 Check OK Dialog Box

OK

Closes the dialog box.

Help

Opens the online help for this dialog box.

Close (File Menu)

This command closes the Design and Floorplan windows. Close frees up all memory associated with the current (loaded) design. If you have edited either the floorplan or hierarchy since the last Open or Save command, Close opens the dialog box shown in Figure 5-3 and prompts for confirmation before closing the design.

Figure 5-3 Confirmation Dialog Box

A description of the buttons on the dialog box follow.

The dialog box displays the following message:

```
Floorplan was modified,
Do you want to save changes?
```

Yes

Closes the dialog box, and saves the floorplan under the same name as the loaded design.

No

Closes the dialog box and the design. All changes made to the design hierarchy and the floorplan are lost.

Cancel

Closes the dialog and allows you to continue with the current floorplanner session.

Help

Opens the online help for this dialog box.

Collapse (Hierarchy Menu)

This command collapses the selected, expanded hierarchical macros in the Design window so that the sub–hierarchy is no longer visible. Logic icons that represent the lower hierarchical levels appear to the left of the text line for the collapsed logic in the Design Hierarchy window.

Colors (Edit Menu)

This command opens the Colors dialog box shown in Figure 5-4, where you change the color associated with logic or nets. The dialog box shows the current color that is assigned to a particular logic node or net. Use the Color Select region to change from one color to another.

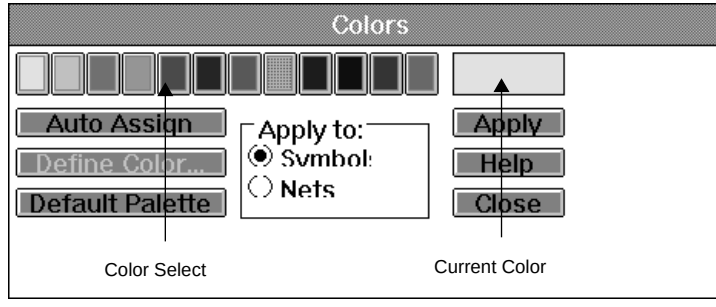


Figure 5-4 Colors Dialog Box

A description of the buttons on the dialog box follow.

Current Color

Shows the color of the currently selected color button.

Color Select

Causes the Floorplanner to use that color when you click the Apply or Define Color buttons. There is one button for each available color.

Auto Assign

Automatically assigns colors to all selected logic nodes. The Floorplanner sequentially assigns colors to hierarchical nodes, and assigns symbols the color of their parent.

Default Palette

Sets all Color Select buttons to their default colors.

Apply to Symbols

Causes the Floorplanner to apply the color changes to the selected logic symbols or hierarchical macros when you click the Apply button.

Apply to Nets

Causes the Floorplanner to apply the color changes to the selected nets and their ratsnest lines in the Floorplan window when you click the Apply button.

Help

Opens the online help for this dialog box.

Apply

Sets the color of all currently selected logic or nets to the currently chosen Color Select Button, based on the selection status of the Nets and Symbols settings.

Close

Closes the Colors dialog box.

Define Color

Opens the Define Color dialog box shown in Figure 5-5 where you edit the RGB (Red, Green, Blue) definitions that are associated with the currently chosen Color Select button.

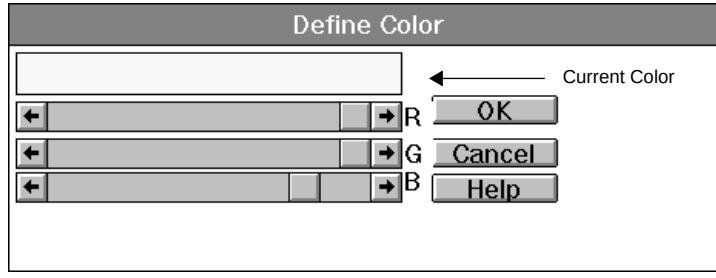


Figure 5-5 Define Color Dialog Box

A description of the fields and buttons on the dialog box follow.

Current Color Field

Shows the color of the currently selected color button.

R Slider Bar

Sets the red component of the color.

G Slider Bar

Sets the green component of the color.

B Slider Bar

Sets the blue component of the color.

OK

Closes the dialog box, making the color changes you indicated.

Cancel

Closes the dialog box without changing colors.

Help

Opens online help for the dialog box.

Congestion (View Menu)

This command puts the Floorplan window into the congestion map display mode, or restores it to the normal mode of display.

The congestion map mode shown in Figure 5-6 gives you information about the congestion of each tile in the FPGA. Congestion is defined as the probable routing density for each CLB tile.

Use the slider bar on the Congestion Contrast dialog box to adjust the color display of the congestion graph, located in the upper left quadrant of the Floorplan window. Above the congestion graph, on the Floorplan window is the maximum and average values of the routing densities through the CLBs that have placed logic.

Use this command to help locate routing problems in the design or, for when the design does not meet specified timing requirements.

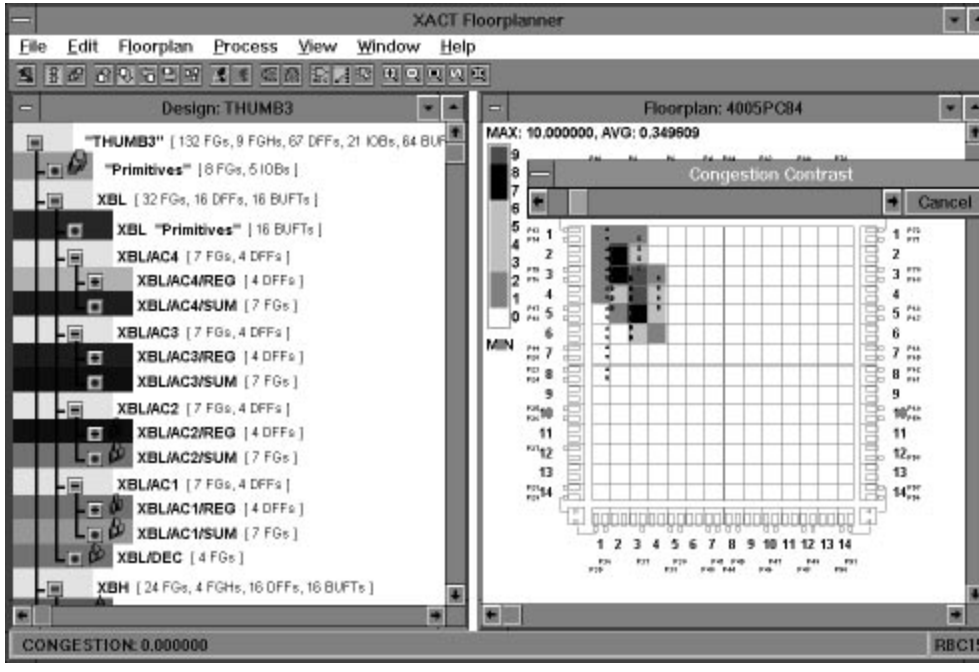


Figure 5-6 Congestion Mode Display

Contents (Help Menu)

This command opens the online help facility for the Floorplanner and initially displays the contents page of the online help.

The contents page is the first page of the online help and lists the available subjects. From this page you can access the online help topics, including command descriptions and procedures, look up glossary terms, search on keywords, and use bookmarks.

Design (Window Menu)

This command puts the Design window in the front of the screen display and gives this window the keyboard focus.

Distribute (Floorplan Menu)

This command sets the distribute mode for dropping a stack of logic icons in the Floorplan window. In this mode, the Floorplanner sequentially assigns single resource locations for each logic icon.

The allocation direction can be up, down, left, right, or spot. The spot direction allows you to select and drop only one logic icon at a time, allowing you to manually pick the locations one by one.

You set the allocation direction using the four allocation direction toolbar buttons in the toolbar. You can also choose the spacing (number of resources) that the Floorplanner uses to lay out the selected logic icons.

The Floorplanner associates the first logic icon with the resource in the Floorplan window at the current mouse pointer location. The next logic icon, and subsequent logic icons thereafter, are associated with resources located above, below, to the right or left of the current mouse pointer location, depending on the allocation direction.

The Floorplanner distributes the selected logic icon stacks until it either reaches an edge of the FPGA, encounters an obstruction from previously placed logic, or until it uses all the selected logic icons.

If you stop the layout and have not used all of the logic icons in transit (selected logic icons that are to be moved from the Design window to the Floorplanner window), these logic icons remain in transit. You must find another location for the placement of these logic icons.

Distribute also distributes any selected logic that you previously floorplanned using the stack mode.

Expand (Hierarchy Menu)

This command expands all currently selected hierarchical macros so that the sub–hierarchical levels and symbols display in the Design window.

Expand fully expands the hierarchical branches to the lowest level. It recursively expands all selected hierarchical macros until the symbols display in the Design window.

Exit (File Menu)

This command exits the Floorplanner. If you have edited the data in your design since the last Open or Save commands, the Floorplanner opens a dialog box shown in Figure 5-7 which prompts you for confirmation before termination.

The dialog box displays the following message:

```
Do you want to save changes
to the current floorplan?
```

Figure 5-7 Confirmation Dialog Box

A description of the fields and buttons on the dialog box follow.

Yes

Saves the changes you have made to the design hierarchy and floorplan in an FPN file and exits the Floorplanner.

No

Exits the Floorplanner without saving the changes you have made to the design.

Cancel

Closes the dialog box and allows you to continue in the current floorplanning session.

Help

Opens the online help for this dialog box.

Find Logic (Edit Menu)

This command opens the Find Logic dialog box shown in Figure 5-8 where you select the criteria that you want the Floorplanner to use when finding logic symbols in the design hierarchy and Floorplan window. Use this command to help find specific logic symbols and hierarchical macros.

When you click the Apply button, the Floorplanner finds those logic symbols that meet all the criteria that you have defined.

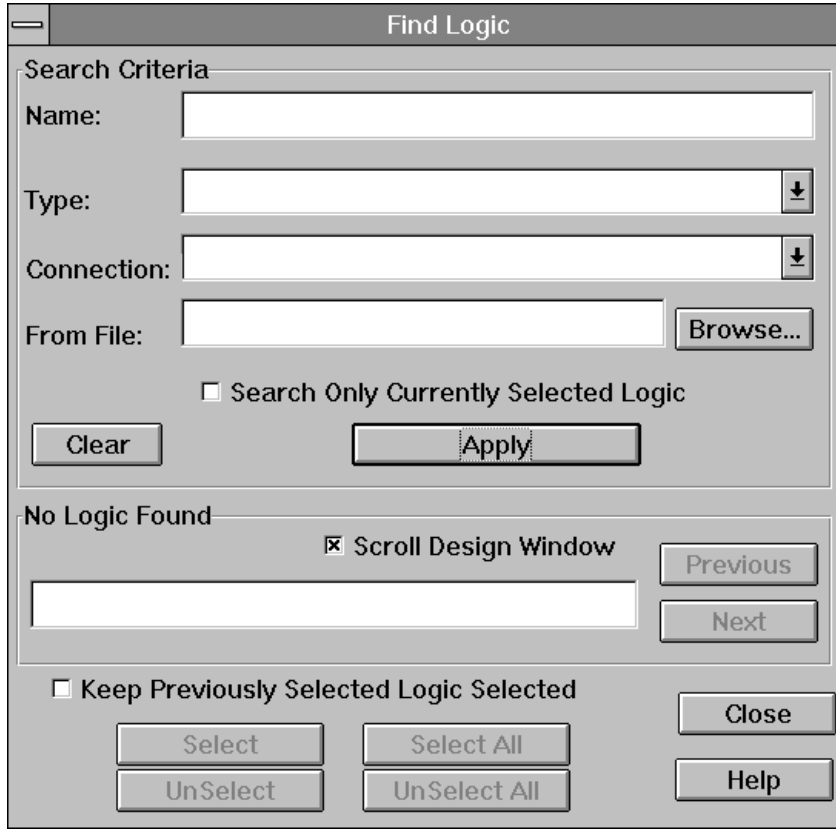


Figure 5-8 Find Logic Dialog Box

A description of the fields and buttons on the dialog box follow.

Name

Finds only symbols that have instance names matching a user-entered pattern. You can use the standard wildcards, "*" and "?."

Type

Finds a particular type of symbol. Valid symbol types are:

- blank (default, no type indicated)
- Hierarchical Groups

- I/O
- CLBs (XC3000A parts only)
- Function Generators (XC4000 and XC5200 parts only)
- Flip Flops (XC4000 parts only)
- Flip Flops or Latches (XC5200 parts only)
- Tristate Buffers
- RAM/ROM (XC4000, except XC4010D)
- Global Buffers (XC4000 and XC5200 parts only)
- Carry logic (XC4000 and XC5200 parts only)

Note: The Floorplanner finds Hierarchical Groups if their names match the "name" criteria, and if the group contains symbols that match the Connection and From File criteria.

Connection

Finds only symbols that are connected to currently selected symbols or nets. Valid connections are:

- blank (default, no connection criteria is indicated)
- Driving Selected Logic

  Finds logic that has outputs directly connected to inputs of selected logic.
- Loading Selected Nets

  Finds logic that has inputs directly connected to selected nets.
- Loading Selected Logic

  Finds logic that has inputs directly connected to outputs of selected logic.
- Driving Selected Nets

  Finds logic that has outputs directly connected to selected nets.
- Common Outputs (BUFTs)

  Finds all BUFTs with the same output net as the selected BUFTs.

- Common Enables (BUFTs, IOBs, DFFs, RAM) for XC4000 only

  Finds all similar symbols with the same enable net as the selected symbols.

- Common Enables (BUFTs, DFFs, DLATs, IO) for XC5200 only.

  Finds all similar symbols with the same enable net as the selected symbols.

From File

Finds only symbols that have instance names matching names in a designated text file. You can type the file name or click the Browse button to bring up the standard File Open dialog box from which you can select a file.

Search Only Currently Selected Logic

Finds only symbols that are currently selected when you enable this feature. It allows you to preselect logic of interest, then apply criteria selection to only that logic.

Clear

Clears all search criteria controls.

Apply

Searches for the logic symbols that meet the selection criteria you have chosen and marks those symbols or hierarchical macros as found. If you enable Scroll Design Window, it scrolls the Design window to the first item found.

Symbols Found

Displays the name of one currently found symbol or hierarchical node. If no logic is found, a message stating this appears in this area. If logic is found, the name of this area changes to "# Symbols Found"or, "# Groups Found;" the name of the first occurrence of that logic appears in this box.

Scroll Design Window

Automatically scrolls the Design window to the item indicated in the Symbols Found box whenever you click the Apply, Next, or Previous buttons. It also temporarily expands hierarchical macros in Design window as necessary, to display the item.

Previous

Displays the name of the previously found item.

Next

Displays the name of the next found item.

Keep Previously Selected Logic Selected

Keeps previously selected logic selected after you have clicked the Select or Select All buttons. If you do not check this box, only the logic that meets the selection criteria remains selected.

Select

Selects the currently found item, which is displayed.

Select All

Selects all found items. If Keep Previously Selected Logic Selected is not used, all logic other than the one that meets the search criteria is deselected.

UnSelect

Deselects the currently found item. This feature is enabled only when there is a name of selected logic displayed in the display area.

UnSelect All

Deselects all found items.

Close

Closes the dialog box.

Help

Opens the online help for the dialog box.

Find Nets (Edit Menu)

This command opens the Find Nets dialog box shown in Figure 5-9 where you can select the desired criteria that the Floorplanner uses to find design nets. The Find Nets command also automatically opens the Ratsnest dialog box. See the Ratsnest command for details.

When you click the Apply button, the Floorplanner finds the nets that meet all the criteria you have chosen.

One use of this command involves the ratsnest display in the Floorplan window. With the ratsnest display on, you can use Find Nets to locate a specific net. Then, to make that particular net more visible, you can change its color with the Colors command.

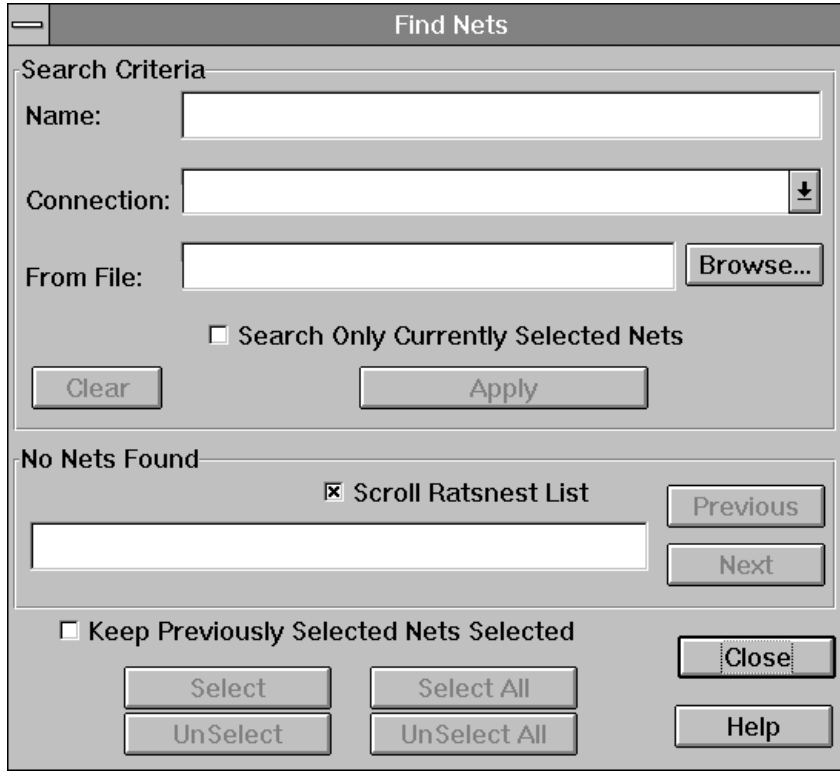


Figure 5-9 Find Nets Dialog Box

A description of the fields and buttons on the dialog box follow.

Name

Finds only the nets that have names matching a user-entered pattern. You can use the standard wildcards, "*" and "?".

Connection

Finds only the nets that are connected to the currently selected symbols. The following connection types are available:

- blank (default, no connection criteria is indicated)
- Within Selected Logic

  Finds nets that have at least two pins connected to the selected logic.
- Into Selected Logic

  Finds nets that have at least one pin connected to the selected logic, and at least one pin connected to the non-selected logic.
- Sourcing Selected Logic

  Finds nets that are directly connected to the inputs of selected logic.
- Driven by Selected Logic

  Finds nets that are directly connected to the outputs of selected symbols (or logic).

From File

Finds only nets with instance names that match the names in a designated text file. You can type the file name in the edit box, or click the Browse button to bring up a standard file open dialog box. For example, from the dialog box, you can choose a file listing unrouted nets or nets that are listed from the Timing Analyzer.

Search Only Currently Selected Nets

Finds only nets that are currently selected. You can preselect nets and apply search criteria to only those nets. If this is the only criteria selection you make, you can scan through all previously selected nets.

Clear

Clears all criteria controls.

Apply

Searches for the nets that meet the selection criteria you have chosen and marks those nets as found. If you have checked “Scroll Ratsnest List” it scrolls the Ratsnest Available Nets List to the first item that is selected.

Nets Found

Displays the name of one currently found net in the Find Nets. If nets are found, the name of this area changes to “# Nets Found.”

Scroll Ratsnest List

Scrolls the Available Nets list in the Rastnest dialog box to the item in the Nets Found box, each time you click the Apply, Next, or Previous buttons. Enabling this feature opens the Rastnest dialog box and puts it in the foreground.

Keep Previously Selected Nets Selected

Keeps previously selected nets selected after clicking the Select or Select All buttons. If you do not check this box, only those nets that meet the selection criteria remain selected.

Select

Selects the currently found net, visible in the Found Net box.

Select All

Selects all found nets. If you do not use Keep Previously Selected Nets Selected, all nets other than those which were found are deselected.

UnSelect

Deselects the currently found net, visible in the Found Nets box. Enabled only when there is a name of a selected net present the in Found Nets box.

UnSelect All

Deselects all found items.

Close

Closes the dialog box.

Help

Opens the online help for the dialog box.

Flashing (View Menu)

This command allows you to turn on and off the flashing borders of selected logic in the Floorplan window. Selected logic in the Floorplan window, by default, displays with its borders flashing.

Flatten (Hierarchy Menu)

This command flattens the selected portions of the design by removing hierarchical names from the lower-level logic, moving all associated symbols up the hierarchy so that their parent is the highest level selected marco. This command is enabled only when you have selected hierarchical macros.

Flip Horizontal (Floorplan Menu)

This command flips the selected floorplanned logic symbols so that symbols on the left move to the right; and the symbols on the right move to the left.

If you use this command on selected floorplanned logic that is not in transit, that logic is flipped in place.

Flipping symbols in the Floorplan window does not affect the design hierarchy.

Flip Vertical (Floorplan Menu)

This command flips the selected floorplanned logic symbols so that the symbols at the top move to the bottom, and the symbols at the bottom move to the top. If you use this command on selected floorplanned logic that is not in transit, that logic is flipped in place.

Flipping symbols in the Floorplan window does not affect the design hierarchy.

Floorplan (Window Menu)

This command puts the Floorplan menu at the front of the screen and gives this window the keyboard focus.

GoTo Next (View Menu)

This command scrolls the Design window to bring the first or next selected line in the hierarchy to the top of the window.

GoTo Previous (View Menu)

This command scrolls the Design window to bring the previously selected line in the hierarchy to the top of the window.

Group (Hierarchy Menu)

This command creates a new hierarchical group in the design. The Floorplanner places the new group into the hierarchical display in the Design window and moves all the selected symbols and logic into that new group.

The Floorplanner assigns an arbitrary name to the new group, GRP*n.* Successive new user-created groups are name GRP*n*+1. You should rename any new group with a more meaningful name using the Rename command from the Hierarchy menu.

Use this command when you want to work with tightly coupled logic as a unit. For example, you might have a group of flip-flops that drive a group of tristate buffers. It might make more sense to work with a single group composed of flip-flops and tristate buffers than it does to work with a group of flip-flops and a group of tristate buffers.

Other examples for user-created groups are:

- Group all the flip-flops that go into a counter
- Group BUFTs that have the same output signal
- Group D flip-flops that drive BUFTs
- Group function generators that drive D flip-flops
- Group function generators, flip-flops, and other state machine logic together, define an area in the floorplan for that group

Group by (Hierarchy Menu)

This command opens the Group by dialog box where you create new hierarchical macros based on the direct connectivity between function generators, flip-flops, BUFTs, and CLBs, You can also create new groups based on tristate buffers with common enable or output signals.

Use this command when you want to work with tightly coupled logic as a unit.

For example, you could use the Tristate Buffers with Common Enable Inputs option to build a group that represents a column of BUFTs.

Next, you could use the Function Generators to Tristate Buffers option to create a set of groups that contain those pairs, within the first grouping.

Then, you could use the Function Generators to Flip Flops option to create groups of those pairs.

The final result would be groups of function generators and flip-flop pairs that are grouped with BUFTs, all of which are grouped into the original BUFT column.

Figure 5-11, Figure 5-12, and Figure 5-12 show the dialog boxes for the XC5200, XC4000, and XC3000 families, respectively.

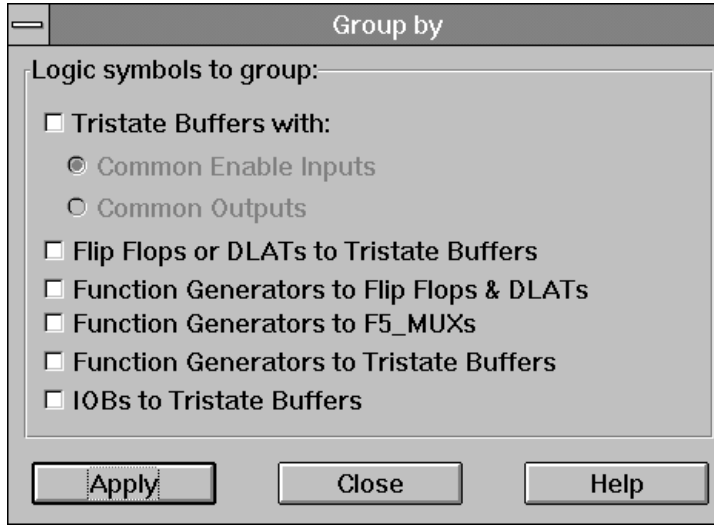


Figure 5-10 Group by Dialog Box for the XC5200 Family

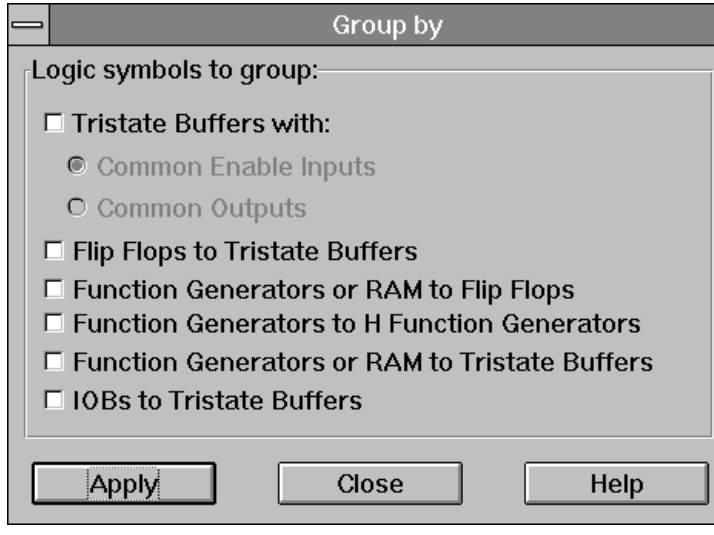


Figure 5-11 Group by Dialog Box for the XC4000 Family

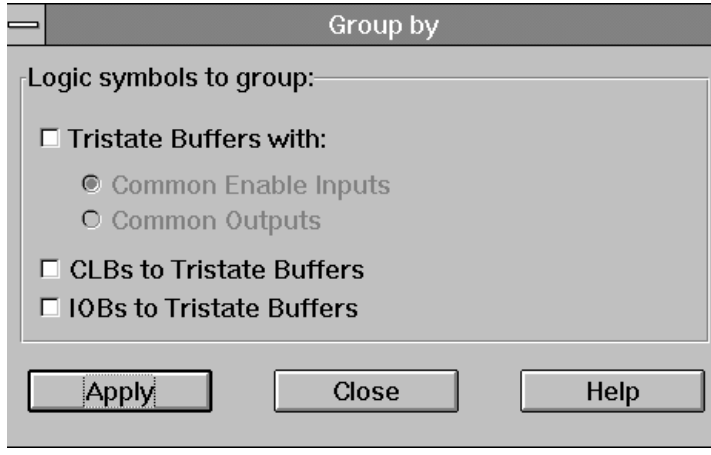


Figure 5-12 Group by Dialog Box for the XC3000 Family

A description of the fields and buttons on the dialog box follow.

When you select more than one group, the Floorplanner creates the groups in the order that they appear on the dialog box.

Tristate Buffers with Common Enable Inputs

Creates groups of tristate buffers that have the same net connected to their output enable pin. The new group is placed nearest to the common parent for all tristate buffers in the group.

The new grouping corresponds to columns of BUFTs in the FPGA architecture. This function is mutually exclusive with the Tristate Buffers with Common Outputs group.

Tristate Buffers with Common Outputs

Creates groups of tristate buffers that all have the same net connected to their output pins. The Floorplanner places the new group in the hierarchy so that the parent hierarchical node is the nearest common parent for all tristate buffers in the group.

The new grouping corresponds to rows of BUFTs in the FPGA architecture. This function is mutually exclusive with the Tristate Buffers with Common Enable Inputs group.

Flip Flops to Tristate Buffers

Creates groups of flip-flop to tristate buffer pairs. The flip-flop drives the primary input of the tristate buffer. The Floorplanner places the new groups in the hierarchy so that the parent hierarchical nodes are nearest the original tristate buffer parent hierarchical node.

This button is only available for the XC4000 family.

Flip Flops or DLATs to Tristate Buffers

Creates groups of flip-flop to tristate buffer pairs or DLAT to tristate buffer pairs. The tristate buffer is driven by the flip-flop or DLAT. The Floorplanner places the new groups in the hierarchy so that the parent hierarchical nodes are nearest the original tristate buffer parent hierarchical node.

This button is only available for the XC5200 family.

Function Generators or RAM to Flip Flops

Creates groups of function generator and flip-flop or, RAM and flip-flop pairs, in which the function generator or RAM drives the D input of the flip-flop. The Floorplanner places the new groups in the hierarchy so that their parent hierarchical nodes are nearest the original flip-flop parent hierarchical node.

This button is only available for the XC4000 family.

Function Generators to Tristate Buffers

Creates groups of function generator and tristate buffer pairs, in which the function generator drives the primary input of the tristate buffer. The Floorplanner places the new groups in the hierarchy so that their parent hierarchical nodes are nearest the original flip-flop parent hierarchical node.

This button is only available for the XC5200 family.

Function Generators to Flip-Flops & DLATs

Creates groups of function generator and flip-flop and DLATs pairs, in which the function generator drives the D input of the flip-flop. The Floorplanner places the new groups in the hierarchy so that their parent hierarchical nodes are nearest the original flip-flop parent hierarchical node.

This button is only available for the XC5200 family.

Function Generators to H Function Generators

Creates groups of function generator pairs or triplets in which the function generator is an H-type function generator and the other function generators have their outputs directly and exclusively connected to the H-type function generator inputs. The Floorplanner places the new groups in the hierarchy so that their parent hierarchical nodes are nearest the original H function generator parent hierarchical node.

This button is only available for the XC4000 family.

Function Generators to F5_MUXs

Creates groups of function generators and F5_MUX pair in which the F5_MUX output is directly connected to the function generator. The Floorplanner places the new groups in the hierarchy so that their parent hierarchical nodes are nearest the original H function generator parent hierarchical node.

This button is only available for the XC5200 family.

Function Generators or RAMS to Tristate Buffers

Creates groups of function generator (RAM) and tristate buffer pairs in which the function generator drives the primary input of the tristate buffer. The Floorplanner places the new groups in the hierarchy so that their parent hierarchical nodes are nearest the original tristate buffer parent hierarchical node.

This button is only available for the XC4000 family.

CLBs to Tristate Buffers

Creates groups of CLB to tristate buffer pairs or triplets in which the CLB drives the primary input of the tristate buffer. The Floorplanner places the new groups in the hierarchy so that their parent hierarchical nodes are nearest the original tristate buffer parent hierarchical node.

This button is only available for the XC3000 family.

IOBs to Tristate Buffers

Creates groups of IOB-to-Tristate buffer pairs in which the IOB drives the primary input of the tristate buffer. The Floorplanner places the new groups in the hierarchy so that their parent hierarchical nodes are nearest the original tristate buffer parent hierarchical node.

Apply

Creates the types of groups you have indicated from selected logic and places them in the appropriate location in the design hierarchy, as indicated in the previous descriptions.

Close

Closes the dialog box.

Help

Opens the online help for the dialog box.

Icon Stacks (View Menu)

This command toggles the three dimensional aspect in presenting icons for hierarchical macros.

Icon Stacks gives you a visual estimate of the number of symbols in a particular hierarchical macro.

At times, you might not want to see the size of the icon stack; this command allows you to toggle it off for a clearer view.

Impose Pattern (Edit Menu)

This command imposes a relative placement upon the logic currently in transit or selected, that corresponds to the reference pattern, saved with the Capture Pattern command. You can also use this command on logic that is already placed in the Floorplan window.

The Floorplanner imposes the reference pattern upon the transitory logic by matching symbol for symbol in the order they are found in the Design window.

This command is disabled until you use either the Capture Pattern command or Capture Pattern toolbar button to make a pattern.

Move (Hierarchy Menu)

This command allows you to use the mouse to designate a location within the hierarchy tree to where the Floorplanner moves all selected macros and symbols.

When you select this command, the mouse pointer appears as a thick horizontal line that lies between lines of text in the Design window. This "node move" cursor indicates that the mouse is in the mode of designating the location.

You complete the move of the selected logic to the desired location (indicated by the cursor) by clicking the mouse button. You can cancel the move with the ESC key.

Use this command to reorganize symbols for placement into the Floorplan window using the distribute mode.

Open (File Menu)

This command opens the standard File Open dialog box shown in Figure 5-13 (workstations) and Figure 5-14 (PCs). Choose from a list of MAP files that you want to load into the Floorplanner.

The Floorplanner reads the selected MAP file and opens a Design window for that design, as well as a Floorplan window, based on the device and package file specified in the design. The Floorplanner also reads any floorplan (FPN) or constraints (CST) files of the same name, if they are present in the directory of the selected MAP file.

Note: The dialog boxes shown in Figure 5-13 and Figure 5-14 are also invoked by the Read Placed Design, Read Constraints, Write Constraints, and Save As commands. The defaults for the dialog box name and file extensions change depending upon which command you invoke.

Figure 5-13 Open Command Dialog Box for Workstations

A description of the fields and button on dialog box for workstations follow.

Filter

Contains the character string that controls which file names appear in the Files list. Use the keyboard to edit the path name.

Directories

Lists the directories accessible from the current directory. You can change the current directory by double-clicking in this list.

Files

Lists all the files (in alphanumeric order) in the current directory that match the pattern shown in the Filter box.

Select design file

Contains the file name that the Floorplanner loads when you click the OK button. Load the file by double-clicking on a file name in Files or typing in the file name.

OK

Closes the dialog box and loads the selected design file.

Filter

Applies the file extension you specified in the Filter box when reloading the files list in Files and lists those files.

Cancel

Closes the File Open dialog box without opening the file.

The File Open dialog box for the PC is shown in Figure 5-14.

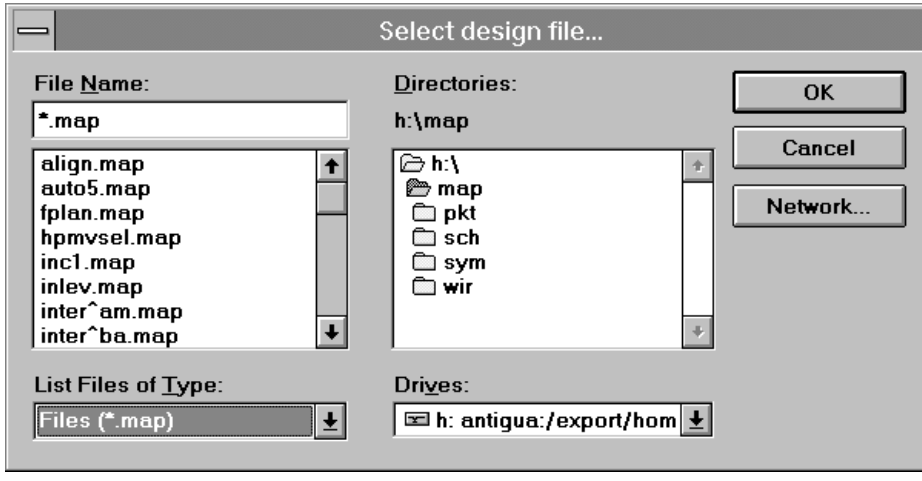


Figure 5-14 Select Design File Dialog Box (PCs)

A description of the fields and button on the dialog box for the PC follow.

File Name

Displays the file extension that is currently selected in the List Files of Type box. You can edit the type of file name you want to search.

Directories

Lists the directories accessible from the current directory. You can change the current directory by double-clicking in this list.

List Files of Type

Lists all the files (in alphanumeric order) in the current directory that match the pattern shown in File Name.

Drives

Shows the current drive that is selected. Lists the drives that are available to use. Click the arrow to display the list. When you select a drive, the software updates the information in the Directories box.

OK

Closes the dialog box and loads the selected design file.

Cancel

Closes the dialog box without opening the file.

Network

Accesses the network drive. This option is only available if you are running Windows for Workgroups.

Place (Process Menu)

This command opens the Process Options dialog box and runs PPR to place selected logic into the Floorplan window. Place generates a design file that represents floorplanned and selected logic, and a constraints file that represents the floorplanned logic.

Place runs PPR from the Process dialog box using the currently designated PPR options for that design, including the optional use of any existing LCA file from previously placed or placed and routed parts of the design as a guide.

When PPR completes, Place reads the resulting LCA file and updates the floorplan to reflect the results of PPR on the selected logic. Refer to the PPR Chapter in the *Development System Reference Guide*, Volume II for more details about PPR.

This command is enabled only when there is selected logic.

Use the Process Options dialog box shown in Figure 5-15 to choose the desired placement effort.

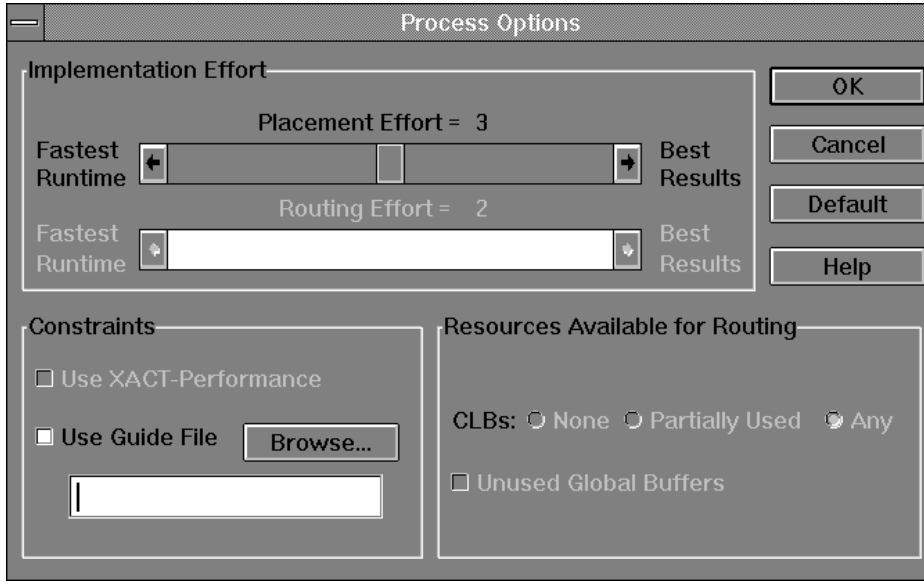


Figure 5-15 Process Options Dialog Box

A description of the fields and buttons on the dialog box follow.

Placement Effort

Choose the level of effort you want to use to place the selected logic. A slider bar permits you to choose fastest runtime and best results. The default is 3; a compromise between fastest runtime and best results.

Routing Effort

This option is disabled for the Place command.

Use XACT-Performance

This option is disabled for the Place command.

Use Guide File

Allows you to use a previous PPR result as a guide for routing and placement. The edit box displays the path of the LCA file (PM file for XC5200), if one is present in the current directory.

Browse

Opens the Select a File dialog box where you can select from a list of LCA files to use as a guide file. You can also change directories and choose an LCA file from a directory other than the current one.

Resources Available for Routing

This option is disabled for the Place command.

OK

Runs PPR with the given options.

Cancel

Closes the dialog box without changing the PPR settings or running PPR.

Default

Sets the dialog box to the default settings.

Help

Opens the online help for the dialog box.

Place and Route (Process Menu)

This command opens the Process Options dialog box shown in Figure 5-16 and runs PPR to place and route selected logic into the Floorplan window. Place and Route generates a file that represents all logic in the current floorplan, as well as a constraints file that represents the current floorplanned logic.

Place and Route runs PPR with the current options for that design, including the optional use of any existing LCA file (PM file for XC5200) from previously routed parts of the design as a guide.

When PPR is done, this command reads the resulting LCA file and updates the floorplan to reflect the results of PPR. Refer to the PPR Chapter in the *Development System Reference Guide* for more details.

This command is enabled only when there is selected logic.

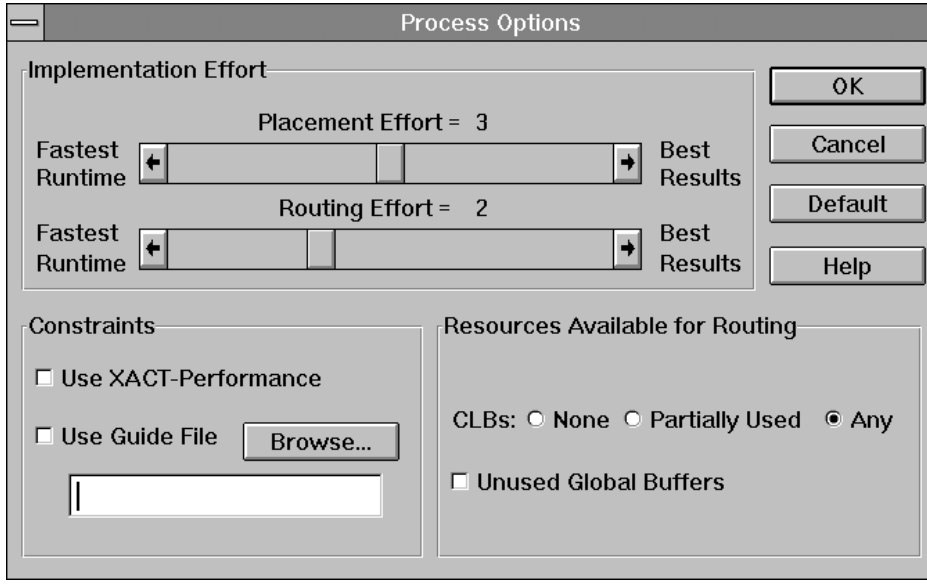


Figure 5-16 Process Options Dialog Box

A description of the fields and buttons on the dialog box follow.

Placement Effort

Choose the level of effort you want to use to place the selected logic. A slider bar permits you to choose fastest runtime and best results. The default is 3; a compromise between fastest runtime and best results.

Routing Effort

Choose the level of effort you want to use to route the selected logic. A slider bar permits you to choose from a range of fastest runtime to best results. The default is 2.

Use XACT-Performance

Check this box if you want to place and route the design based on TimeSpecs that you have placed on the schematic.

Use Guide File

Allows you to use a previous PPR result as a guide for routing and placement. The edit box displays the path of the LCA file (PM file for XC5200), if one is present in the current directory.

Browse

Opens the Select a File dialog box where you can select from a list of LCA files (PM file for XC5200) to use as a guide file. You can also change directories and choose an LCA file from a directory other than the current one.

Resources Available for Routing

This option permits you to determine whether PPR uses CLBs to route nets and to route through unused global buffers, if necessary.

- CLBs

  Select either None, Partially Used or Any.

  - None

    PPR will not use blocks for feedthroughs

  - Partially Used

    PPR will only use partially used CLBs for feedthroughs.

  - Any

    PPR will use any available CLB for feedthroughs.

- Unused Global Buffers

  Check this box if you want PPR to route signals through any unused global buffers in the die.

OK

Runs PPR with the given options.

Cancel

Closes the dialog box without changing the PPR settings or running PPR.

Default

Sets the dialog box to the default settings.

Help

Opens the online help for the dialog box.

Plot (File Menu)

This command opens the Plot dialog box shown in Figure 5-17 where you can plot either the contents of the floorplan or the entire Floorplan window.

Note: Plot is enabled for the Floorplanner only on the workstation version.

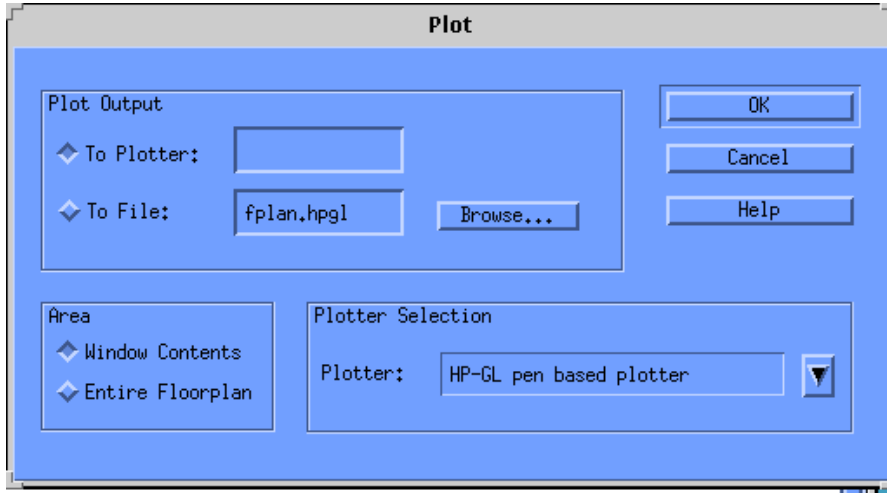


Figure 5-17 Plot Dialog Box

A description of the fields and buttons on the dialog box follow.

To Plotter

Instructs the Floorplanner to print the floorplan image to the plotter you have selected. Edit the adjacent box with the name of the appropriate plotter. The default is the value of the PLOTTER environment variable or blank if not defined.

To File

Instructs the Floorplanner to write either an HPGL or HPGL2 file to the file name that you have selected. You can plot this file at a later time. The default file name is fplan.hpgl and is written to the directory from which you invoked the Floorplanner.

Browse

Opens a standard file open dialog box which you can use to specify the name of the file for the To File box.

Window Contents

Plots only the current visible contents of the Floorplan window. This is the default.

Entire Floorplan

Plots the entire floorplan at the scale and detail present in the Floorplan window.

Plotter Type

Lists the types of plotters you can use. Initially, only HPGL and HPGL2-based plotters are supported. The default is the HPGL pen-based plotter. Xilinx recommends using the HPGL2 option if the target plotter supports HPGL2 as it provides better support for filled color rectangles, overlapped graphics, lines, and labels.

OK

Plots the current floorplan contents to the specified plotter.

Cancel

Cancels all changes you make in the dialog box and closes the dialog box.

Help

Opens the online help for this dialog box.

Print (File Menu)

This command opens the Print dialog box, shown in Figure 5-18 (PCs) or Figure 5-19 (for workstations) where you can print an image of the floorplanned logic in the Floorplan window. You can choose between printing the entire Floorplan window or just the contents (floorplanned logic) in the floorplan.

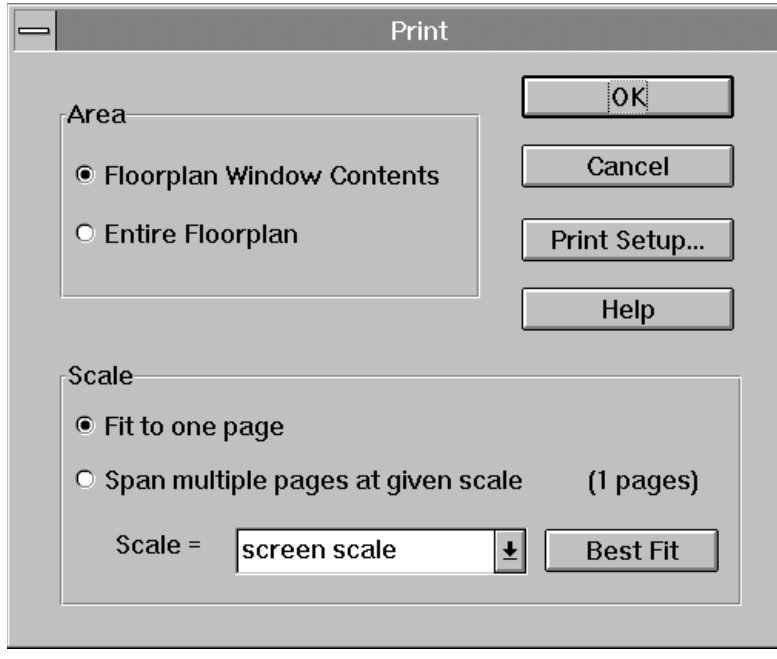


Figure 5-18 Print Dialog Box (PCs)

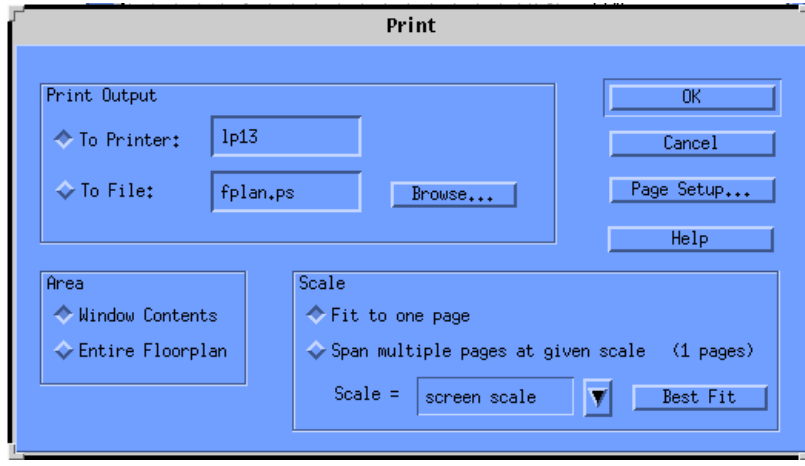


Figure 5-19 Print Dialog Box (Workstations)

A description of the fields and buttons on the dialog box follow.

Floorplan Window Contents

Prints only the current visible contents of the Floorplan window. This is the default.

Entire Floorplan

Prints the entire floorplan either scaled to one page or spanning multiple pages.

Fit to One Page

Prints the desired image to a size that fits on a single page. This is the default.

Span Multiple Pages at Given Scale

Prints the desired image at the desired scale.

Scale

Adjusts the scale relative to the Floorplan window scale. The scale is ignored when you use the Fit to One Page option. The default is the Floorplan window scale, called screen scale.

Best Fit

Sets the scale to show sufficient detail, while minimizing the number of pages required for print.

OK

Closes the dialog box and prints the desired image.

Cancel

Closes the dialog box and returns you to the current Floorplanner session.

Help

Opens the online help for this dialog box.

Print Setup

Opens the Print Setup dialog box. Figure 5-20 shows the Printer Page Setup dialog box for workstations. Figure 5-21 shows the Print Setup dialog box for PCs.

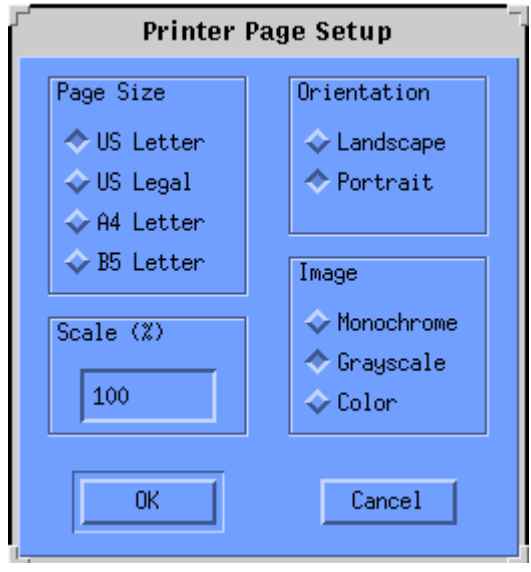


Figure 5-20 Printer Page Setup Dialog Box (Workstations)

A description of the fields and buttons on this dialog box follow.

Page Size

- US Letter (default)

  Selects a page size that is 8 1/2 inches by 11 inches.

- US Legal

  Selects a page size that is 8 1/2 inches by 14 inches.

- A4 Letter

  Selects a page size that is the European equivalent of 8 1/2 inches by 11 inches.

- B5 Letter

  Selects a page size that is the European equivalent of 8 1/2 inches by 14 inches.

Orientation

- Landscape

  Orients the printed page such that the shorter edges are horizontal.

- Portrait (default)

  Orients the printed page such that the shorter edges are vertical.

Scale (%)

Permits you change the scaling of the desired image. The default is 100%.

Image

- Monochrome

  Prints the image in black and white.

- Grayscale (default)

  Prints the image using black, white and shades of gray.

- Color

  Prints the image in the colors that are supported by the color printer you are using.

OK

Sets the options, closes the Print Page Setup dialog box and brings the Print dialog box to the foreground.

Cancel

Closes the dialog box without making any changes to the print setup options, and brings the Print dialog box to the foreground.

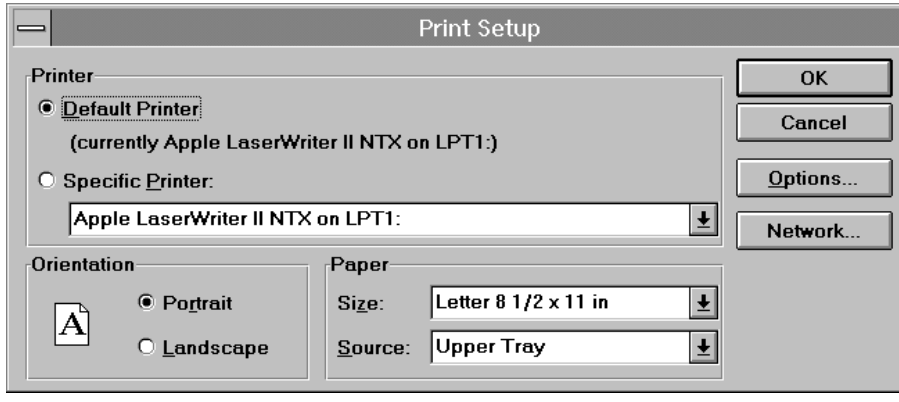


Figure 5-21 Print Setup Dialog Box (PCs)

A description of the fields and buttons on this dialog box follow.

Default Printer

Automatically prints the image to the default printer that has been defined for your system.

Specific Printer

Prints to a printer that you select from a list of printers.

Portrait

Prints the image to a page whose width is less than its length. For example, an A-size page is 8 1/2 inches by 11 inches.

Landscape

Prints the image to a page whose width is greater than its length. For example, an A-sized page is 11 inches by 8 1/2 inches.

Paper

Permits you to select the size of the paper and specific paper tray, if the printer contains more than one tray.

OK

Closes the dialog box and retains the settings you made for future printing.

Cancel

Closes the dialog box without retaining the settings you made.

Network (PC only)

Opens the Printer - Network Connections dialog box where you access the network drive to change the network path, system port and protocol. This option is only available if you are running Windows for Workgroups.

Options

Opens the Options dialog box shown in Figure 5-22 where you can specify the printer‘s settings.

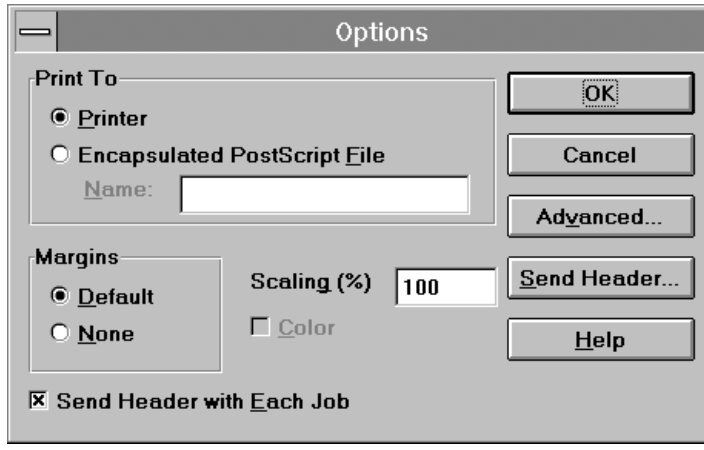


Figure 5-22 Options Dialog Box

Note: This Options dialog box will vary depending on the type of printer you are using.

A description of the fields and buttons on this dialog box follow.

Printer

Enables the print job to print to the printer specified in the Print Setup dialog box. This is the default.

Encapsulated PostScript File

Will print the selected image to an encapsulated postscript format specified in the Name edit box.

Name

Specify the name of the postscript file to which the Print command prints the selected image.

Margins

Determines whether the image is printed on the page with or without margins.

Scaling (%)

Permits you to change the scaling of the desired image. The default is 100%.

Color

Check this box if you have a color printer and you want the image to be printed in color.

OK

Closes this dialog box with your options, and brings the Print Setup dialog box to the foreground.

Cancel

Cancels the options set in this dialog box and brings the Print Setup dialog box to the foreground.

Help

Opens the online help for this dialog box.

Advanced

Opens the Advanced Options dialog box shown in Figure 5-23.

Send Header

Opens the Send Header dialog box shown in Figure 5-24.

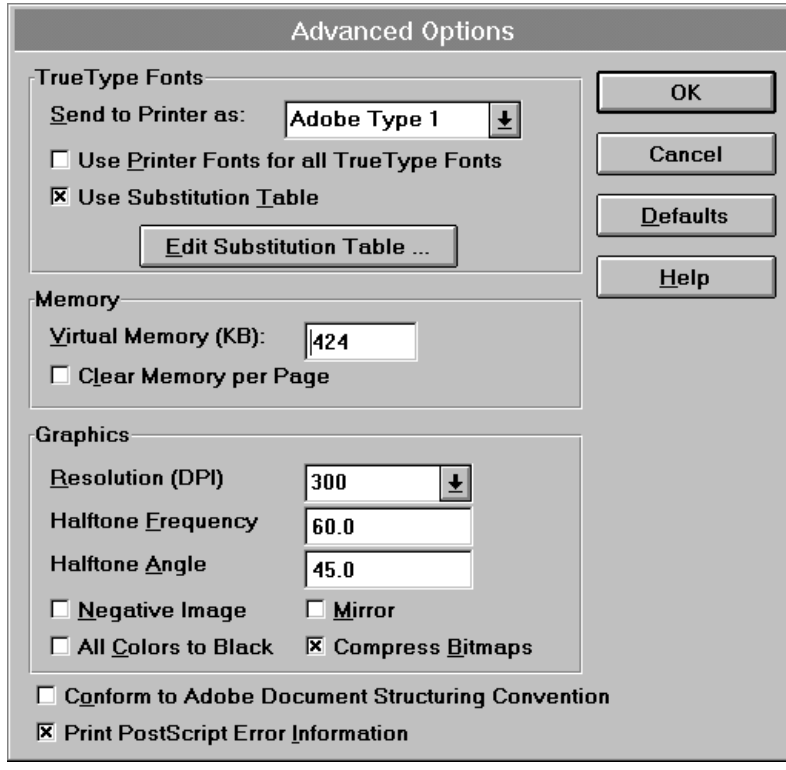


Figure 5-23 Advanced Options Dialog Box

Note: This dialog box will be different depending on the type of printer you are using.

A description of the fields and buttons on this dialog box follow.

True Type Fonts

- Send to Printer as

  Provides a list of available Adobe font types from which to choose.

- Use Printer Fonts for all True Type Fonts

  Checking this box enables the use of printer fonts. The default is off.

- Use Substitution Table

  Checking this box enables more type and printer fonts that are available from the Substitution Table.

- Edit Substitution Table (default)

  Opens the Substitution dialog box, shown in Figure 5-25 where you can change the true type font and printer font.

Memory

- Virtual Memory (KB)

  Sets the memory limitations available for the print job. The default is 424 kilobytes.

- Clear Memory per Page

  Clears the memory each time a page is printed when enabled.

Graphics

- Resolution (DPI)

  Sets the DPI (dots per inch) resolution for the printed image. The default is 300 dpi. Click the down arrow for more choices.

- Halftone Frequency

  Sets the LPI (lines per inch) resolution for the printed image. It designates the number of rows of halftone dots per inch during printing. The higher the value, the better will be the printed images. The default is 60.

- Halftone Angle

  Sets the degree of the screen angle which determines the angle that the rows of halftone dots are printed. The default is 45, which makes the dot rows less conspicuous.

- Negative Image

  Prints a reverse image of the floorplan when enabled.

- All Colors to Black

  Converts all color to black when enabled.

- Mirror

  Prints the mirror image of the selected floorplan.

- Compress Bitmaps (default)

  Enables the compress mode for printing bitmaps. The default is enabled, so that the print files take less memory.

- Conform to Adobe Document Structuring Convention

  Meets the Adobe PostScript printing requirements for color matches, true type fonts, and so forth.

- Print PostScript Error Information (default)

  Writes out error information when you select to write the floorplan to an encapsulated postscript file.

OK

Sets the options that you have selected, closes the Advanced Options dialog box, and returns the Print Setup dialog box to the foreground.

Cancel

Cancels any changes you might have made in the Advanced Options dialog box, closes the dialog box, and returns the Print Setup dialog box to the foreground.

Defaults

Resets the Advanced Options dialog box settings to the default settings.

Help

Opens the online help for this dialog box.

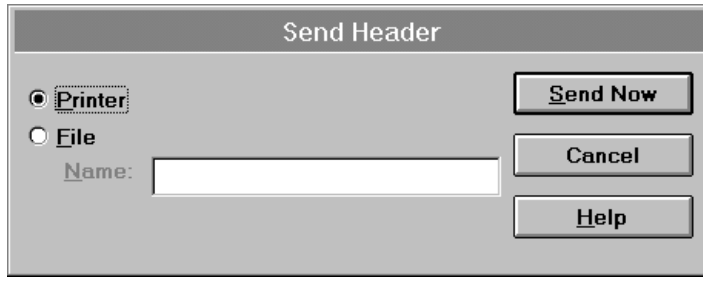


Figure 5-24 Send Header Dialog Box

Note: This dialog box will be different depending on the type of printer you are using.

A description of the fields and button on this dialog box follow.

Printer

Prints the image with the header information.

File

Prints the header information to the specified file.

Send Now

Prints the image with the options you have selected with the header information you have specified.

Cancel

Closes this dialog box and returns you to the Options dialog box.

Help

Opens the online help for this dialog box.

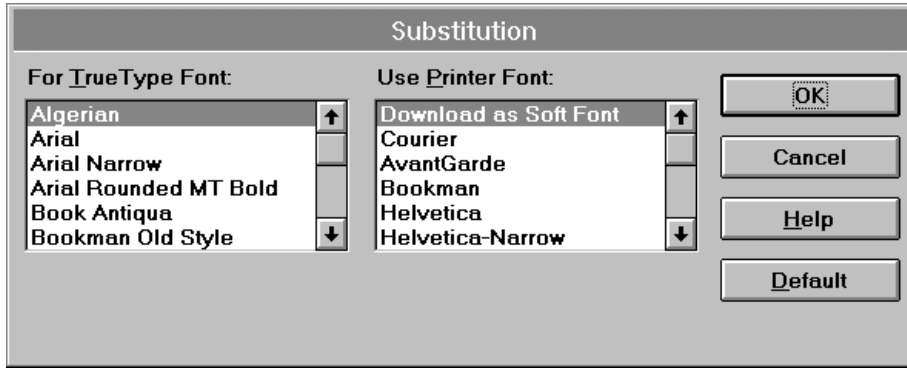


Figure 5-25 Substitution Dialog Box

Note: This dialog box will be different depending on the type of printer you are using.

A description of the fields and buttons on this dialog box follow.

For True Type Font

Lists the available true type fonts for your print jobs.

Use Printer Font

Lists the available printer fonts that you can use for printing.

OK

Sets the selections for true type font and printer fonts for the current print job, closes the dialog box, and brings the Advanced Options dialog box to the foreground.

Cancel

Closes the dialog box without updating the print options for the current print job.

Help

Opens the online help for this dialog box.

Default

Resets this dialog box to the default settings, Algerian for true type font and Download as Soft Font for printer font.

Prohibit (Floorplan Menu)

This command allows you to lock specified resources on the die by preventing PPR from being able to place logic at those locations.

Invoke the command, then click or drag the mouse on the resources in the Floorplan window that you want to designate as prohibited.

When the constraints file is generated, the Floorplanner creates a prohibit block record (XC3000 devices only) for each resource that must be reserved. For all other devices, a prohibit instance record is created.The block record instructs PPR not to place logic at those locations.

Note: You cannot prohibit global buffers because you cannot specify this type of limitation in the constraints file without prohibiting the use of some IOBs.You also cannot prohibit carry logic.

Ratsnest (View Menu)

This command opens the Ratsnest dialog box where you control which nets are present in the ratsnest display and how the Floorplanner presents those nets. If this dialog box is already open, clicking on the command from the menu brings it to the front of the display.

You can use the Ratsnest dialog box shown in Figure 5-26 to manually find and select individual nets.

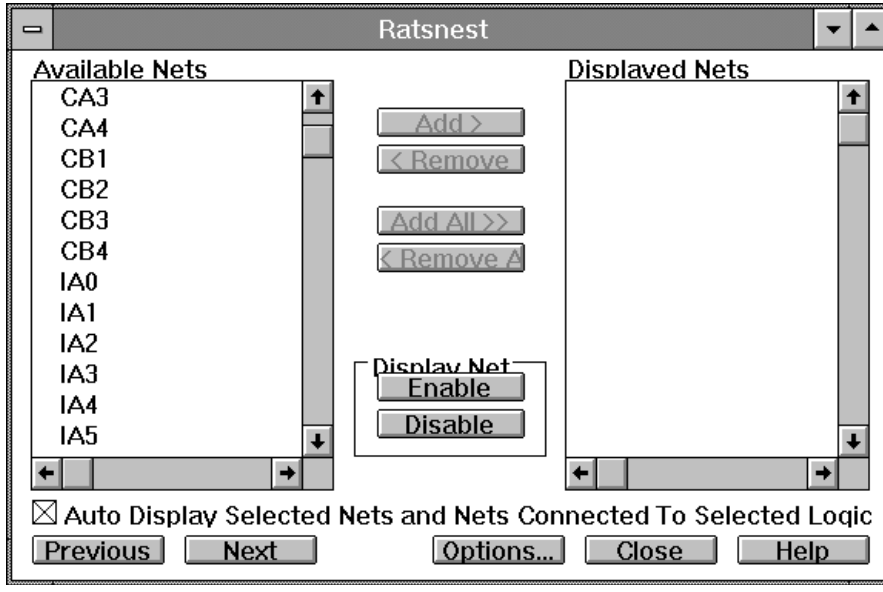


Figure 5-26 Ratsnest Dialog Box

A description of the fields and buttons on the dialog boxes follow.

Note: You can disable nets using Display Net: Disable. The Floorplanner excludes disabled nets from automatically displaying when you click the Disable button. By default, all nets driven from global buffers are disabled. The presentation of nets in the Floorplan Window is subject to the settings in the Ratsnest Options dialog box.

Available Nets

Presents a scrollable, sorted list of all nets in the design. You can select nets from this list using the mouse, or using the Select Nets dialog box.

Displayed Nets

Presents a scrollable, sorted list of nets presently available for display in the Floorplan window. Disabled nets do not appear in this list.

In automatic mode, this list is automatically updated to show which nets are visible. In manual mode use the Add, Add All, Remove, and Remove All buttons to change the list.

Auto Display Selected Nets and Nets Connected to Selected Logic

Selects either the automatic or manual mode for the presentation of nets in the Floorplan window.

When this option is enable (box is checked), the Floorplanner draws display lines only for nets that are selected or have at least one end on the selected logic. The display automatically changes as you select or deselect logic and nets. The Displayed Nets option lists which nets are visible in the Floorplan window. When this box is not checked, the manual mode is on. You must choose which nets are displayed by using the Add, Add All, Remove, and Remove All buttons.

Add

Adds all selected nets that are also enabled to the Displayed Nets list. This button is disabled if the Auto Display Selected Nets... button is enabled.

Remove

Removes all selected nets from the Displayed Nets list. This button is disabled if the Auto Display Selected Nets... button is enabled.

Add All

Adds all enabled nets to the displayable nets list. This button is disabled if the Auto Display Selected Nets... button is enabled.

Remove All

Removes all nets from the Displayed Nets list. This button is disabled if the Auto Display Selected Nets... button is enabled.

Display Net

- Enable

  Enables all selected nets for addition to the Displayed Nets list when you use the All or Insert buttons, or when appropriate in automatic mode.

- Disable

  Disables all selected nets and prohibits you from adding them to the Displayed Nets list. Disabled nets appear in light gray.

Next

Scrolls the Available Nets list to bring the first or next selected net to the top of the display.

Previous

Scrolls the Available Nets list to bring the previously selected net to the top of the display.

Close

Closes the dialog box.

Help

Opens the online help for the dialog box.

Options

Opens the Ratsnest Options dialog box shown in Figure 5-27. The Ratsnest Options dialog box gives you control over how the Floorplanner displays nets in the Floorplan window and over rubberbanding.

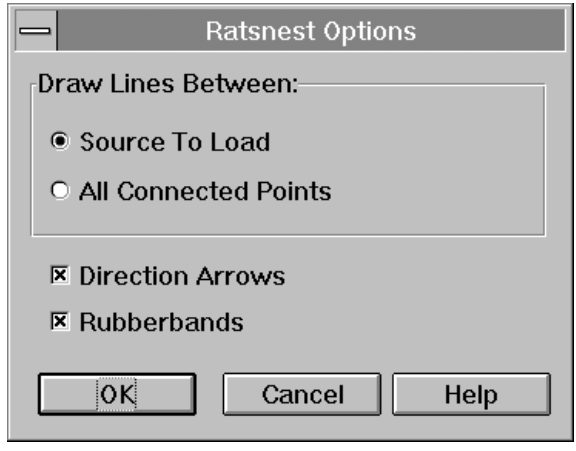


Figure 5-27 Ratsnest Options Dialog Box

A description of the fields and buttons on the dialog boxes follow.

Draw Lines Between

- Source To Load (default)

  Displays only lines beginning at signal source pins and extending to all load pins.

- All Connected Points

  Displays lines between all connected pins, irrespective of whether they are loads or source. This mode generally results in a cluttered display.

Direction Arrows (default on)

Toggles the presentation of direction arrowheads at the load pins of lines.

Rubberbands (default on)

Toggles the display of stretching the lines that represent nets when moving icons or patterns in the Floorplan window.

OK

Closes the dialog box and uses the current settings.

Cancel

Closes the dialog box but ignores the settings.

Help

Opens the online help for the dialog box.

Read Constraints (File Menu)

This command opens the standard file open dialog box where you can select a constraints file to load. It is called Select constraints file, as shown in Figure 5-28.

The Floorplanner reads the selected constraints file to floorplan the design.

This command ignores all previously floorplanned logic unless constraints in the file call that logic or the occupied resources.

Note: The Floorplanner has a limited ability to understand constraints in a constraints file. Generally, it only understands a 1 to 1 correspondence between symbols and resources.

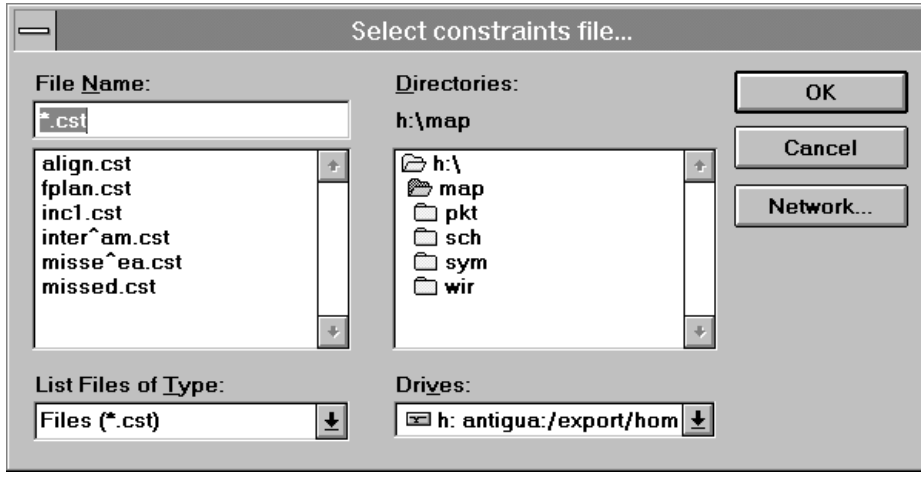


Figure 5-28 Select Constraints File Dialog Box

A description of the fields and buttons on the dialog box follow.

File Name

Displays the file extension that is currently selected in the List Files of Type box. You can edit the type of file name you want to search.

Directories

Lists the directories accessible from the current directory. You can change the current directory by double-clicking in this list.

List Files of Type

Lists all the files (in alphanumeric order) in the current directory that match the pattern shown in File Name.

Drives

Shows the current drive that is selected. Lists the drives that are available to use. Click the arrow to display the list. When you select a drive, the software updates the information in the Directories box.

OK

Closes the dialog box and loads the selected design file.

Cancel

Closes the File Open dialog box without opening the file.

Network (PC only)

Accesses the network drive. This option is only available if you are running Windows for Workgroups.

Read Placed Design (File Menu)

This command opens the standard File Open dialog box where you can select a placed version of the design (LCA file) to load. It is called Select design file, as shown in Figure 5-29.

The Floorplanner reads the selected LCA file (PM file for XC5200 devices) and updates the floorplan to correspond to the placement information in the LCA/PM file. The resulting floorplan reflects the PPR placement of the design.

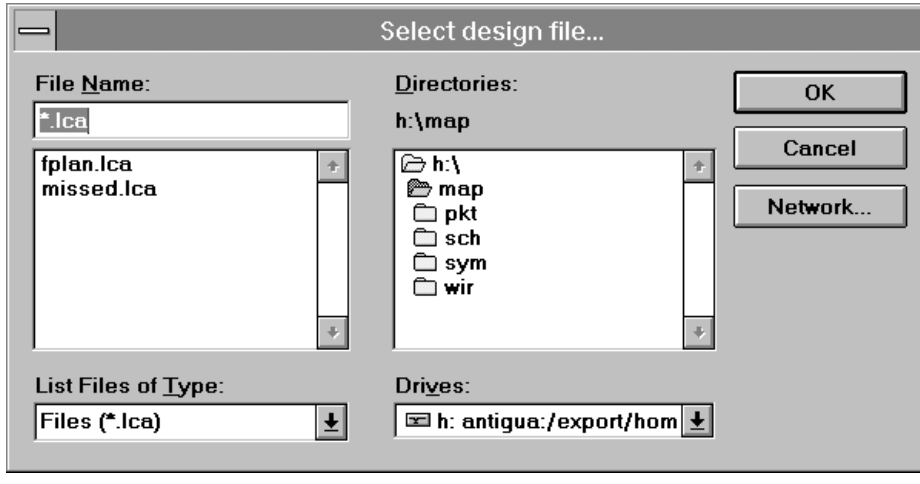


Figure 5-29 Select Design File Dialog Box

A description of the fields and buttons on the dialog box follow.

File Name

Displays the file extension that is currently selected in the List Files of Type box. You can edit the type of file name you want to search.

Directories

Lists the directories accessible from the current directory. You can change the current directory by double-clicking in this list.

List Files of Type

Lists all the files (in alphanumeric order) in the current directory that match the pattern shown in File Name.

Drives

Shows the current drive that is selected. Lists the drives that are available to use. Click the arrow to display the list. When you select a drive, the software updates the information in the Directories box.

OK

Closes the dialog box and loads the selected design file.

Cancel

Closes the File Open dialog box without opening the file.

Network (PC only)

Accesses the network drive. This option is only available if you are running Windows for Workgroups.

ReBuild (Hierarchy Menu)

This command constructs a hierarchy tree using the symbol instance names in the design. It also builds subtrees for these symbols that are associated with selected nodes. The Floorplanner derives the new hierarchy macros from the symbol instance names.

This command is enabled only when there is logic that is selected.

Refresh (View Menu)

This command clears and redraws all open windows associated with the Floorplanner.

Use this command whenever you need to clean up the display.

Remove (Floorplan Menu)

This command removes all selected logic from the Floorplan window and returns them to the Design window.

Use this command to remove symbols from the floorplan.

Remove All (Floorplan Menu)

This command removes all logic icons in the design from the Floorplan window and returns them to the design hierarchy in the Design window.

Use this command to remove all the symbols from the floorplan, and create an empty resource map.

Remove Group (Hierarchy Menu)

This command removes the selected group from the design hierarchy. This command is enabled only when you have one or more groups selected from the Design window.

When the Floorplanner ungroups a macro, it does not ungroup the associated lower-level logic, even though it is selected.

Rename (Hierarchy Menu)

This command opens the Rename dialog box shown in Figure 5-30 where you can change the name of the currently selected hierarchical macro.

This command is enabled only when a non-RPM hierarchical macro is selected. You cannot change the names of symbols and nets with this command.

Since new user-created hierarchical macros get computer-generated names (unless you specified a label for a given symbol or macro), use this command to create more meaningful names.

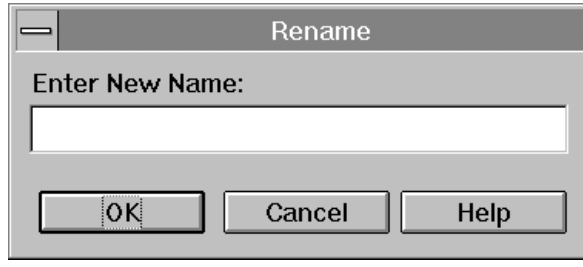


Figure 5-30 Rename Dialog Box

A description of the fields and buttons on the dialog box follow.

Enter the new name

Enter the name that you want the selected group to have.

OK

Applies the new name to the currently selected hierarchical node. OK only works if there is only one selected hierarchical macro (other than the lower-level logic of the selected macro).

Cancel

Closes the dialog without renaming the macro.

Help

Opens the online help for the dialog box.

Resources (View Menu)

This command (available when the Floorplan window is in focus) opens the Resources dialog box where you control the resource and placed logic graphics and labels, the display of the tile grid, row and column, and I/O pin labels that are present in the Floorplan window

display of the selected floorplan. Figure 5-31, Figure 5-32 and Figure 5-33 show the dialog boxes for the XC5200, XC4000 family and XC3000 family, respectively.

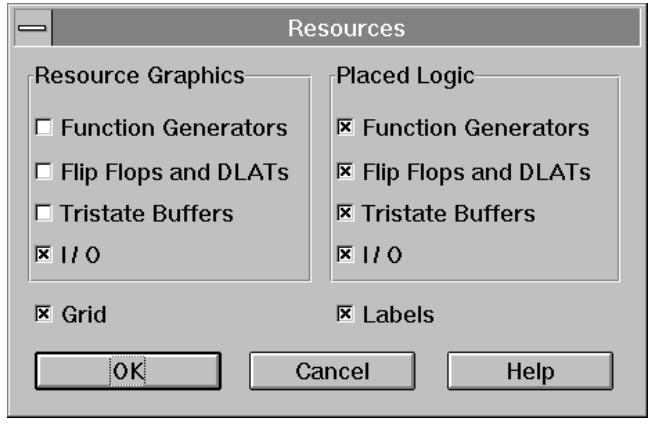


Figure 5-31 Resources Dialog Box for the XC5200 Family

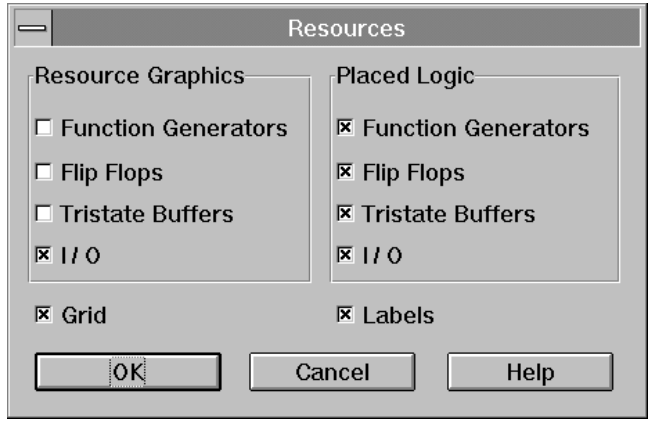


Figure 5-32 Resources Dialog Box for the XC4000 Family

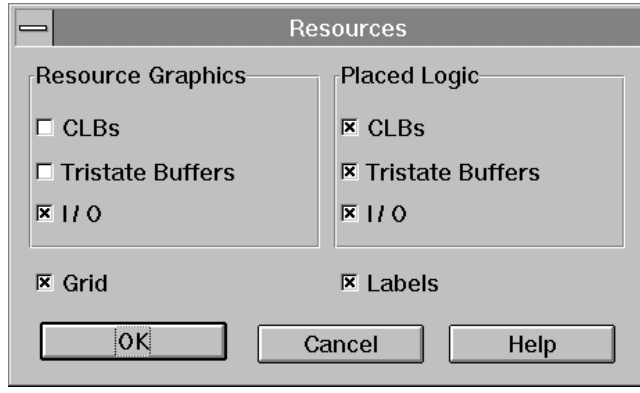


Figure 5-33 Resources Dialog Box for the XC3000 Family

A description of the fields and buttons on the dialog boxes follow.

Resource Graphics

- CLBs (default off)

  Controls the display of CLB resource graphics in the Floorplan window.

  This button is present only for the XC3000 family.

- Function Generators (default off)

  Controls the display of the function generator, RAM, and carry logic resource graphics in the Floorplan window.

  This button is present for the XC4000 and XC5200 families.

- Flip Flops (default off)

  Controls the display of D flip-flop resource graphics in the Floorplan window. It does not display flip-flops that are associated with IOBs.

  This button is present only for the XC4000 family.

- Flip Flops and DLATs (default off)

  Controls the display of D flip-flop resource graphics and DLATs (a level sensitive D-type latch) in the Floorplan window.

This button is present only for the XC5200 family.

- Tristate Buffers (default off)

  Controls the display of tristate buffer resource graphics in the Floorplan window.

- I/O (default on)

  Controls the display of IOB and global buffer resource graphics in the Floorplan window.

Placed Logic

- CLBs (default on)

  Controls the display of CLB placed logic graphics and logic icons in the Floorplan window.

  This button is present only for the XC3000 family.

- Function Generators (default on)

  Controls the display of placed function generator, RAM/ROM, and carry-logic logic symbols and logic icons in the Floorplan window.

  This button is present for the XC4000 and XC5200 families.

- Flip Flops (default on)

  Controls the display of placed D flip-flop placed logic symbols and logic icons in the Floorplan window. It does not display flip-flops that are associated with IOBs.

  This button is present only for the XC4000 family.

- Flip Flops and DLATs (default on)

  Controls the displays of flip-flops and DLATs in the Floorplan window.

  This button is present only for the XC5200 family.

- Tristate Buffers (default on)

  Controls the display of placed tristate buffer logic symbols and logic icons in the Floorplan window.

- I/O (default on)

  Controls the display of placed IOB and global buffer logic symbols and logic icons in the Floorplan window.

Grid (default on)

Controls the display of the grid, column and row labels, and I/O pin labels in the Floorplan window.

Labels (default on)

Controls the display of text labels associated with logic icons in the Floorplan window.

OK

Closes the dialog box and applies the chosen display settings to the Floorplan window.

Cancel

Closes the dialog box without changing the display settings.

Help

Opens the online help for the dialog box.

Save (File Menu)

This command saves the current design as an FPN file with the name of the current design. This file contains information about the design including, hierarchy organization, symbol and node to resource association, net and logic color assignments.

You can use this file later to restore this information to the design.

Save also creates a constraints file for the floorplan, which you can use when running PPR.

Save As (File Menu)

This command opens the standard file open dialog box shown in Figure 5-34 where you change the name of design or change directories.

Use this command to create a floorplan file of the current design under a different file name. You can also use this command to change directories and save the new design file name in a directory other than the current directory.

The name of the design currently loaded in the Floorplanner changes to the new name. Save As also allows you to create a constraints file under the new design name directory.

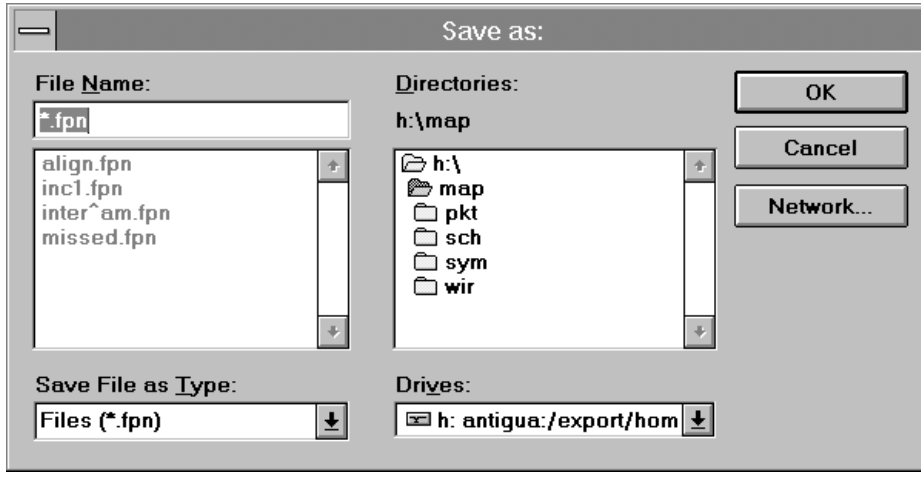


Figure 5-34 Save As Dialog Box

A description of the fields and buttons on this dialog box follow.

File Name

Permits you to select the name of the FPN file that will be created with the Save As command. It also lists existing FPN files that have been created in the current directory during past Floorplanning sessions.

Directories

Lists the directories accessible from the current directory. You can change the current directory by double-clicking in this list.

Save File as Type

Contains a list of available file extensions that you can choose for the file that is to be created.

Drives

Lists the drives that have been defined on your system.

OK

Saves the current floorplan in an FPN file with the file name you have selected.

Cancel

Cancels the Save As command, closes the dialog box, and returns you to the current floorplanning session.

Network (PC only)

Accesses the network drive. This option is only available if you are running Windows for Workgroups.

Search for Help On (Help Menu)

This command opens the Search dialog box, shown in Figure 5-35. Use this dialog box to search on keyword topics for the Floorplanner in the online help.

You can type in a character string that the Floorplanner will match to similar characters in the keyword list, or select a topic from the list. The Floorplanner displays a list of relevant topics and, when you click the Go To button, displays the appropriate online help information.

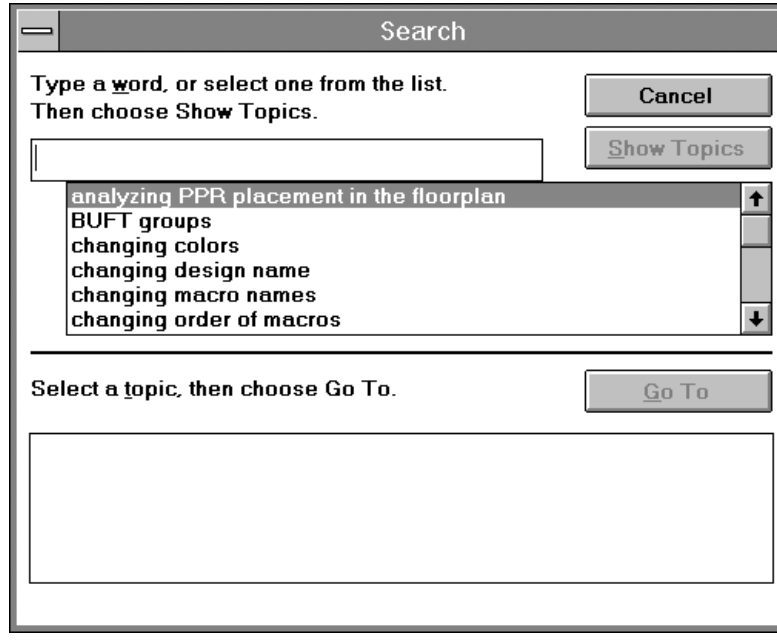


Figure 5-35 Search Dialog Box

A description of the fields and buttons on this dialog box follow.

Type a word

Permits you to type in characters that the Floorplanner will match to similar characters found in the keyword list.

Cancel

Closes the Search dialog box without accessing the online help, and returns you to the current floorplanning session.

Show Topics

Displays a list of topics associated with the keyword that you have selected.

Go To

Takes you to the online help information for the desired topic.

Select Loads (Edit Menu)

This command allows you to select logic symbols whose inputs connect to selected logic outputs. You can only use Select Loads when there is logic that is selected.

Use this command to determine data flow.

Select Sources (Edit Menu)

This command allows you to select logic symbols whose outputs connect to selected logic inputs. You can only use Select Sources when there is logic that is selected.

Use this command to determine data flow.

Sort (Hierarchy Menu)

This command opens the Sort dialog box shown in Figure 5-36 where you can change the order in which Floorplanner displays the macros and symbols in the Design window.

The ordering of symbols is important for distributed floorplanning because the symbols are distributed in the order in which they are listed in the hierarchy window.

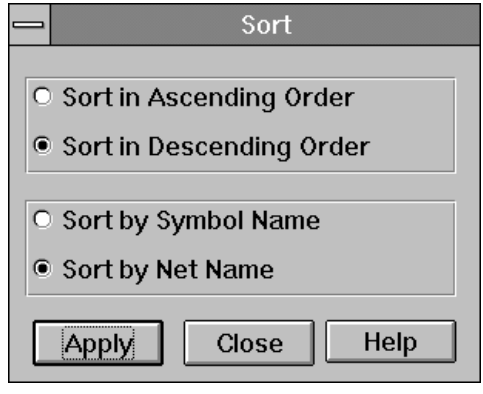


Figure 5-36 Sort Dialog Box

A description of the fields and buttons on the dialog box follow.

Sort in Ascending Order

Rearranges the currently selected logic in the hierarchical lists so that the first (top most) node or net name has the lowest ASCII value (closest to ‘a’ or ‘0’). For a bus, this results in the least significant bit at the top, such as databus0.

Sort in Descending Order (default)

Rearranges the currently selected macros in the hierarchical lists so that the first (top most) node or net name has the highest ASCII value (closest to ‘Z’). For a bus, this results in the most significant bit at the top, such as databus31 for a 32-bit bus.

Sort by Symbol Name

Rearranges currently selected macros in the hierarchical lists based on the symbol instance names.

Sort by Net Name (default)

Rearranges the currently selected macros in the hierarchical lists based on the symbol instance (pad) names for IOBs, input net names for tristate buffers, and output net names for all other logic.

Apply

Causes the Floorplanner to sort the selected logic as indicated. Sorting changes just the position of the names in the hierarchy. It does not change the hierarchical structure of the design, or the position of logic already floorplanned.

Close

Closes the dialog box.

Help

Opens the online help for the dialog box.

Spacing (Floorplan Menu)

This command opens the Spacing dialog box shown in Figure 5-37. Here you can change the spacing that the Floorplanner uses during distribution and allocation when you drop logic icon stacks in the Floorplan window in the distribute mode.

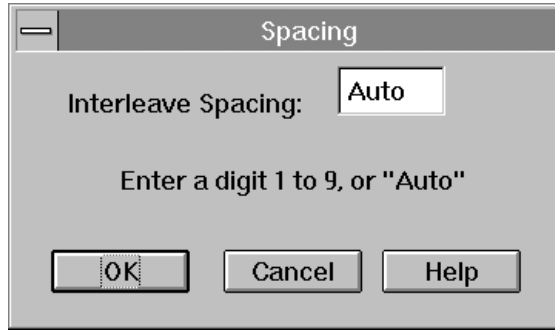


Figure 5-37 Spacing Dialog Box

A description of the fields and buttons on the dialog boxes follow.

Interleave Spacing

A user-controlled value (positive number) that controls the separation of resources when dropping an icon stack onto the floorplan.

A value of 1 means no separation between adjacent resource allocations. A value of 2 means that every other resource is allocated.

When set to Auto (default), spacing is 1 or 2 depending on the type of symbols being dropped and the allocation direction.

Use this feature to help you place an interleaved bus pattern.

OK

Makes the indicated change to the resource spacing value and closes the dialog box.

Cancel

Closes the dialog box without changing the resource spacing value.

Help

Opens the online help for this dialog box.

Stack (Floorplan Menu)

This command sets the stack mode for dropping a stack of logic icons in the Floorplan window. In stack mode, logic icons are left in a stack, and all resources allocated for that stack are available to all logic symbols associated with that stack. The placer will assign specific locations to the resources within the stack.

In the stack mode, dropping the logic icon stack automatically allocates resources for the stack, as described in the Distribute command.

If the current mode is stack mode and you pick up an icon stack from the Floorplan window that was placed using distribute mode, then stack mode have no effect; however, clicking the Stack Mode toolbar button while moving the stack or pattern, forces stack mode when you drop the logic icons. This way you can restack previously placed logic that had been floorplanned in distribute mode.

The Stack command is the primary mechanism for initial floorplanning at the high, or macro, level. Placing stacks in single resource locations, with the spot allocate direction, provides the mechanism for “bubble graph” representations (connectivity between macros) of a design, which is useful for making pre–floorplanning decisions about relative locations of logic groupings.

Toolbar (View Menu)

This command (available when the Floorplan window is in focus) toggles the presence of the toolbar just below the menus. (On the workstation version, the toolbar appears under the menus on the Floorplan window). The toolbar contains buttons for easy access to many commands. Figure 5-38 shows the toolbar.

Figure 5-38 Floorplanner Window Toolbar

Toolbar Buttons

The following buttons, arranged here in the order they appear on the toolbar from left to right, are available from the toolbar.

Assign

Figure 5-39 Assign Button

This two-position button, shown in Figure 5-39 indicates whether the cursor is in selection or resource assignment mode. You must press the button to change to resource assignment mode after selecting some logic.

- Selection mode (default)

  Dragging out areas and clicking on objects changes what items are currently selected.

- Resource assignment mode

  Dragging and clicking the mouse in the Floorplan window defines an area allocation for selected logic.

Usually, after running in the resource assignment mode, this button changes to the selection mode. To prevent this change, hold down the Shift key when choosing the resource assignment mode.

Distribute

Figure 5-40 Distribute Button

The Distribute button shown in Figure 5-40 sets the distribute mode for dropping a stack of icons in the Floorplan window. In this mode, the Floorplanner sequentially assigns single resource locations for each icon, dependent on the current allocation direction.

The allocation direction can be up, down, left, right, or spot. The spot direction allows you to select and drop only one icon at a time, allowing you to manually pick the locations one by one.

Distribute also distributes selected logic that has been floorplanned previously in stack mode.

Stack Icons

Figure 5-41 Stack Icons Button

The Stack Icons button shown in Figure 5-41 sets the stack mode for dropping a stack of logic icons in the Floorplan window. In stack mode, icons are left in a stack, and all resources allocated for that stack are available to all logic symbols associated with that stack.

In the stack mode, dropping the icon stack automatically allocates resources for the stack dependent on the current allocate direction, as described in the Distribute command. In this case, the spot allocate direction results in only a single resource being allocated to the stack of icons.

This button also “stacks up” any selected logic that has been floorplanned previously in distribute mode.

Allocate Direction

Figure 5-42 Allocate Up Button

Figure 5-43 Allocate Down Button

Figure 5-44 Allocate Left Button

Figure 5-45 Allocate Right Button

Figure 5-46 Allocate One at a Time (Spot) Button

These five buttons shown in Figure 5-42 through Figure 5-46 toggle the allocation direction of the icons when you place them in the Floorplan window. In distribute mode, you drop icons into the Floorplan window starting with the resource indicated by the cursor and continuing upward (up position), downward (down position), to the left (left position), or to the right (right position) until all icons have been dropped, an occupied resource is encountered, or the edge of the FPGA map has been reached. In stack mode, these buttons allocate resources to the entire group of icons, not individual logic icons.

The Allocate Manually (Spot) button allows you to distribute one logic icon at a time. Each time you click the mouse button on a resource, that resource is allocated to the next logic icon. Only a single resource is allocated in stack mode. These logic icons do not affect patterns.

Capture Pattern

Figure 5-47 Capture Pattern Button

The Capture Pattern button shown in Figure 5-47 makes a copy of the currently selected logic icon pattern, and saves it as the "reference" pattern. You can apply the reference pattern to other logic of similar makeup using the menu command or toolbar button. The Floorplanner saves the reference pattern as a list, keeping the selection order of the symbols as same as they appear in the Design window.

Impose Pattern

Figure 5-48 Impose Pattern Button

The Impose Pattern button shown in Figure 5-48 imposes a relative placement upon the logic currently in transit or floorplanned and selected, that corresponds to the reference pattern saved with the Capture Pattern command. The reference pattern is imposed on the transitory logic by matching symbols one by one in the order in which they are found in the Design window. This button is grayed out when it is inoperative. It is enabled when a pattern has been captured.

Flip Vertical

Figure 5-49 Flip Vertical Button

The Flip Vertical button shown in Figure 5-49 flips the selected logic so that the symbols at the top move to the bottom and the symbols at the bottom move to the top.

If you use this button on selected logic that is not in transit, the logic is flipped in place. Flipping symbols in the Floorplan window does not affect the design hierarchy.

Flip Horizontal

Figure 5-50 Flip Horizontal Button

The Flip Horizontal button shown in Figure 5-50 flips the selected logic so that symbols on the left move to the right and the symbols on the right move to the left.

If you use this button on selected logic that is floorplanned, the logic is flipped in place. Flipping symbols in the Floorplan window does not affect the design hierarchy.

Labels

Figure 5-51 Labels Button

The Labels button shown in Figure 5-51 toggles the display of symbol names and instance names of floorplanned logic in the Floorplan window. The default is on.

Ratsnest

Figure 5-52 Ratsnest Button

The Ratsnest button shown in Figure 5-52 toggles the display of the ratsnest (net connectivity lines) in the floorplan. When enabled, vectors are drawn on the Floorplan window between floorplanned logic to show connectivity between the inputs and outputs. The default is on.

Resources

Figure 5-53 Resources Button

The Resources button shown in Figure 5-53 toggles the display of resource graphics in the floorplan. When enabled, the resources that are in the CLB, such as function generators, flip-flops, and tristate buffers are drawn in each CLB. The default is off.

Zoom In

Figure 5-54 Zoom In Button

The Zoom In button shown in Figure 5-54 enlarges the objects in the window.

Zoom Out

Figure 5-55 Zoom Out Button

The Zoom Out button shown in Figure 5-55 reduces the objects in the window.

Zoom Full View

Figure 5-56 Zoom Full View Button

The Zoom Full View button shown in Figure 5-56 sets the scale and pan position so that the entire FPGA map fits in the window. It also sets automatic resizing, where resizing of the window automatically rescales the view.

Zoom To Area

Figure 5-57 Zoom To Area Button

The Zoom To Area button shown in Figure 5-57 puts the pointer into the area pick mode, where you can use the mouse to drag out an area that is then used to set the scale and pan position. After dragging out a single area, the cursor reverts to the normal Select mode.

Zoom To Selected

Figure 5-58 Zoom To Selected Button

The Zoom To Selected button shown in Figure 5-58 sets the scale and the pan position so that all selected logic is visible. This command also clears automatic resizing.

Undo (Edit Menu)

This command undoes the most recent command or floorplanning operation. Undo only affects commands that actually change the hierarchy tree or the way that resources are allocated to symbols. You can also use this command to undo any changes made using the mouse to move logic, such as:

Read Placed Design	Prohibit
Read Constraints	Allow
Group	Remove
Group by	Remove All
Remove Group	Undo

Move	Rename
Sort	Place
Flatten	Place and Route
ReBuild	Distribute (in place)
UnPlace Last	Stack (in place)
Impose Pattern	Flip Vertical
	Flip Horizontal

UnPlace Last (Process Menu)

This command undoes all changes made to the floorplan by the most recent reading of a placed design file.

This file can be one of the following:

- A result of Read Placed Design
- A PPR result from Place or Place and Route

This command is enabled only after the first time you use the Read Placed Design, Place, or Place and Route commands.

UnSelect All (Edit Menu)

This command deselects all logic and nets in the design. The design logic and nets must be selected before you can perform any hierarchical or floorplan operations on them.

Write Constraints (File Menu)

This command opens the Save as dialog box shown in Figure 5-59 where you can generate a constraints file that represents the current floorplan.

By default, the Floorplanner writes the constraints file into the current directory under the design name.

You can change the current directory if you want to place the constraints file in another location.

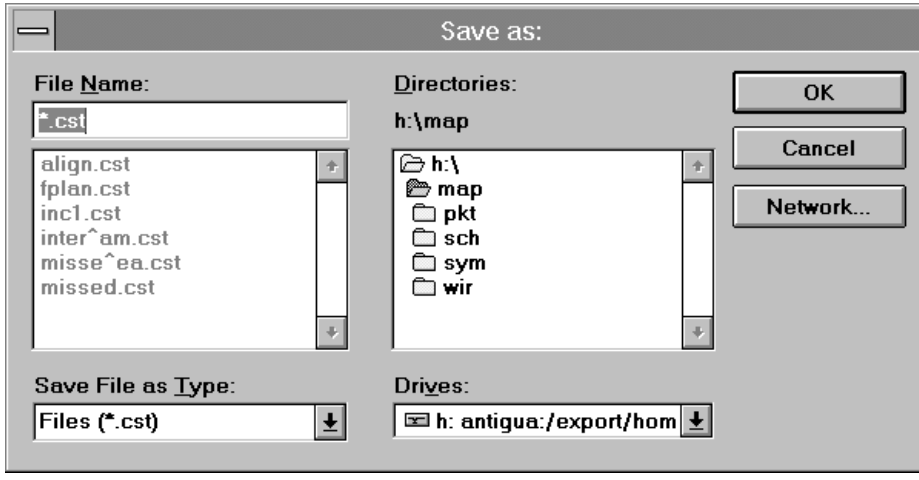


Figure 5-59 Save As Dialog Box (Write Constraints Command)

A description of the fields and buttons on the dialog box follow.

File Name

Permits you to select the name of the CST file that will be created with the Write Constraints command. It also lists existing constraints files that have been created in the current directory during past Floorplanning sessions.

Directories

Lists the directories accessible from the current directory. You can change the current directory by double-clicking in this list.

Save File as Type

Contains a list of available file extensions that you can choose for the file that is to be created.

Drives

Lists the drives that have been defined on your system.

OK

Saves the current floorplan with the file name you have selected and the .cst extension.

Cancel

Cancels the Save As command, closes the dialog box, and returns you to the current floorplanning session.

Network (PC only)

Accesses the network drive. This option is only available if you are running Windows for Workgroups.

Zoom (View Menu)

There are five separate functions available from the Zoom command when the Floorplan window is in focus. Use these functions to adjust the display of the Floorplan window.

Full View

This command sets the scale and the pan position so that the entire FPGA map fits in the window. It also sets automatic resizing, where resizing of the window automatically rescales the view.

In

This command changes the scale so that objects appear larger. It also clears automatic resizing.

Out

This command changes the scale so that objects appear smaller. It also clears automatic resizing.

To Box

This command allows you to use the mouse to drag out an area, then automatically sets the scale and the pan position so that the area is visible. It also clears automatic resizing.

After dragging out a single area, the mouse reverts to the normal Select mode.

To Selected

This command sets the scale and the pan position so that all selected logic is visible. It also clears automatic resizing.

Glossary

This appendix contains glossary definitions of the terms used in this manual.

block

A group consisting of one or more logic functions.

BUFT

Tristate buffer.

CLB

Configurable Logic Block.

critical path

A signal in a section of combinatorial logic that limits the speed of the logic. Storage elements begin and end a critical path, which may include an I/O pad.

design hierarchy

A graphical representation of the MAP file in the Floorplanner Design window.

DFF

D-Latch flip-flop.

function generator

A look-up table or black box with three or four inputs implementing any combinational functions of $(2^2)^3$ or 256 functions or $(2^2)^2$ or 65556 functions. The output is any value resulting from the logical functions executed within the box. The function generator implements a complete truth table, allowing speedy prediction of the output.

guide file

An LCA file representing a previously placed and routed design, which is used in a subsequent place and route operation.

HDL

Hardware Description Language. The most common HDLs in use today are Verilog and VHDL. They describe designs in a technology-independent manner using a high level of abstraction.

IOB (input/ouput block)

An IOB is a collection or grouping of basic elements that implement the input and output functions of an FPGA device.

I/O blocks

The input/output logic of the device containing pin drivers, registers, and latches, and tristate control functions.

I/O pads

The input/output pads interface the design logic with the pins of the device.

logic icon

Graphical representation of a logic resource, such as a flip-flop, buffer, or register.

logic icons in transit

Selected logic that is being moved from one location to another in the Floorplanner.

longlines

Each CLB has four dedicated vertical longlines, and each of these lines connects to a primary global net or to any secondary global net. These lines are very fast. See switch matrix.

map

The process of assigning a design's logic elements to the specific physical elements that actually implement logic functions in a device.

menu bar

The area located at the top of the main window that provides access to the menus.

net

A logical connection between two or more symbol instance pins. After routing, the abstract concept of a net is transformed to a physical connection called a wire.

optimize

The process of transforming a design to decrease its area or to increase its speed performance.

pad

The physical bonding pad on an integrated circuit. All signals on a chip must enter and leave by way of a pad. Pads are connected to package pins in order for signals to enter or leave an integrated circuit package.

place

The process of putting logic from your design into physical cell locations in the FPGA.

ratsnest

Lines that indicate connectivity between logic placed in the Floorplanner window.

resource graphics

Graphical representation of elements in the target FPGA Floorplan window, such as function generators, registers, tristate buffers in the CLB, and IOBs.

route

The process of assigning logical nets to physical wire segments in the FPGA that interconnect logic cells.

router

The utility that connects all appropriate pins to create the design's nets.

schematic

An electronic drawing representing a design in terms of primitive elements.

selecting logic

In the Floorplanner, the process of using the mouse to choose logic in either the Design window or the Floorplan window for placement, movement, or processing.

status bar

An area located at the bottom of a window that provides information about the commands that you are about to select or that are being processed.

tristate buffer

A logic primitive with three possible output states.

toolbar

A field located under the menu bar at the top of your window. It contains a series of icons (buttons) that you click on to execute some of the most commonly used commands. These buttons constitute an alternative to the menu commands.

Appendix B

Error and Warning Messages

This appendix contains the error and warning messages that the Floorplanner can generate. Each error or warning message is numbered. A brief description of the problem and possible solution accompanies each message.

Warning Messages

`W12936 Cannot place symbol` *symbol* `on block` *block* `because it is already occupied.`

Cause:

- There are overlapping constraints in your constraints file.
- There are overlapping constraints in the LOC parameters in your design's MAP file
- A symbol in the constraints file or MAP file is constrained to a location where another symbol has been floorplanned.

Workaround:

Examine your constraints file and fix any overlapping constraints. If you have logic floorplanned in a location that is assigned to another symbol, move the floorplanned to another location in the die.

`W12925 Cannot place symbol` *symbol* `on prohibited block` *block*

Cause:

The symbol has a constraint or LOC parameter attached to it that calls out a prohibited location on the floorplan.

Workaround:

Change the constraint or LOC parameter of the symbol to an allowable location in the floorplan.

`W12926 Symbol` *symbol* `in constraint file was not found`

Cause:

The symbol called out in the constraints file does not exist in the design.

Workaround:

Edit the constraints file and remove the offending symbol.

`W12927 Cannot place symbol` *symbol* `on block` *block*

Cause:

The location to which you want to constrain the symbol is illegal for the current part.

Workaround:

Place the symbol at a location in the floorplan that is legal for the target device. Change the target device to another part in which the constraint is legal for the symbol.

`W12928 Cannot find block` *block* `to prohibit`

Cause:

The block that you want to prohibit does not exist for the current part.

Workaround:

Select another block in the current part.

`W12929 Constraint error for RPM` *rpm_name*

Cause:

- The RPM cannot be constrained to the location you have specified because the location is illegal.
- The RPM cannot be constrained to the location because all of the symbols could not be placed due to an obstacle.

Workaround:

Change the RPM constraints to a legal location on the floorplan. Remove the obstacle preventing the placement of all symbols in the RPM.

`W12930 RPM` *rpm_name* `in constraint file was not found`

Cause:

The RPM named in the constraints file does not exist in the design.

Workaround:

Edit the constraints file with the correct RPM.

`W12931 Constraint(s) on RPM symbol` *symbol* `is not allowed`

Cause:

A constraint was assigned illegally to a symbol that was a part of an RPM.

Workaround:

Remove the constraint on the offending symbol. You cannot assign a constraint to a symbol that is part of an RPM.

`W12954 Cannot place symbol` *symbol* `on block` *block* `because they are incompatible.`

Cause:

The symbol has a constraint that calls out an incompatible block type. For example, trying to place a function generator into a flip-flop resource.

Workaround:

Replace the constraint on the symbol with one that is compatible.

Warnings Generated by the Read Placed Design Command

`W12937 The CLB with output net` *netname* `was not found in the design.`

Cause:

A correlation between a placed CLB in the LCA file could not be found with the current design that is loaded in the Floorplanner.

Workaround:

Verify that you have loaded the correct LCA file for the current design.

`W12938 The DFF with output net` *netname* `was not found in the design.`

Cause:

A correlation between a placed D flip-flop in the LCA file could not be found with the current design that is loaded in the Floorplanner.

Workaround:

Verify that you have loaded the correct LCA file for the current design.

`W12939 The CY4 with input net` *netname* `was not found in the design.`

Cause:

A correlation between a placed carry logic symbol in the LCA file could not be found with the current design loaded in the Floorplanner.

Workaround:

Verify that you have loaded the correct LCA file for the current design.

`W12940 The CY4 with output net` *netname* `was not found in the design.`

Cause:

A correlation between a placed carry logic symbol in the LCA file could not be found with the current design loaded in the Floorplanner.

Workaround:

Verify that you have loaded the correct LCA file for the current design.

`W12941 The FG or MEM with output net` *netname* `was not found in the design.`

Cause:

A correlation between a placed function generator or RAM/ROM in the LCA file could not be found with the current design that is loaded in the Floorplanner.

Workaround:

Verify that you have loaded the correct LCA file for the current design.

`W12942 The IOB named` *symbol* `was not found in the design.`

Cause:

A correlation between a placed IOB in the LCA file could not be found with the current design that is loaded in the Floorplanner.

Workaround:

Verify that you have loaded the correct LCA file for the current design.

`W12943 The BUFT named` *symbol* `was not found in the design.`

Cause:

A correlation between a placed tristate buffer in the LCA file could not be found with the current design that is loaded in the Floorplanner.

Workaround:

Verify that you have loaded the correct LCA file for the current design.

`W12944 The BUFGP or BUFGS with output net` *netname* `was not found in the design.`

Cause:

A correlation between a placed global buffer in the LCA file could not be found with the current design that is loaded in the Floorplanner.

Workaround:

Verify that you have loaded the correct LCA file for the current design.

`W12946 The FG symbol,` *symbol,* `was not found in the design.`

Cause:

A correlation between a placed function generator in the PM file could not be found with the current design that is loaded in the Floorplanner.

Workaround:

Verify that you have loaded the correct PM file for the current design.

`W12947 The F5_MUX symbol,` *symbol,* `was not found in the design.`

Cause:

A correlation between a placed F5_MUX in the PM file could not be found with the current design that is loaded in the Floorplanner.

Workaround:

Verify that you have loaded the correct PM file for the current design.

`W12948 The DFF symbol, symbol, was not found in the design.`

Cause:

A correlation between a placed D flip-flop in the PM file could not be found with the current design that is loaded in the Floorplanner.

Workaround:

Verify that you have loaded the correct PM file for the current design.

`W12949 The DLAT symbol, symbol, was not found in the design.`

Cause:

A correlation between a placed DLAT in the PM file could not be found with the current design that is loaded in the Floorplanner.

Workaround:

Verify that you have loaded the correct PM file for the current design.

`W12950 The CY_MUX symbol, symbol, was not found in the design.`

Cause:

A correlation between a placed CY_MUX in the PM file could not be found with the current design that is loaded in the Floorplanner.

Workaround:

Verify that you have loaded the correct PM file for the current design.

`W12951 The BUFT symbol, symbol, was not found in the design.`

Cause:

A correlation between a placed tristate buffer in the PM file could not be found with the current design that is loaded in the Floorplanner.

Workaround:

Verify that you have loaded the correct PM file for the current design.

`W12952 The BUFG symbol,` *symbol,* `was not found in the design.`

Cause:

A correlation between a placed global buffer in the PM file could not be found with the current design that is loaded in the Floorplanner.

Workaround:

Verify that you have loaded the correct PM file for the current design.

`W12953 The IOB symbol,` *symbol,* `was not found in the design.`

Cause:

A correlation between a placed IOB in the PM file could not be found with the current design that is loaded in the Floorplanner.

Workaround:

Verify that you have loaded the correct PM file for the current design.

Floorplanner Error Messages

This section describes the error messages that the Floorplanner can generate. A brief description of the problem and possible solution accompanies each message.

`E12901 Error opening file:` *filename*

Cause:

The Floorplanner could not open the file you specified. The proper read permission is not set or, the design does not exist.

Workaround:

- Verify that you have the proper file permissions to the file you have specified.
- Verify that the design exists in the directory specified in the path to the design.

`E12902 Error opening file:` *filename*

Cause:

The Floorplanner could not open the named constraints file. The proper read/write file permissions are not set or, the file does not exist.

Workaround:

- Verify that you have the proper file permissions to the file you have specified.
- Verify that the design exists in the directory specified in the path to the constraints file.

`E12903 Unable to load design` *design_name*

Cause:

The Floorplanner was unable to load the specified design.

Workaround:

- Verify that the specified design file exits.
- Check that there are no syntax errors in the MAP file (if you have edited this file).
- Verify that you have the proper read permissions for the file.

`E12904 Could not change directory to "`*directory*`"`

Cause:

The Floorplanner was unable to change to the named directory.

Workaround:

Ensure that the directory exists and the file permissions allow to read the directory.

`E12905 The design cannot be opened because the given directory "`*directory*`" cannot be opened.`

Cause:

The specified design could not be opened because the directory it is in is not readable by the user.

Workaround:

Change the file permissions for the directory in which the design resides so that you have read permissions.

`E12909 Unable to load part type` *device*`.`

Cause:

The Floorplanner could not load the device that is specified in the design.

Workaround:

- Verify that the requisite data files needed to support the specified part type can be read by the Floorplanner.
- If you have edited the "PART" field in the MAP file, ensure that you have specified a supported part type.

`E12911 The XACT Floorplanner help file "`*help file*`" could not be found.`

Cause:

The files for the online help could not be found.

Workaround:

Check your system setup.

`E12917 Could not find "PPR" path.`

Cause:

The Floorplanner could not find PPR in the search path.

Workaround:

Verify that the XACT variable is in the current search path for your system and properly defined to include PPR.

`E12918 Error creating the processing batch file`

Cause:

This is a Windows-only error. The Floorplanner could not create a batch file from which to invoke PPR.

Workaround:

Close all unrelated applications and files.

```
E12919 Error! Cannot find the necessary PIF file.
```

Cause:

This is a Windows-only error. The Floorplanner could not find a PIF file with which to run PPR, which may indicate a setup problem.

Workaround:

Ensure that the proper xftshmt.pif file is in the XACT data directory.

```
E12920 Error copying the necessary PIF file.
```

Cause:

This is a Windows-only error. This error may be a system error such as having too many files open, or due to a network problem.

Workaround:

Close all unrelated applications and files.

```
E12921 Error in spawning batch file process from
floorplanner.
```

Cause:

This is a Windows-only error. This error may be a system error such as having too many files open, or due to a network problem

Workaround:

Close all unrelated applications and files.

```
E12922 System Error! There are no available
TIMERS.
```

Cause:

This is a Windows-only error. MS-Windows has a limited number of timers for applications. Currently all timers are being used, so the Floorplanner cannot invoke PPR and check when PPR completes.

Workaround:

Close all unrelated applications.

`E12923 A system setup error occurred while loading in your design.`

Cause:

The Xilinx software may be improperly installed.

Workaround:

Ensure that the software is properly installed on your system.

`E12924 Unable to allocate memory for design.`

Cause:

The system does not have enough memory to open the specified design.

Workaround:

Contact your system administrator about increasing the memory on your system.

`E12934 Cannot guide mapping of` *design* `because` *design*`.map could not be loaded. Floorplanner will load previously saved design.`

Cause:

The Floorplanner could not guide the design because the MAP file could not be properly loaded. It will only load the FPN file.

Workaround:

Verify that MAP file in question is valid and that you have read permissions on that file

`E12935 Could not find guide file` *filename*

Cause:

The guide file that you specified for PPR could not be found.

Workaround:

Verify that the specified guide file exists.

`E12945 The placed design,` *`design_name`*`, was targeted for a different device` *`parttype`*`. Unable to process placed design.`

Cause:

The LCA/PM file has the design placed in a different part than the one currently loaded in the Floorplanner.

Workaround:

You must choose the appropriate LCA/PM file.

Index

D

E

F

G

H

I

K

L

M

N

O

P

Q

R

S

T

U

V

W

X

Z

Trademark Information