HDL Verification

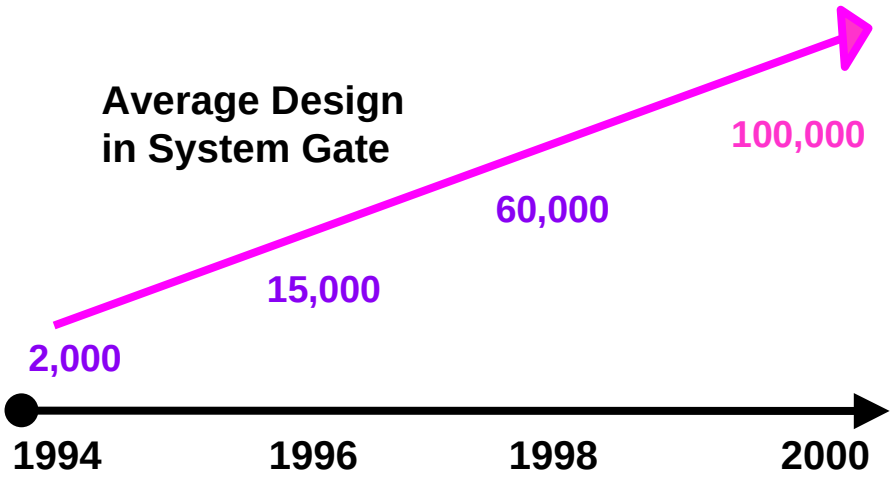
We will take you to the leaders.

Powerful HDL Verification Solutions for the Industries Highest Density Devices

- What is driving the FPGA Verification trends?
- What is an HDL Testbench Methodology?
- What is Xilinx doing to lead the way?
- Visit our WEB site at:
  http://www.xilinx.com/products/alliance.htm
- Appendix
  - Who are our partners?
  - What are the future verification tools?

What's Driving the FPGA Verification Trends?

The average FPGA design size is increasing dramatically year-to-year



"In 2000 the average design size will be over 100,000 gates"

- Sandeep Vij, Xilinx GM High Volume

The Changing Verification Trends

1994

- Schematic Capture
- Functional and Timing Simulation
- Static Timing analysis for critical paths
- In-system verification

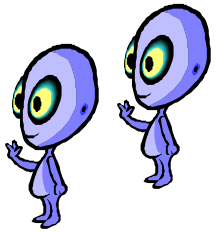
Single designer

1998

Plus

- HDL
- Functional & timing simulation using HDL simulator

Small teams



Dedicated verification engineers

2000

Plus

- IP
- Formal verification

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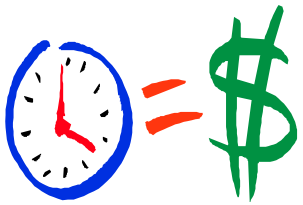
What are the Challenges Today?

- As design size and complexity increase the cost of find error increase exponentially over time
  - Errors detected early in the design cycle are **cheap to fix**
  - Errors detected late require redesign and re-verification **are expensive**
  - Debugging a chip to isolate errors is **time consuming or impossible**
- Design cycles are getting longer
- Large designs use team and modular design techniques
- FPGAs are replacing ASICs

"At 60K gates HDL simulation becomes a requirement"

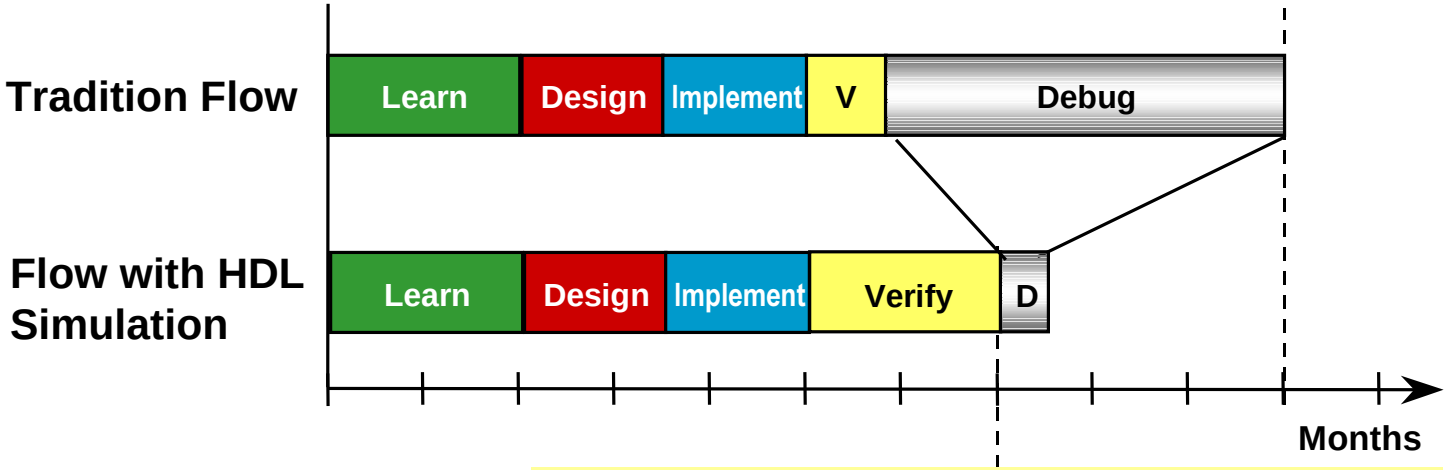
Rich Sevick, Senior VP Software

- Increase your productivity
- Get to market faster



- Make design changes faster
- Team design requires module verification
- Widely used by ASIC designers

Gaining Productivity through HDL Simulation



Increasing HDL Simulation
reduced expensive and lengthy chip-level debug

I reduced my design cycle by 25% by adopting an HDL simulation methodology

- Steve Winkelman, Display Tech

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Testbench Methodology

- Testbench methodology is based on developing a specification and testing to the specification
  - Provides stimulus and response information
- Why adopt?
  - Isolates the problem fast
  - Find and fix the problem as early as possible
  - Perform hardware regression, software and system debug is parallel
  - Test different RTL (register transfer level) implementation by plugging in different architectures

HDL Verification Design Flow

RTL - Register Transfer

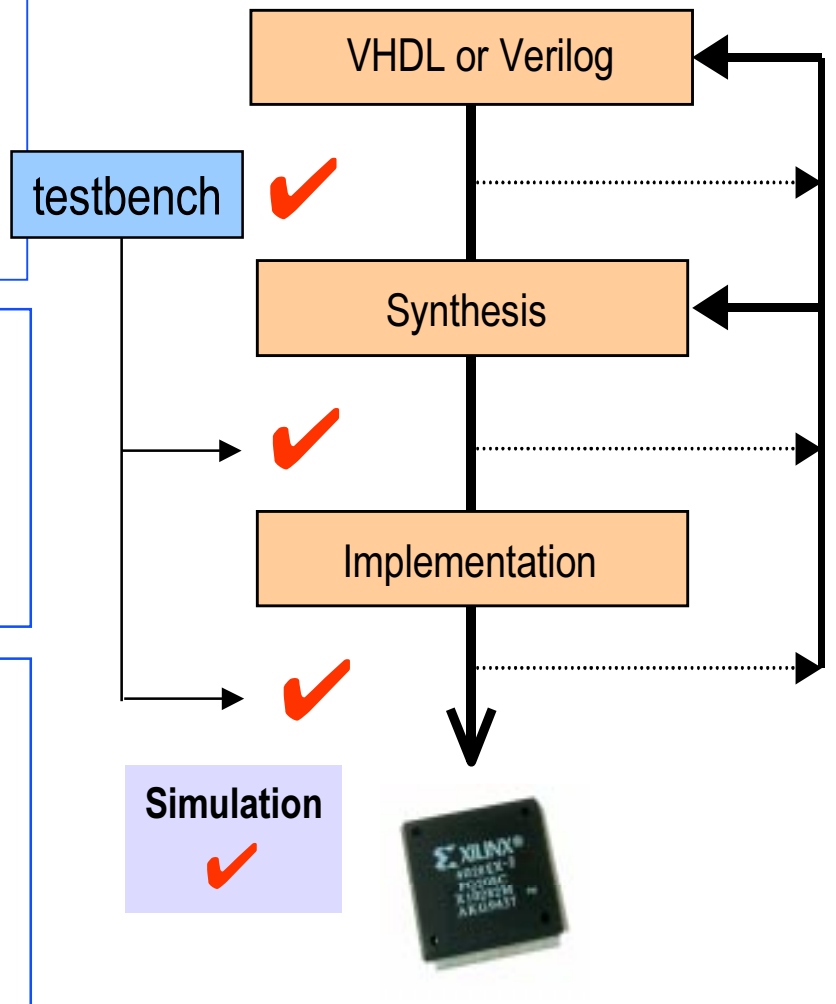
- Create testbench
- Verifies syntax & functionality
- Majority of design cycle time
- Errors found are inexpensive to fix

Gate-level Functional

- Checks the synthesis implementation to gates
- Test initialization states
- Analyze ‘don’t care’ conditions

Gate-level Timing

- Post implementation timing simulation
- Test race conditions
- Test set-up and holds violations based on operating conditions



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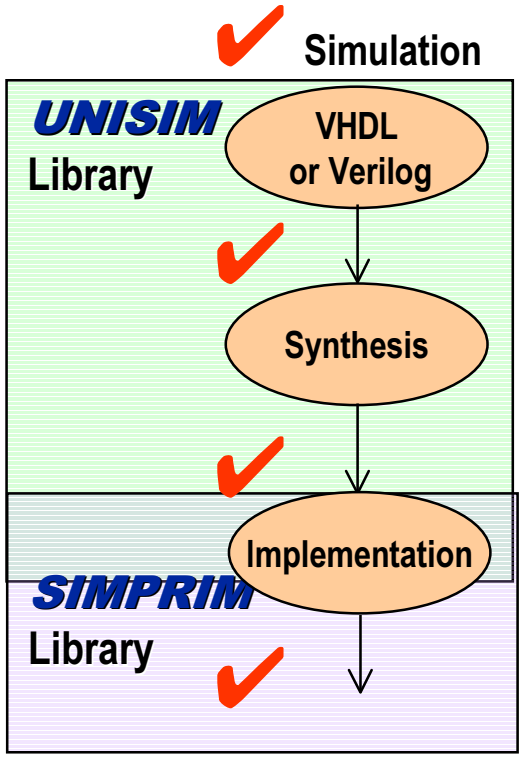
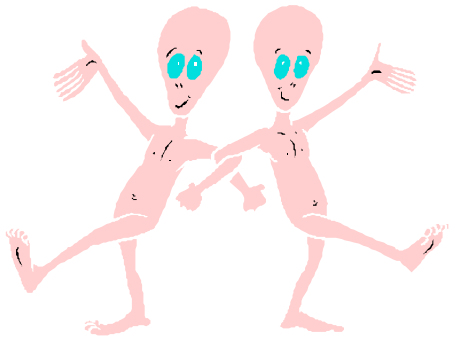
What Does Xilinx Provide for You?

- Libraries and interfaces provided to simulate anywhere in the design flow
  - Functional simulation with ***UNISIM***
  - Timing simulation with ***SIMPRIM***
- Mixed mode simulation
  - Schematic and HDL
  - Multiple EDA vendors
- Early adopters of industry standards
  - VITAL, Verilog, VHDL and SDF
  - Defining these standards for FPGAs
  - Continue libraries development that focus on minimizing compile time
- Unique VHDL simulation of Global Set/Reset capabilities



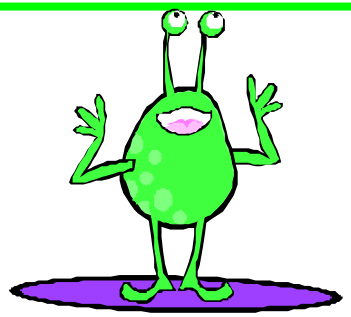
What Does Xilinx Provide for You?



- Expertise
  - Technical articles and design guides with getting started and verification tips
    - How to verify for PCI compliance
  - July 98 supplement issue of XCELL dedicated to Verification
  - Leaders in high density methodology research
- Minimum Delays
  - Guarantee your designs performance with both minimum and maximum process delays
  - Design and test asynchronous circuits
- Voltage and Temperature Prorating
  - Test your design under favorable operating conditions
  - Achieve higher speeds if voltage and temperatures conditions are better than worstcase specifications

Other Verification Tools

- Critical path identifications
- Cross probing and highlighting between Schematic,HDL and Simulation
  - For faster debugging
- System level documentation
  - Board schematics, bill of materials for production, PCB layout netlist
  - Complete data on Xilinx devices for production
- Board level debugging



What are the Future Verification Tools?

- **Formal Verification**
  - Reduces the time to perform regression simulation of gate-level implementation through equivalency checking
  - Complete coverage without vectors
- **HVL - Hardware Verification Languages**
  - Verilog and VHDL were not optimally designed for verification
  - Write compact highly readable testbench
- **Emulation**
  - Rapid prototyping for large ASIC and system verification
  - Run test at system speeds
  - 10x reduction in verification time
- **Cycle-Base Simulation**
  - Functional testing of synchronous designs at cycle boundaries
  - Dramatic runtime reductions

What's Coming?

Version 2.1
Q199

- **Static Timing Analysis**
  - Checks timing characteristics
  - Reduces timing verification time
- **System Level Models**
  - Fast advance verification and debugging capabilities
  - Models are templates of configured devices that are programmed by a design's FPGA netlist
- **Embedded Implementation into Synthesis**
  - Get an accurate estimation of your critical path before implementation

Interstellar Map to HDL Verification Partners

VHDL Simulators

Aldec Active-VHDL™
+ VHDL Simulator
www.aldec.com
(702) 456-1222

Model Technology ModelSim/VHDL™
www.model.com
503 641-1340

OrCAD Express™
VHDL simulator plus more
www.orcad.com
1-800-671-9505

Synopsys VSS™
VHDL System Simulator
www.synopsys.com
1-800-245-8005

VeriBest VHDL ChipSim™
www.veribest.com
1.888.482.3322

Viewlogic Fusion/ Speedwave™
www.viewlogic.com
508-480-0881

Verilog Simulators

Cadence Verilog-XL™ Verilog-XL Turbo™ Verilog-XL Turbo NT™
www.cadence.com
1-800-CADENC2

Model Technology ModelSim/VLOG™
Gate & RTL Verilog Simulation
www.model.com
503 641-1340

Synopsys Chronlogic VCS™
Verilog System Simulator
www.synopsys.com
1-800-245-8005

VeriBest Verilog Simulator™
www.veribest.com
1.888.482.3322

Viewlogic Fusion / VCS™
www.viewlogic.com
508-480-0881

Mixed & Gate

Mentor QuickSim II™
Gate-level Simulator
www.mentor.com
800-547-3000

Mentor SimView™
Common Simulator Interface
www.mentor.com
800-547-3000

Mentor QuickHDL Pro™
QuickHDL and QuickSim Co-simulator
www.mentor.com
800-547-3000

Mentor QuickHDL™
Mixed Verilog and VHDL
www.mentor.com
800-547-3000

Model Technology ModelSim/PLUS™
Mixed Verilog and VHDL
www.model.com
503 641-1340

VeriBest VHDL SysSim™
VHDL simulator for and system designs
www.veribest.com
1.888.482.3322

Viewlogic Fusion Viewsim™
Gate-level Simulator
www.viewlogic.com
508-480-0881

Other

Exemplar Leonardo Spectrum™
www.exemplar.com
(510) 789-3333

Synopsys RTL Analyzer™
RTL Performance Debugger
www.synopsys.com
1-800-245-8005

Synopsys LMG™
System Level Modeling
www.synopsys.com
1-800-245-8005

Synplicity HDL Analyst™
Displays timing information for critical paths, cross probing, + more
www.synplicity.com
408-617-6000

In Summary

Design Verification is the most critical task in successfully creating complex designs and getting to market faster

Kevin Curtis, General Manager Model Technology

Engineers have found that a HDL simulation strategy improves their productivity and keeps the design project on schedule

Hitesh Patel, Xilinx Technical Marketing Manager

Appendix

Simulate FPGA Dedicate Global Signals

- Problem: How do you simulate and monitor global signals in VHDL when VHDL requires you to declare all signals as ports?
  - Global Set/Reset and Global 3-state is used to initialize the FPGAs and an be utilized by the designer to save routing resources
  - The declaration of these ports would make pre- and post-implementation verification of your design different
  - One testbench can no longer be used through-out the flow
- Solution: New library cells and interface provides:
  - Easy way to implement and simulate GSR/GTS behavior
  - Uses only one testbench
  - Automatically utilize the existing routing resources improving your designs performance
  - Automatically adds or deletes required I/O pins
  - Simulate with any VITAL compliant simulator